SmartFusion2 SOM (System-On-Module)

Hardware Architecture

Version 1.1

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems SmartFusion2 SOM (System-On-Module).

The SmartFusion2 SOM is intended to provide a flexible platform for embedded applications that require rich connectivity, low power and flexibility of the SmartFusion2 SoC (System-on-Chip) FPGA device coupled with a full-fledged Linux software execution environment running on the ARM Cortex-M3 SmartFusion2 processor core.

The SmartFusion2 SOM is based on the Microsemi SmartFusion2 versatile, low-power, high-integration microcontroller. The uClinux kernel and applications execute on the 166 MHz 32-bit ARM Cortex-M3 processor core, while the integrated controllers and FPGA fabric of the SmartFusion2 device are used to implement various communication interfaces and protocols.

Using a miniature mezzanine form factor, the SmartFusion2 SOM is specifically designed to provide the primary SmartFusion2-based intelligence on various boards targeting industrial automation, system and power management, wireless networking / sensors and other embedded applications. SmartFusion2 SOM hardware and software are architected to ensure flexibility in customizing its functionality for the needs of particular products and/or customers.

2. Hardware Platform

This section defines the hardware platform of the SmartFusion2 SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the SmartFusion2 SOM:

- Compact (34 mm x 59 mm) mezzanine module;
- External interface using two 80-pin 0.4 mm-pitch connectors;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- SmartFusion2 SoC FPGA in FG896 package capable of running the system clock at up to 166 MHz;
- JTAG interface to SmartFusion2;
- Powered from single +3.3 V power supply;
- Low-power mode with fast wake-up times;
- On-module clocks;
- 64 MBytes LPDDR;
- 16 MBytes SPI Flash;
- Serial console interface at UART CMOS levels;
- 802.3 Ethernet interface;
- Watchdog Timer (WDT);
- Key uncommitted interfaces of the SmartFusion2 device available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the SmartFusion2 SOM:

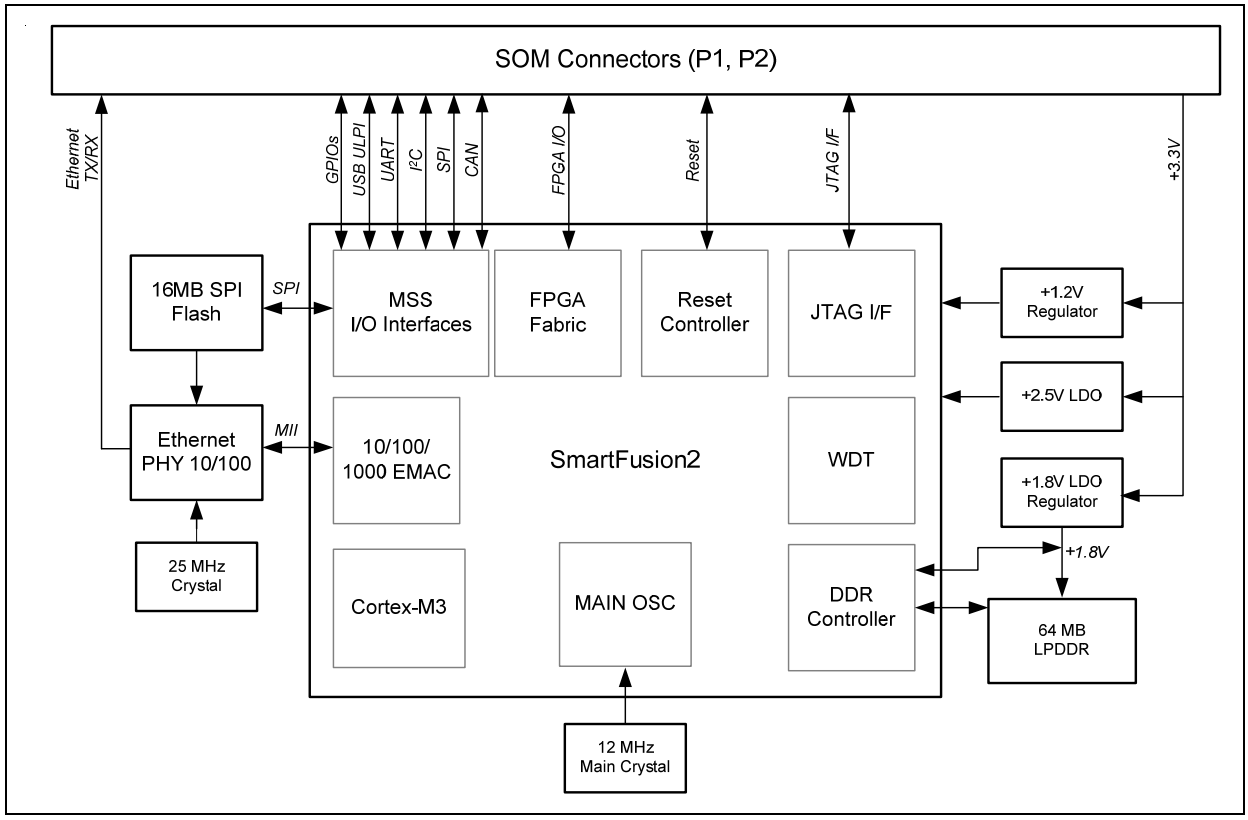

Figure 1: SmartFusion2 SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. SmartFusion2 FPGA

The architecture of the SmartFusion2 SOM is built around the Microsemi SmartFusion2 SoC FPGA that combines a 32-bit ARM Cortex-M3 processor core with a wide range of the integrated peripheral controllers as well as the FPGA fabric.

The SmartFusion2 device is implemented using the FG896 package.

2.3.2. SmartFusion2 Configuration

The SmartFusion2 SOM supports build-time selection of the following SmartFusion2 devices:

- Capacity:
  - M2S050T-ES[1] (48672 Logic Units, 256 KB eNVM, 64 KB eSRAM)
- Speed Grade:
  - Standard Grade
- Temperature Range:
  - Room temperature only

Selection of any of the options above in an actual assembled unit does not affect the other sections of the hardware architecture. For those configuration options that affect software

[1] *Currently, Libero V11.0 SPA shows M2S050T as the part number. In a service pack SP1, there is a part number M2S050T_ES that is selectable as the device and the users should select M2S050T_ES as the device.*

functionality, software running on the SmartFusion2 SOM is expected to determine the specific microprocessor configuration at run-time and adjust its operation accordingly.

2.4. JTAG Interface

The SmartFusion2 SOM provides a FlashPro-3/4-compatible JTAG interface on the interface connectors. The JTAG interface is routed to the corresponding signals of the SmartFusion2 device.

2.5. FPGA

2.5.1. SmartFusion2 On-Chip Configuration and FPGA Design

Customers of the SmartFusion2 SOM are provided with a SmartFusion2 on-chip configuration and FPGA design suitable for the intended operation of the SmartFusion2 SOM.

The SmartFusion2 SOM on-chip configuration and FPGA design can be viewed as an extension of the SmartFusion2 SOM hardware design. It contains a logical definition of the internal SmartFusion2 architecture, which consists of the Microcontroller Subsystem (MSS) configuration, as well as FPGA logic developed by Microsemi and Emcraft Systems. It also describes an electrical interface between the SmartFusion2 device and external components, such as the SmartFusion2 device pin configuration and assignment.

2.5.2. Libero Project

The SmartFusion2 SOM on-chip configuration and FPGA design is provided as a Libero IDE project. It is expected that customers will use this project as a starting point for their application-specific FPGA development.

Note: *It is assumed that the reader is familiar with the Microsemi FPGA development process using the Libero IDE and Libero SoC tools. For more information on these and other Microsemi development tools, refer to the Microsemi SoC Product Group web page at http://www.microsemi.com/soc.*

Note: *The Libero project files included in this release of the SmartFusion2 SOM are intended to be used with Libero SoC v11.0. Using these files with any other release of the Libero IDE or Libero SoC software (earlier or later) may require manual adaptation of the FPGA design.*

In addition to the Libero project files customers are provided with a resulting `.stp` file. This `.stp` file is installed on every SmartFusion2 SOM unit shipped to customers.

The `.stp` file is provided for convenience, allowing the original design to be re-programmed into the SmartFusion2 device using the Microsemi FlashPro programming tool, if necessary. Here is how the `.stp` file can be installed onto SmartFusion2 using the FlashPro tool:

1. Start FlashPro on a Windows host;
2. From the FlashPro IDE, create a new project with an arbitrary name;
3. From the main FlashPro window, push `Configure Device`;
4. Push `Browse` next to `load existing programming file`. Browse to the `.stp` file and choose it;
5. Push `Program` at the top of the main window to program the project onto the SmartFusion2 device and wait for the programming procedure to complete. If the programming completes successfully, a next reset should bring the U-Boot start-up messages and the command line interface onto the serial console interface on the SmartFusion2 SOM.

2.5.3. FPGA IP Programming Interfaces

The Libero project installs the following IP blocks to the FPGA fabric of the SmartFusion2.

Address Range	IP	Tiles	Description	Mandatory / Optional
	None			

Table 1: IP Blocks

2.6. Power

2.6.1. Power Source

The SmartFusion2 SOM is run from a single +3.3 V power source provided through multiple pins on the interface connectors. The SOM converts the +3.3 V input power into other power sources required by the SmartFusion2 SOM design using appropriate on-module circuitry.

2.6.2. Power Modes

The SmartFusion2 SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation where both the MSS and the FPGA fabric are operational. The main clock is running and the Cortex-M3 is active running RTOS and/or application code. All memory controllers are enabled.

  Software is configured to enable only those SmartFusion2 sub-systems that are used by installed device drivers; all other sub-systems are in reset and do not consume power. If the Ethernet interface is not enabled by a corresponding device driver, the Ethernet PHY is in a low power mode (refer to section 2.12.5).

- Low-power mode. This is the mode of operation the Linux software may be configured to enter when the SmartFusion2 SOM is idle from the software perspective. To elaborate, this mode may be entered when Linux has no active processes to run and is running the so-called "idle process". When Linux finds itself in the idle state, it transitions the SmartFusion2 to the Standby mode, which is intended by the SmartFusion2 architecture for applications that intend to put the device into a low-power state but be ready to respond to an interrupt sourced from the MSS and the FPGA. Software transitions into this mode by executing a "wait for interrupt" (WFI) instruction in the Cortex-M3, causing the reference clock to be gated off to the Cortex-M3 processor. This disables the majority of the Cortex-M3 logic. In the Standby mode, the SmartFusion2 device is active, but running off of a lower frequency clock than what is used for normal system operation. Peripherals not being used can be put into a low-power state by asserting their individual resets.

  To put external devices into a low-power mode, the SmartFusion2 SOM provides a dedicated output signal intended as a control for switching off-board devices to low-power modes. This active-low signal is available as `MSIOD138PB7` on the interface connectors.

  When switching the system to the low-power mode, software activates the low-power mode signal. Various on-board and off-board devices are expected to react to activation of that signal by switching themselves to low-power modes. Conversely, when software is switching back to the full-power mode, it de-asserts the low-power mode signal indicating to on-board and off-board devices that they are expected to switch back to the full-power mode.

2.7. System Reset

2.7.1. Reset Architecture Overview

The SmartFusion2 SOM implements a sophisticated reset architecture that ensures that the SmartFusion2 device is reset as appropriate on various hardware and software events.

Software running on the SmartFusion2 SOM is expected to configure the `MSS_RESET_N` signal of the SmartFusion2 device as an output making it a reset request signal for on-board and

off-board devices. The SmartFusion2 SOM ensures that the on-board PHY and Flash devices are reset as soon as the SmartFusion2 SOM is subjected to a reset by connecting this signal to the reset input of the respective devices.

Those off-board devices that require synchronizing their resets with SmartFusion2 SOM resets must connect the active-low DEVRST_N signal to the reset input of a respective device.

2.7.2. Types of System Resets

The following types of reset are implemented by the SmartFusion2 SOM:

- Power-on reset. This type of reset occurs when the SmartFusion2 SOM is being powered-up.
- Power down or power supply fault reset. The integrated triggers the power-on reset sequence as soon as the on-module voltages have gone below certain levels.
- Brown-out reset. In case the +3.3 V supply falls below +2.5 V, the integrated power supply monitor of SmartFusion2 may be configured by software to trigger a brown-out interrupt to the Cortex-M3 processor core. Software running on the SmartFusion2 SOM may chose to handle such an event by initiating the software reset sequence.
- Software reset. This type of reset is activated by software running on the SmartFusion2 SOM through performing the SmartFusion2 software reset sequence.
- WDT reset. This type of reset is activated when the integrated WDT of the SmartFusion2 expires.
- Manual reset. To activate this type of reset, a baseboard drives low the nRESET signal.

2.8. System Clocks

The SmartFusion2 SOM provides a 12 MHz quartz crystal as a reference to the internal oscillator of the SmartFusion2 device.

The SmartFusion2 device contains integrated PLLs driven by the above oscillator from which the various clocks required by the SmartFusion2 subsystems are derived. More specifically, the SmartFusion2 on-chip configuration and FPGA design (refer to section 2.5.1) provide the following clocks for the various SmartFusion2 domains:

Clock	Frequency (MHz)	Purpose
MCCC_CLK_BASE	80	MSS CCC clock source
M3_CLK	166	Cortex-M3 and main MSS clock
MDDR_CLK	166	LPDDR clock
APB_0_CLK	83	APB_0 bus clock
APB_1_CLK	83	APB_1 bus clock

Table 2: System Clocks

In addition to the 12 MHz crystal, the SmartFusion2 SOM provides a dedicated clock reference for the Ethernet sub-section (refer to section 2.12.3).

2.9. SDRAM

2.9.1. SDRAM Architecture

The SmartFusion2 SOM provides 64 MBytes of 5 ns 16-bit LPDDR SDRAM using the Micron MT46H32M16 device. The SDRAM resides at nDDR_CS chip select of the integrated SDRAM controller of the SmartFusion2 MCU.

2.9.2. SDRAM Operational Mode

The SmartFusion2 MCU SDRAM controller operates in the Low-Power Dual Data Rate Mode.

2.9.3. SDRAM Low-Power Modes

When not accessed, the LPDDR power consumption is only 0.3 mA.

2.10. SPI Flash

2.10.1. SPI Flash Architecture

The SmartFusion2 SOM provides 16 MBytes of SPI Flash memory, using the Spansion S25FL128SDPBHICO SPI0 controller of the SmartFusion2 device.

2.10.2. Flash Low-Power Mode

When not accessed, the SPI Flash power consumption is only 100 uA.

2.11. Serial

2.11.1. UART Controller

The SmartFusion2 SOM provides an UART serial interface at CMOS levels (no RS-232 buffer) using the integrated UART0 controller of the SmartFusion2 device on the interface connectors.

This interface is intended as the console interface for the U-Boot and Linux software.

2.11.2. Serial Baud Rate

The UART controller features an internal divider that allows this serial interface to operate at standard baud rates up to 921,6 Kbps.

2.12. Ethernet

2.12.1. Ethernet Controller

The SmartFusion2 SOM provides a full-featured, configurable Ethernet interface capable of 10/100 Mbps data rates using the integrated 802.3 controller of the SmartFusion2 device.

2.12.2. Ethernet Physical Layer

The physical layer of the Ethernet port is implemented using the Micrel KSZ8051MNLI PHY device to provide a full-featured, 10/100 Mps 802.3 interface.

2.12.3. Ethernet Clock

The SmartFusion2 SOM provides a 25 MHz quartz crystal as a clock reference to the Ethernet PHY device.

The KSZ8051MNLI PHY device drives a 25 MHz RX and TX clock inputs of the integrated Ethernet MAC interface of the SmartFusion2 device.

2.12.4. Ethernet Status LEDs

The SmartFusion2 SOM provides two status signals for the Ethernet channel on the interface connectors for controlling off-module Ethernet LEDs. The functionality of these signals is as follows:

- LED_ACT, used to indicate link status (Link when low, No Link when high) and the RX activity when toggling;
- LED_SPD, used to indicate the 10/100 Mbit link status (100 Mbit when low, 10 Mbit when high).

On a baseboard, the status LEDs must be connected between the SmartFusion2 SOM output signals and a +3.3 V plane.

2.12.5. Ethernet Low Power Mode

When not accessed, the PHY can be switched to the Power-Down mode under software control. When in the Power-Down mode, the PHY current consumption is only 2 mA.

2.13. WDT

The SmartFusion2 SOM provides a hardware watchdog function using the integrated WDT module of the SmartFusion2 device.

If the WDT is enabled and software fails to strobe the WDT within the predefined period of time, the watchdog triggers reset.

The WDT timeout period is defined by software.

2.14. External Interface

2.14.1. Interface Connectors

The external interfaces of the SmartFusion2 SOM are routed through two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors.

2.14.2. Connectors Pin-Out

Note: *Users of the Rev1A SOM (SF2-STARTER-KIT-ES) and Rev2A SOM (SF2-STARTER-KIT-ES-2) should be aware of the following planned design change. With the next revision of the Emcraft Systems SmartFusion2 SOM, certain 3.3 V signals available on the SOM interface connectors will be switched to 2.5 V LVCMOS signals.*

Any such signals are marked with "(2.5 V)" in Column "Type" in the following tables. Any signals that do not have such marking are 3.3 V signals.

The reason for this change is that the SmartFusion2 IO banks that drive these signals have a max voltage rating of 2.5 V. Driving these signals at 3.3 V reduces the lifetime of the SmartFusion2 device to approximately 2.7 years. Switching these signals to 2.5 V will eliminate this problem.

It is extremely important that customers planning to design custom baseboards for the SmartFusion2 SOM or add-on boards for the SOM-BSB-EXT baseboard be aware of this change, and plan their 2.5/3.3 V signals use accordingly.

Note: *For the multi-function SmartFusion2 signals, the item in Bold shows the function initialized by the Libero project included with the SmartFusion2 Starter Kit.*

The following table details the allocation of the external interface connectors pins on the P1 connector:

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
Power (14 pins)					
2, 3, 5, 8, 9, 11, 14, 57, 75, 76	GND	Power	SOM ground	SmartFusion2 GND	Must be connected to GND on a baseboard.

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
77, 79	VCC3	Power	+3.3 V power supply	SmartFusion2 +3.3 V power supply	An external +3.3 V+/- 5% power supply must be applied to these pins.
13	nRESET_IN	Input	SOM reset input	AC27 (**DEVRST_N**)	Active-low hardware reset to the SOM.
15	nRESET_OUT (MSIO102PB8 in SOM Rev 3A)	Output	SOM reset output	R2 (**MSIOD119NB7**)	Active-low reset from the SOM to external devices. Connected to the SmartFusion2 pin J1 (MSIO102PB8) in SOM Rev 3A. Connected to the SmartFusion2 pin AC27 (**DEVRST_N**) in Rev1A.
JTAG (7 pins)					
20	JTAG_TCK	Input	JTAG clock signal to the SmartFusion2	AC26 (JTAG_TCK/ M3_TCK)	
22	JTAGSEL	Input	SmartFusion2 JTAG controller mode selection	AA25 (JTAGSEL)	When driven high, the SmartFusion2 JTAG controller is in the FPGA programming mode. When driven low, the SmartFusion2 JTAG controller is in the Cortex-M3 debug mode.
24	JTAG_TMS	Input	JTAG mode select	AB27 (JTAG_TMS/ M3_TMS/ M3_SWDIO)	
36	JTAG_nTRST	Input	JTAG controller reset	AB25 (**JTAG_TRSTB**/ M3_TRSTB)	Active-low
38	JTAG_TDO	Output	JTAG data output from the SmartFusion2	AC25 (JTAG_TDO/ M3_TDO/ M3_SWO)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
47	JTAG_TDI	Input	JTAG data input to the SmartFusion2	Y23 (JTAG_TDI/ M3_TDI)	
62	VJTAG_VPP	Power			Not connected on M2S-SOM.
Serial (4 pins)					
28	UART_1_TXD	Output	SmartFusion2 MSS UART1 transmit data output/ GPIO	H30 (MSIO41NB1/ **MMUART_1_TXD**/ GPIO_24_B/ USB_DATA2_C)	
29	UART_0_TXD	Output	SmartFusion2 MSS UART0 transmit data output/ GPIO	H27 (MSIO46NB1/ MMUART_0_TXD/ GPIO_27_B/ USB_DIR_C)	Used for the software console interface.
30	UART_0_RXD	Input	SmartFusion2 MSS UART0 receive data input/ GPIO	L23 (MSIO47PB1/ MMUART_0_RXD/G PIO_28_B/ USB_STP_C)	Used for the software console interface.
31	UART_1_RXD	Input	SmartFusion2 MSS UART1 receive data input/ GPIO	G29 (MSIO42NB1/ **MMUART_1_RXD**/ GPIO_26_B/ USB_DATA3_C)	
Ethernet (6 pins)					
1	LED_ACT	Output	Ethernet Link/Activity status		Low – Link, High – No Link, Toggling – RX activity.
4	TD_P	Output	Ethernet differential positive transmit signal		TD_N and TD_P signals should be routed on a baseboard with a 100 Ohm differential impedance.
6	TD_N	Output	Ethernet differential negative transmit signal		
7	LED_SPD	Output	Ethernet 10/100Mbit link status		Low – 100 Mbit, High – 10 Mbit.
10	RD_P	Input	Ethernet differential positive receive signal		RD_N and RD_P signals should be routed on a baseboard with a 100 Ohm differential impedance.
12	RD_N	Input	Ethernet differential negative receive signal		

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
GPIO (29 pins)					
16	MSIOD138PB7 (MSIO102NB8 in SOM Rev 3A)	Input/Output		AC2 (MSIOD138PB7)	When low, enables a low-power mode of external devices. If the low-power mode control signal is not needed, this pin can be used as an FPGA signal. Connected to the SmartFusion2 pin J2 (MSIO102NB8) in SOM Rev 3A.
17	MSIOD139NB7	Input/Output (2.5 V)		AD1 (MSIOD139NB7)	
18	MSIOD140NB7	Input/Output (2.5 V)		AC3 (MSIOD140NB7)	
19	MSIOD139PB7	Input/Output (2.5 V)		AD2 (MSIOD139PB7)	
21	MSIOD143NB7	Input/Output (2.5 V)		AD3 (MSIOD143NB7)	
23	MSIOD138NB7	Input/Output (2.5 V)		AC1 (MSIOD138NB7)	
32	MSIOD143PB7	Input/Output (2.5 V)		AC4 (MSIOD143PB7)	
34	MSIOD134NB7	Input/Output (2.5 V)		AA1 (MSIOD134NB7)	
35	MSIOD134PB7	Input/Output (2.5 V)		AA2 (MSIOD134PB7)	
37	MSIOD135NB7	Input/Output (2.5 V)		AB1 (MSIOD135NB7)	
39	MSIOD135PB7	Input/Output (2.5 V)		AB2 (MSIOD135PB7)	
40	MSIOD127PB7	Input/Output (2.5 V)		V1 (MSIOD127PB7)	
41	MSIOD144PB7	Input/Output (2.5 V)		V7 (MSIOD144PB7)	
42	MSIOD130PB7	Input/Output (2.5 V)		V5 (MSIOD130PB7)	
43	MSIOD128NB7	Input/Output (2.5 V)		W1 (MSIOD128NB7)	
44	MSIOD129PB7	Input/Output (2.5 V)		V6 (MSIOD129PB7)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
45	MSIOD131NB7	Input/Output (2.5 V)		Y1 (MSIOD131NB7)	
46	MSIOD133NB7	Input/Output (2.5 V)		W6 (MSIOD133NB7)	
48	MSIOD141PB7	Input/Output (2.5 V)		W7 (MSIOD141PB7)	
49	MSIOD131PB7	Input/Output (2.5 V)		Y2 (MSIOD131PB7)	
50	DDRIO165PB5	Input/Output (2.5 V)		AK18 (DDRIO165PB5/ FDDR_DQ16)	
51	DDRIO165NB5	Input/Output (2.5 V)		AJ18 (DDRIO165NB5/ FDDR_DQ17)	
52	DDRIO167NB5 (DDRIO148PB5 in SOM Rev 3A)	Input/Output (2.5 V)		AJ19 (**DDRIO167NB5**/ FDDR_DQS2_N)	Connected to the SmartFusion2 pin AK9 (DDRIO148PB5/ PROBE_A) in SOM Rev 3A.
53	DDRIO167PB5	Input/Output (2.5 V)		AK19 (DDRIO167PB5/ FDDR_DQS2)	
54	DDRIO170PB5 (DDRIO148NB5 in SOM Rev 3A)	Input/Output (2.5 V)		AJ20 (**DDRIO170PB5**/ FDDR_DQ23)	Connected to the SmartFusion2 pin AJ9 (DDRIO148NB5/ PROBE_B) in SOM Rev 3A.
55	DDRIO168NB5	Input/Output (2.5 V)		AK20 (DDRIO168NB5/ FDDR_DQ20)	
56	DDRIO173PB5	Input/Output (2.5 V)		AJ22 (DDRIO173PB5/ FDDR_DQS3)	
58	DDRIO173NB5	Input/Output (2.5 V)		AK22 (DDRIO173NB5/ FDDR_DQS3_N)	
60	DDRIO179NB5	Input/Output (2.5 V)		AJ24 (DDRIO179NB5/ FDDR_CAS_N)	
I²C (4 pins)					
25	I2C_1_SCL	Input/Output	SmartFusion2 MSS I2C1 bus serial clock input/output/ GPIO	V26 (MSIO11NB3/ CCC_NE1_I0/ **I2C_1_SCL**/ GPIO_1_A/ USB_DATA4_A)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
26	I2C_1_SDA	Input/Output	SmartFusion2 MSS I2C1 bus serial data input/output/ GPIO	V23 (MSIO11PB3/ CCC_NE0_I0/ **I2C_1_SDA**/ GPIO_0_A/ USB_DATA3_A)	
27	I2C_0_SDA	Input/Output	SmartFusion2 MSS I2C0 bus serial data input/output/ GPIO	K23 (MSIO48PB1/ **I2C_0_SDA**/ GPIO_30_B/ USB_DATA0_C)	
33	I2C_0_SCL	Input/Output	SmartFusion2 MSS I2C0 bus serial clock input/output/ GPIO	K24 (MSIO48NB1/ **I2C_0_SCL**/ GPIO_31_B/ USB_DATA1_C)	
SPI (12 pins)					
59	SPI_1_SDO	Output	SmartFusion2 MSS SPI1 serial data output/ GPIO	V27 (MSIO17PB3/ **SPI_1_SDO**/ GPIO_12_A)	
61	SPI_1_SDI	Input	SmartFusion2 MSS SPI1 serial data input/ GPIO	U27 (MSIO16NB3/ **SPI_1_SDI**/ GPIO_11_A)	
63	SC_SPI_DO	Output	SmartFusion2 MSS Golden Flash serial data output/ GPIO	Y29 (SC_SPI_DO)	
64	SPI1_nSS1	Input/Output	SmartFusion2 MSS SPI1 slave select 1/ GPIO	R29 (MSIO23NB3/ SPI_1_SS1/ GPIO_14_A)	
65	SC_SPI_DI	Input	SmartFusion2 MSS Golden Flash serial data input/ GPIO	Y28 (SC_SPI_SDI)	
66	SPI1_nSS2	Input/Output	SmartFusion2 MSS SPI1 slave select 2/ GPIO	R24 (MSIO24PB3/ SPI_1_SS2/ GPIO_15_A)	
68	SPI1_nSS3	Input/Output	SmartFusion2 MSS SPI1 slave select 3/ GPIO	R28 (MSIO24NB3/ SPI_1_SS3/ GPIO_16_A)	
67	SPI_1_CLK	Output	SmartFusion2 MSS SPI1 serial clock output/ GPIO	U23 (MSIO16PB3/ **SPI_1_CLK**)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
69	SPI1_nSS0	Output	SmartFusion2 MSS SPI1 slave select 0/ GPIO	V28 (MSIO17NB3/ **SPI_1_SS0**/ GPIO_13_A)	
70	FPGA_RPRG	Output	Control Golden Flash operation	G28 (FLASH_GOLDEN)	
71	SC_SPI_CLK	Output	SmartFusion2 MSS Golden Flash serial clock output/ GPIO	AA30 (SC_SPI_CLK)	
73	SC_SPI_nSS	Output	SmartFusion2 MSS Golden Flash slave select/ GPIO	W26 (SC_SPI_SS)	
Unconnected pins (4 pins)					
72, 74, 78, 80		N/A			

Table 3: SmartFusion2 SOM P1 Connector

The following table details the allocation of the external interface connectors pins on the P2 connector:

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
Power (3 pins)					
24, 28, 52	GND	Power	SOM ground	SmartFusion2 GND	
GPIO (53 pins)					
1	MSIO99PB8	Input/Output		H1 (MSIO99PB8)	
2	MSIO100NB8	Input/Output		G1 (MSIO100NB8)	
3	MSIO99NB8	Input/Output		H2 (MSIO99NB8)	
4	MSIO95PB8	Input/Output		G2 (MSIO95PB8)	
5	MSIO107PB8	Input/Output		M1 (MSIO107PB8)	
6	MSIO95NB8	Input/Output		G3 (MSIO95NB8)	
7	MSIO107NB8	Input/Output		M2 (MSIO107NB8)	
8	MSIO104NB8	Input/Output		L1 (MSIO104NB8)	
9	MSIO106PB8	Input/Output		M3 (MSIO106PB8)	
10	MSIO103PB8	Input/Output		L2 (MSIO103PB8)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
11	MSIO106NB8	Input/Output		M4 (MSIO106NB8)	
12	MSIO103NB8	Input/Output		L3 (MSIO103NB8)	
13	MSIO111PB8	Input/Output		N1 (MSIO111PB8)	
14	MSIO113NB8	Input/Output		L4 (MSIO113NB8)	
15	MSIO111NB8	Input/Output		N2 (MSIO111NB8)	
16	MSIO110NB8	Input/Output		N4 (MSIO110NB8)	
17	MSIO110PB8	Input/Output		N3 (MSIO110PB8)	
18	MSIO109NB8	Input/Output		N5 (MSIO109NB8)	
19	MSIO115PB8	Input/Output		P1 (**MSIO115PB8**/ GB2/ CCC_NW0_I1)	
20	MSIO100PB8	Input/Output		N6 (MSIO100PB8)	
21	MSIO115NB8	Input/Output		P2 (MSIO115NB8)	
22	MSIO96PB8	Input/Output		N7 (MSIO96PB8)	
23	MSIO114PB8	Input/Output		P3 (**MSIO114PB8**/ GB6/ CCC_NW1_I1)	
25	MSIO114NB8	Input/Output		P4 (MSIO114NB8)	
26	MSIO25PB2	Input/Output		P30 (MSIO25PB2/ **USB_XCLK_D**)	
27	MSIO112NB8	Input/Output		P5 (MSIO112NB8)	
29	MSIO105PB8	Input/Output		P6 (MSIO105PB8)	
30	MSIO30NB2	Input/Output		M28 (MSIO30NB2/ **USB_DATA7_D**/ GPIO_23_B)	
31	MSIO108PB8	Input/Output		P7 (MSIO108PB8)	
32	MSIO30PB2	Input/Output		N27 (MSIO30PB2/ **USB_DATA6_D**)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
33	MSIO112PB8	Input/Output		P8 (MSIO112PB8)	
34	MSIO29NB2	Input/Output		M30 (MSIO29NB2/ **USB_DATA5_D**)	
35	MSIOD118PB7 (MSIO101PB8 in SOM Rev 3A)	Input/Output		R3 (MSIOD118PB7/ GB5/ CCC_SW1_I1)	Connected to the SmartFusion2 pin N8 (MSIO101PB8) in SOM Rev 3A.
36	MSIO29PB2	Input/Output		N28 (MSIO29PB2/ **USB_DATA4_D**)	
37	MSIOD118NB7 MSIO108NB8 in SOM Rev 3A	Input/Output		R4 (MSIOD118NB7)	Connected to the SmartFusion2 pin F2 (MSIO108NB8) in SOM Rev 3A.
38	MSIO28NB2	Input/Output		N29 (MSIO28NB2/ **USB_DATA3_D**)	
39	MSIO116NB8	Input/Output		R5 (MSIO116NB8)	
40	MSIO28PB2	Input/Output		P25 (MSIO28PB2/ **USB_DATA2_D**)	
41	MSIO117NB8	Input/Output		R6 (MSIO117NB8)	
42	MSIO27NB2	Input/Output		P27 (MSIO27NB2/ **USB_DATA1_D**)	
43	MSIO109PB8	Input/Output		R7 (MSIO109PB8)	
44	MSIO27PB2	Input/Output		P26 (MSIO27PB2/ **USB_DATA0_D**)	
45	MSIO113PB8	Input/Output		R8 (MSIO113PB8)	
46	MSIO25NB2	Input/Output		P29 (MSIO25NB2/ **USB_DIR_D**)	Connected to the SmartFusion2 pin P28 in Rev 1A.
47	MSIOD120NB7 (MSIO98PB8 in SOM Rev 3A)	Input/Output		T1 (MSIOD120NB7)	J3 (MSIO98PB8) Connected to the SmartFusion2 pin in SOM Rev 3A.
48	MSIO26NB2	Input/Output		N30 (MSIO26NB2/ **USB_NXT_D**)	Connected to the SmartFusion2 pin P29 in Rev 1A.

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
49	MSIOD125NB7 (MSIO98NB8 in SOM Rev 3A)	Input/Output		T5 (MSIOD125NB7)	Connected to the SmartFusion2 pin J4 (MSIO98NB8) in SOM Rev 3A.
50	MSIO26PB2	Input/Output		P28 (MSIO26PB2/ **USB_STP_D**)	Connected to the SmartFusion2 pin P30 in Rev 1A.
51	MSIOD128PB7 (MSIO97NB8 in SOM Rev 3A)	Input/Output		T6 (MSIOD128PB7)	Connected to the SmartFusion2 pin K5 (MSIO97NB8) in SOM Rev 3A.
53	MSIOD124PB7 (MSIO117PB8 in SOM Rev 3A)	Input/Output		T8 (MSIOD124PB7)	Connected to the SmartFusion2 pin R9 (MSIO117PB8/ CCC_NW0_I0) in SOM Rev 3A.
54	MSIOD122NB7	Input/Output (2.5 V)		U1 (MSIOD122NB7)	
55	MSIOD122PB7 (MSIO104PB8 in SOM Rev 3A)	Input/Output		U2 (MSIOD122PB7)	Connected to the SmartFusion2 pin N9 (MSIO104PB8) in SOM Rev 3A.
56	MSIOD123NB7	Input/Output (2.5 V)		U3 (MSIOD123NB7)	
57	MSIOD123PB7 (MSIO116PB8 in SOM Rev 3A)	Input/Output		U4 (MSIOD123PB7)	Connected to the SmartFusion2 pin P9 (MSIO116PB8/ CCC_NW1_I0) in SOM Rev 3A.
58	MSIOD124NB7	Input/Output (2.5 V)		U5 (MSIOD124NB7)	
59	MSIOD136PB7 (MSIO15PB3 in SOM Rev 3A)	Input/Output		U6 (MSIOD136PB7)	Connected to the SmartFusion2 pin U24 (MSIO15PB3/ SPI_0_SS6/ GPIO_21_A) in SOM Rev 3A.
60	MSIOD121PB7	Input/Output (2.5 V)		U7 (MSIOD121PB7/ CCC_SW0_I0)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
61	MSIOD125PB7 (MSIO15NB3 in SOM Rev 3A)	Input/Output		U8 (MSIOD125PB)	Connected to the SmartFusion2 pin U26 (MSIO15NB3 SPI_0_SS7/ GPIO_22_A) in SOM Rev 3A.
62	MSIO33NB2	Input/Output		L29 (MSIO33NB2/ GPIO_2_B)	
63	MSIO37NB2	Input/Output		K29 (MSIO37NB2/ GPIO_10_B)	
64	MSIO33PB2	Input/Output		L30 (MSIO33PB2/ GPIO_1_B)	
65	MSIO37PB2	Input/Output		K30 (MSIO37PB2/ GPIO_9_B)	
66	MSIO32NB2	Input/Output		M27 (MSIO32NB2/ **GPIO_0_B**)	
67	MSIO43PB1	Input/Output		M24 (MSIO43PB1/ MMUART_0_RTS/ GPIO_17_B/ USB_DATA5_C)	
68	MSIO23PB3	Input/Output		R25 (MSIO23PB3/ SPI_0_SS3/ GPIO_10_A/ USB_DATA7_A)	
69	MSIO40PB1	Input/Output		M25 (MSIO40PB1/ CCC_NE1_I1/ MMUART_1_RI/ GPIO_15_B)	
70	MSIO22NB3	Input/Output		R30 (MSIO22NB3/ SPI_0_SS2/ GPIO_9_A/ USB_DATA6_A)	
71	MSIO36NB2	Input/Output		M26 (MSIO36NB2/ GPIO_8_B)	
72	MSIO35NB2	Input/Output		J27 (MSIO35NB2/ GPIO_6_B)	
73	MSIO47NB1	Input/Output		H26 (MSIO47NB1/ MMUART_0_CLK/ GPIO_29_B/ USB_NXT_C)	

Pin	Name	Type	Description	SmartFusion2 Pin	Notes
74	MSIO38NB1	Input/Output		J28 (MSIO38NB1/ MMUART_1_DTR/ GPIO_12_B)	
75	MSIO40NB1	Input/Output		H28 (MSIO40NB1/ MMUART_1_DCD/ GPIO_16_B)	
76	MSIO38PB1	Input/Output		J29 (MSIO38PB1/ MMUART_1_RTS/ GPIO_11_B)	
77	MSIO42PB1	Input/Output		H29 (MSIO42PB1/ GB14/VCCC_SE1/ MMUART_1_CLK/ GPIO_25_B/ USB_DATA4_C)	
78	MSIO41PB1	Input/Output		J30 (MSIO41PB1/ GB10/VCCC_SE0/ USB_XCLK_C)	
79	MSIO45NB1	Input/Output		F30 (MSIO45NB1/ MMUART_0_DCD/ GPIO_22_B)	
80	MSIO45PB1	Input/Output		G30 (MSIO45PB1/ MMUART_0_RI/ **GPIO_21_B**)	

Table 4: SmartFusion2 SOM P2 Connector

2.14.3. Unavailable Signals of SmartFusion2

The following signals of the SmartFusion2 device are not available on the interface connectors. These signals are unused and left unconnected on the SmartFusion2 SOM:

SmartFusion2 Pin	Name
D11	MDDR_DQ35_ECC
E11	MDDR_DQ34_ECC
B11	MDDR_DQ33_ECC
A11	MDDR_DQ32_ECC
A10	MDDR_DQS_ECC
B10	MDDR_DQS_ECC_N
D10	MDDR_DM_RQDS4_ECC

SmartFusion2 Pin	Name
J4 (in SOM Rev 1A and Rev 2A)	MSIO98NB8
J26	MSIO43NB1/MMUART_0_DTR
K3	MSIO101NB8
K5 (SOM Rev 1A and Rev 2A)	MSIO97NB8
K25	MSIO44NB1/MMUART_0_DSR
K28	MSIO34NB2/GPIO_4_B
L26	MSIO39NB1/MMUART_1_DSR

SmartFusion2 Pin	Name
D23	MDDR_DQ31
E23	MDDR_DQ30
B23	MDDR_DQ29
A23	MDDR_DQ28
E21	MDDR_DQ27
D21	MDDR_DQ26
B21	MDDR_DQ25
A21	MDDR_DQ24
B22	MDDR_DQS3
A22	MDDR_DQS3_N
D22	MDDR_DM_RQDS3
B20	MDDR_DQ23
E20	MDDR_DQ22
D20	MDDR_DQ21
A20	MDDR_DQ20
E18	MDDR_DQ19
D18	MDDR_DQ18
B18	MDDR_DQ17
A18	MDDR_DQ16
A19	MDDR_DQS2
B19	MDDR_DQS2_N
D19	MDDR_DM_RQDS2
B16	MDDR_DQS1_N
B13	MDDR_DQS0_N
A26	MDDR_BA2
C29	MDDR_ADDR15
D29	MDDR_ADDR14

SmartFusion2 Pin	Name
L28	MSIO34PB2/GPIO_3_B
M5	MSIO105NB8
M8	MSIO97PB8
M23	MSIO44PB1/MMUART_0_CTS
N8 (in SOM Rev 1A and Rev 2A)	MSIO101PB8
N9 (in SOM Rev 1A and Rev 2A)	MSIO104PB8
N23	MSIO39PB1/CCC_NE0_I1/ MMUART_1_CTS
N24	MSIO36PB2/GPIO_7_B
N25	MSIO35PB2/GPIO_5_B
N26	MSIO31NB2/GPIO_30_A
P9 (in SOM Rev 1A and Rev 2A)	MSIO116PB8/CCC_NW1_I0
P23	MSIO32PB2/GPIO_31_A
P24	MSIO31PB2/GPIO_29_A
R1	MSIOD119PB7/GB1/ CCC_SW0_I1
R2 (in SOM Rev 1A and Rev 3A)	MSIOD119NB7
R3 (in SOM Rev 3A)	MSIOD18PB7/GB5/CCC_SW1_I1
R4 (in SOM Rev 3A)	MSIOD118NB7
R9 (in SOM Rev 1A and Rev 2A)	MSIO117PB8/CCC_NW0_I0
T1 (in SOM Rev 3A)	MSIOD120NB7
T4	MSIOD121NB7
T5 (in SOM Rev 3A)	MSIOD125NB7
T6 (in SOM Rev 3A)	MSIOD128PB7
T7 (in SOM Rev 1A)	MSIOD120PB7/CCC_SW1_I0
T8 (in SOM Rev 3A)	MSIOD124PB7
T9	MSIOD133PB7
T24	MSIO20PB3/GB9/VCCC_SE0
T26	MSIO21PB3/GPIO_27_A

SmartFusion2 Pin	Name
E25	MDDR_ODT
A24	MDDR_RST_N
A9	DDRIO91PB0/GB0/CCC_NW0I3
AA3	MSIOD129NB7
AA4	MSIOD136NB7
AA5	MSIOD141NB7
AA26 (in SOM Rev 1A and Rev 2A)	MSIO2PB3/USB_STP_B
AA27	MSIO2NB3/USB_NXT_B
AA28 (in SOM Rev 1A and Rev 2A)	MSIO7NB3/CAN_TX
AA29	MSIO8NB3/CAN_TX_EN_N
AB4	MSIOD137NB7
AC2 (in SOM Rev 3A)	MSIOD138PB7
AB26	MSIO0NB3/USB_DATA7_B
AB29 (in SOM Rev 1A and Rev 2A)	MSIO6PB3/USB_DATA6_B
AB30 (in SOM Rev 1A and Rev 2A)	MSIO6NB3
AC28 (in SOM Rev 1A and Rev 2A)	MSIO1PB3/USB_XCLK_B
AC29 (in SOM Rev 1A and Rev 2A)	MSIO1NB3/USB_DIR_B
AC30 (in SOM Rev 1A and Rev 2A)	MSIO5NB3/USB_DATA5_B
AD12	DDRIO150PB5
AD30 (in SOM Rev 1A and Rev 2A)	MSIO5PB3/USB_DAT4_B
AE2	MSIOD144NB7
AE11	DDRIO147PB5
AE14	DDRIO158NB5
AE15	DDRIO162PB5

SmartFusion2 Pin	Name
T27	MSIO21NB3/GPIO_28_A
T28	MSIO20NB3/GB13/VCCC_SE1
T30	MSIO22PB3/SPI_0_SS1
U2 (in SOM Rev 3A)	MSIOD122PB7
U4 (in SOM Rev 3A)	MSIOD123PB7
U6 (in SOM Rev 3A)	MSIOD136PB7
U8 (in SOM Rev 3A)	MSIOD125PB7
U9	MSIOD132PB7
U24 (in SOM Rev 1A and Rev 2A)	MSIO15PB3/SPI_0_SS6
U25	MSIO19PB3/SPI_1_SS6
U26 (in SOM Rev 1A and Rev 2A)	MSIO15NB3/SPI_0_SS7
U30	MSIO19NB3/SPI_1_SS7
V2	MSIOD127NB7
V3	MSIOD126NB7
V4	MSIOD126PB7
V8	MSIOD140PB7
V24	MSIO8PB3/CAN_RX
V29	MSIO18PB3/SPI_1_SS4
V30 (in SOM Rev 1A and Rev 2A)	MSIO18NB3/SPI_1_SS5
W4	MSIOD132NB7
W5	MSIOD130NB7
W8	MSIOD137PB7
W23 (in SOM Rev 1A and Rev 2A)	MSIO7PB3
W24	MSIO3PB3

SmartFusion2 Pin	Name
AE18	DDRIO170NB5
AE21	DDRIO174PB5
AE23	DDRIO185NB5
AE24	DDRIO185PB5
AE27	DDRIO189PB5
AE29	DDRIO178NB5
AE30 (in SOM Rev 1A and Rev 2A)	MSIO4NB3/USB_DAT3_B
AF11	DDRIO152PB5/GB3/ CCC_SW0_I3
AF12	DDRIO154NB5
AF14	DDRIO157NB5
AF15	DDRIO160NB5
AF17	DDRIO164PB5/VCCC_SE1
AF18	DDRIO166NB5
AF20	DDRIO169NB5
AF21	DDRIO172NB5
AF23	DDRIO176PB5
AF24	DDRIO186NB5
AF25	DDRIO186PB5
AF27	DDRIO189NB5
AF29	DDRIO178PB5
AG9	DDRIO147NB5/CCC_SW0_I2
AG10	DDRIO150NB5
AG11	DDRIO152NB5/GB7/CCC_SW1_I 2
AG12	DDRIO154PB5
AG13	DDRIO156PB5
AG14	DDRIO157PB5
AG15	DDRIO160PB5/VCCC_SE0

SmartFusion2 Pin	Name
W25 (in SOM Rev 1A and Rev 2A)	MSIO4PB3
W29 (in SOM Rev 1A and Rev 2A)	MSIO14PB3/SPI_0_SS4
W30 (in SOM Rev 1A and Rev 2A)	MSIO14NB3/SPI_0_SS5
Y6	MSIOD142NB7
Y7	MSIOD142PB7
Y22 (in SOM Rev 1A and Rev 2A)	MSIO0PB3
Y25 (in SOM Rev 1A and Rev 2A)	MSIO3NB3
AB8	PCIE_0_RXDP0
AB9	PCIE_0_RXDN0
AC9	PCIE_0_RXDP1
AC10	PCIE_0_RXDN1
AB10	PCIE_0_RXDP2
AB11	PCIE_0_RXDN2
AD10	PCIE_0_RXDP3
AD11	PCIE_0_RXDN3
AA6	PCIE_0_REXTL
K6	PCIE_1_REXTL
J8	PCIE_1_RXDP0
J9	PCIE_1_RXDN0
H9	PCIE_1_RXDP1
H10	PCIE_1_RXDN1
J10	PCIE_1_RXDP2
J11	PCIE_1_RXDN2
G10	PCIE_1_RXDP3
G11	PCIE_1_RXDN3
V9	MSIOD145PB6/ PCIE_0_REFCLK0P
V10	MSIOD145NB6/ PCIE_0_REFCLK0N

SmartFusion2 Pin	Name
AG16	DDRIO162NB5
AG17	DDRIO164NB5
AG18	DDRIO166PB5
AG19	DDRIO168PB5
AG20	DDRIO169PB5
AG21	DDRIO172PB5
AG22	DDRIO174NB5
AG23	DDRIO176NB5
AG24	DDRIO181PB5
AG25	DDRIO181NB5
AG27	DDRIO187PB5
AG28	DDRIO187NB5
AG29	DDRIO190PB5
AG30	DDRIO177PB5
AH27	DDRIO183PB5
AH29	DDRIO190NB5
AH30	DDRIO177NB5
AJ17	DDRIO163NB5
AJ19 (in SOM Rev 3A)	DDRIO167NB5
AJ20 (in SOM Rev 3A)	DDRIO170PB5
AJ21	DDRIO171NB5
AJ23	DDRIO175NB5
AJ25	DDRIO180NB5
AJ26	DDRIO182NB5
AJ27	DDRIO183NB5
AJ28	DDRIO188NB5
AJ29	DDRIO188PB5
AK21	DDRIO171PB5
AK23	DDRIO175PB5

SmartFusion2 Pin	Name
AF1	MSIOD146PB6/ PCIE_0_REFCLK1P
AE1	MSIOD146NB6/ PCIE_0_REFCLK1N
E1	MSIOD94NB9/ PCIE_1_REFCLK0N
F1	MSIOD94PB9/ PCIE_1_REFCLK0P
L6	MSIOD93PB9/ PCIE_1_REFCLK1P
L7	MSIOD93NB9/ PCIE_1_REFCLK1N
AJ2	PCIE_0_TXDP0
AJ4	PCIE_0_TXDP1
AJ8	PCIE_0_TXDP3
AJ6	PCIE_0_TXDP2
AJ10 (in SOM Rev 3A)	DDRIO149NB5
AJ11 (in SOM Rev 3A)	DDRIO151NB5
AJ12 (in SOM Rev 3A)	DDRIO153NB5
AJ13 (in SOM Rev 3A)	DDRIO155NB5
AJ14 (in SOM Rev 3A)	DDRIO158PB5
AJ15 (in SOM Rev 3A)	DDRIO159NB5
AJ16 (in SOM Rev 3A)	DDRIO161NB5
AK2	PCIE_0_TXDN0
AK4	PCIE_0_TXDN1
AK6	PCIE_0_TXDN2
AK8	PCIE_0_TXDN3
AK10 (in SOM Rev 3A)	DDRIO149PB5
AK11 (in SOM Rev 3A)	DDRIO151PB5
AK12 (in SOM Rev 3A)	DDRIO153PB5
AK13 (in SOM Rev 3A)	DDRIO155PB5
AK14 (in SOM Rev 3A)	DDRIO156NB5
AK15 (in SOM Rev 3A)	DDRIO159PB5/CCC_SW1_I3
AK16 (in SOM Rev 3A)	DDRIO161PB5/GB11/VCCC_SE0
AK17 (in SOM Rev 3A)	DDRIO163PB5/GB15/VCCC_SE1

SmartFusion2 Pin	Name
AK24	DDRIO179PB5
AK25	DDRIO180PB5
AK26	DDRIO182PB5
AK27	DDRIO184PB5
AK28	DDRIO184NB5
B9	DDRIO91NB0/GB4/CCC_NW1_I2
D9	DDRIO92NB0/CCC-NW0_I2
F2 (in SOM Rev 1A and Rev 2A)	MSIO108NB8
H4	MSIO96NB8
J1 (in SOM Rev 1A and Rev 2A)	MSIO102PB8
J2 (in SOM Rev 1A and Rev 2A)	MSIO102NB8
J3 (in SOM Rev 1A and Rev 2A)	MSIO98PB8

SmartFusion2 Pin	Name
AA9	PCIE_0_REXTR
K9	PCIE_1_REXTR
B2	PCIE_1_TXDP0
A2	PCIE_1_TXDN0
B4	PCIE_1_TXDP1
A4	PCIE_1_TXDN1
B6	PCIE_1_TXDP2
A6	PCIE_1_TXDN2
B8	PCIE_1_TXDP3
A8	PCIE_1_TXDN3

Table 5: Unavailable Signals of SmartFusion2

3. Mechanical Specifications

3.1. SmartFusion2 SOM Mechanicals

The SmartFusion2 SOM is implemented as a miniature 34 x 59 x 4.8 mm module.

The SmartFusion2 SOM PCB thickness is 1.6+/- 0.16 mm. The maximum height of the SOM components is 1.6 mm.

The following figure shows the location of the SOM connectors on the module:

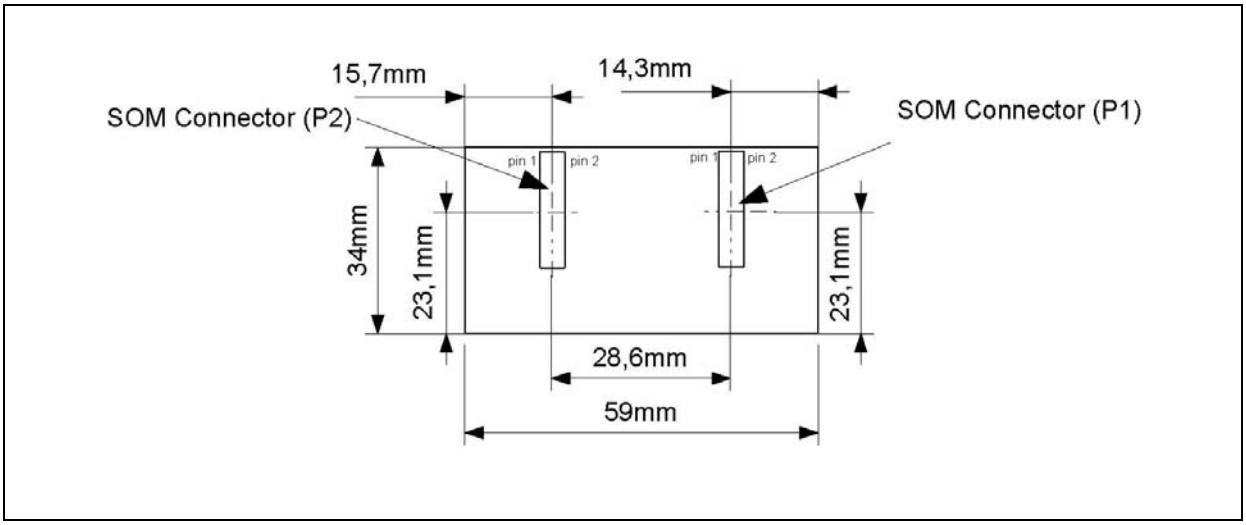

Figure 2: SmartFusion2 SOM Bottom View

3.2. SmartFusion2 SOM Connector Mechanicals

On a baseboard, the SmartFusion2 SOM is installed into two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors. The exact part number of the connectors is Hirose DF40C-80DP-0.4V(51).

The recommended mating connectors for a baseboard are the Hirose DF40HC(4.0)-80DS-0.4V connector, which provides 4 mm stacking height for the SmartFusion2 SOM. The maximum height of the SOM above a baseboard for 4 mm stacking height is 7.6 mm.

4. Revision History

4.1. Hardware Changes from Rev 1A to Rev 2A

Hardware Component(s)	Rev 1A Value	Rev 2A Value
JTAG		
TCK and nTSRT pull-down resistors (R39 and R40)	33 Ohm	1 k
Golden Flash SPI		
The SC_SPI_nSS pull-up (R38)	33 Ohm	1 k
Golden Flash SPI		
The FlLASH_GOLDEN pull resistor (R37)	pull-down	pull-up
SPI_0		
SPI0_DI	SPI0_DI_R is connected to Y30	SPI0_DI_R is connected to W27
SPI0_DO	SPI0_DO_R is connected to Y30	SPI0_DO_R is connected to W27
Part Corrections		
C34	0.01 µF	0.1 µF
C7, C8, C13, C14	4.7 µF	10.0 µF
DDR Voltage Reference		
R14/R16 (a DDR reference voltage divider)	1.2 V	1.8 V
Net and Pin Names		
Pin R3	MSIO18PB7	MSIOD18PB7/GB5/CCC_SW1_I1
ULPI		
P2 pin 46	Net MSIO26PB2	Net MSIO25NB2
P2 pin 48	Net MSIO25NB2	Net MSIO26NB2
P2 pin 50	Net MSIO26NB2	Net MSIO26PB2

Hardware Component(s)	Rev 1A Value	Rev 2A Value
R1	33 Ohm	wire
P2 pin 24	Net MSIO101PB8	GND
P2 pin 28	Net MSIOD119NB7	GND
P2 pin 52	Net MSIOD120PB7	GND
Ethernet PHY		
D1	BAT54ALI1	Removed
R32	270 Ohm	Removed
R33	10 k	Removed
C1	4.7 µF	Removed
U3 pin 32	Net nRSI_PHY	Net nRESET_OUT
P2		
Pin 15	Net nRESET	Net nRESET_OUT
U1		
Pin R2	Net MSIOD119NB7	Net nRESET_OUT
Pin N8	Net MSIO101PB8	Unconnected
Pin T7	Net MSIOD120PB7	Unconnected
1.2 DC-DC		
R22	DNI	Removed
R46	-	0 Ohm
TP1, TP2	-	Test points

5. Document Revision History

Revision	Date	Changes Summary
1.1	February 6, 2013	• Allocation of SF2 signals updated to provide DDRIO148PB5/PROBE_A and DDRIO148NB5/PROBE_B on the SOM connectors and on the breadboard area of SOM-BSB-EXT. • Added detailed definition for the multi-function SF2 signals.
1.0	February 1, 2013	Initial version.