THE INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS

IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	12.1
Revision	Subject
A	PLCC (Square)

1.0 SCOPE

This subsection provides the component and land pattern dimensions for plastic leaded chip carriers, square (PLCC components) with J leads on four sides. Basic construction of the PLCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, "Plastic Chip Carrier (PLCC) Family, 1.27 mm [0.050 in] Lead Spacing, Square," Outline MO-047, issue "B," dated 11/88

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C or 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages.

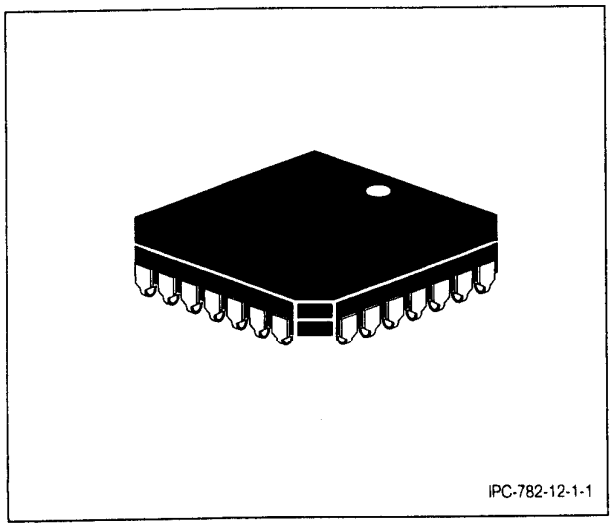


Figure 1 PLCC (Square)

3.1.1 Pre-molded Plastic Chip Carriers The pre-molded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

3.1.2 Post-molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the pre-molded package which has an aperture for mounting microelectronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages which have J-lead configuration and are JEDC standard MO-047, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

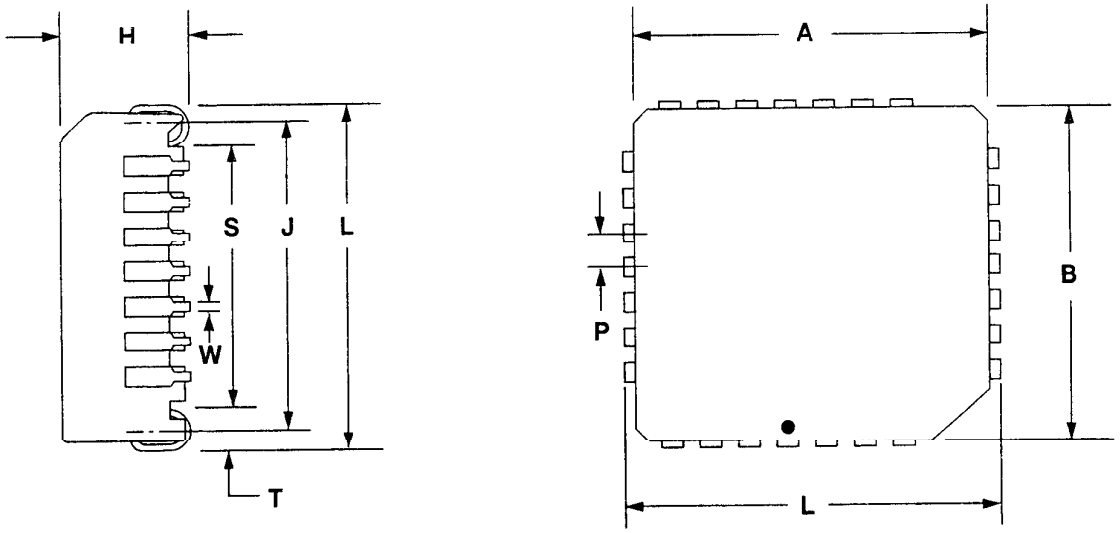
3.1.3 Marking All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body.

3.1.4 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.5 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PLCC (Square) components.



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Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		J (mm)	H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	ref	max	basic
PLCC-20	9.78	10.03	5.78	6.53	0.33	0.53	1.50	2.00	8.89	9.04	8.89	9.04	7.87	4.57	1.27
PLCC-28	12.32	12.57	8.32	9.07	0.33	0.53	1.50	2.00	11.43	11.58	11.43	11.58	10.41	4.57	1.27
PLCC-44	17.40	17.65	13.40	14.15	0.33	0.53	1.50	2.00	16.51	16.66	16.51	16.66	15.49	4.57	1.27
PLCC-52	19.94	20.19	15.94	16.69	0.33	0.53	1.50	2.00	19.05	19.20	19.05	19.20	18.03	5.08	1.27
PLCC-68	25.02	25.27	21.02	21.77	0.33	0.53	1.50	2.00	24.13	24.33	24.13	24.33	23.11	5.08	1.27
PLCC-84	30.10	30.35	26.10	26.85	0.33	0.53	1.50	2.00	29.21	29.41	29.21	29.41	28.19	5.08	1.27
PLCC-100	35.18	35.43	31.18	31.93	0.33	0.53	1.50	2.00	34.29	34.49	34.29	34.49	33.27	5.08	1.27
PLCC-124	42.80	43.05	38.80	39.55	0.33	0.53	1.50	2.00	41.91	42.11	41.91	42.11	40.89	5.08	1.27

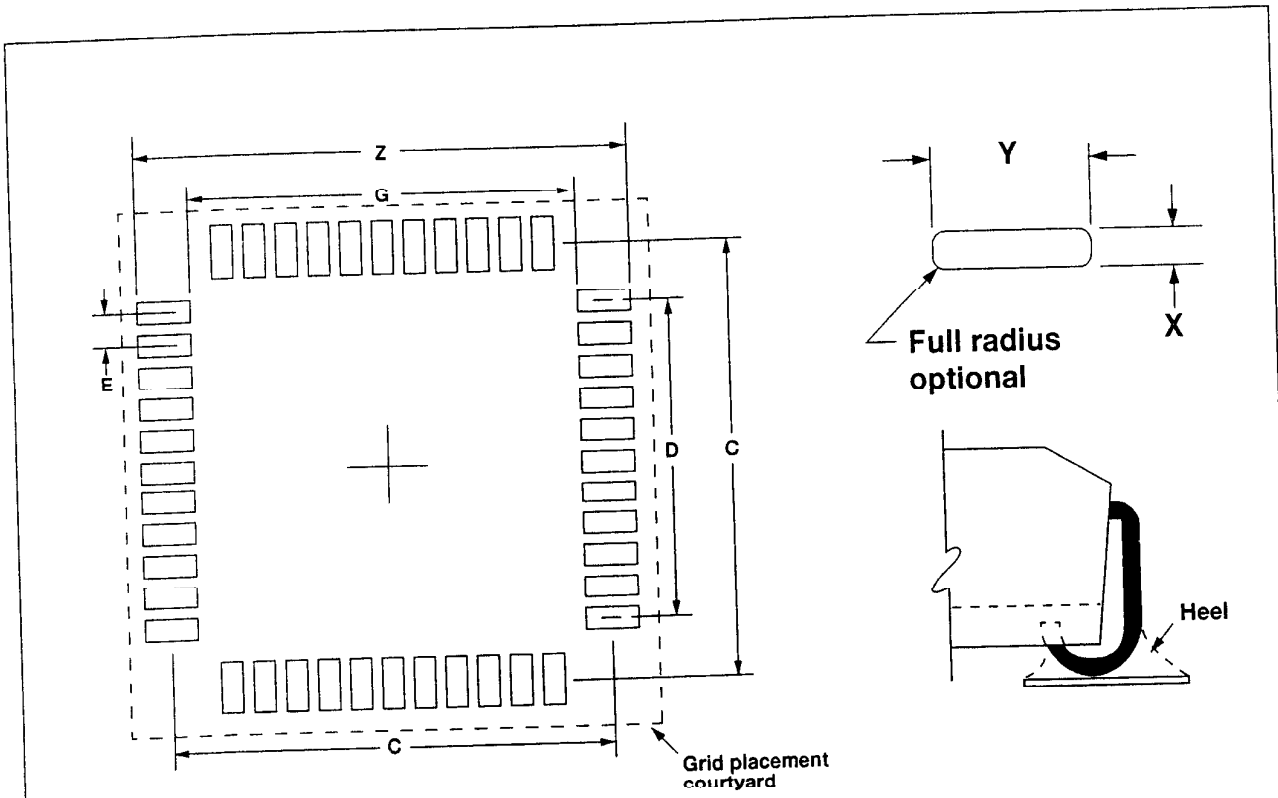
Figure 2 PLCC (Square)

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PLCC (Square) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
790A	PLCC-20	10.80	6.40	0.60	2.20	8.60	5.08	1.27	24x24
791A	PLCC-28	13.40	9.00	0.60	2.20	11.20	7.62	1.27	30x30
792A	PLCC-44	18.40	14.00	0.60	2.20	16.20	12.70	1.27	40x40
793A	PLCC-52	21.00	16.60	0.60	2.20	18.80	15.24	1.27	44x44
794A	PLCC-68	26.00	21.60	0.60	2.20	23.80	20.32	1.27	54x54
795A	PLCC-84	31.20	26.80	0.60	2.20	29.00	25.40	1.27	66x66
796A	PLCC-100	36.20	31.80	0.60	2.20	34.00	30.48	1.27	76x76
797A	PLCC-124	43.80	39.40	0.60	2.20	41.60	38.10	1.27	90x90

Figure 3 PLCC (Square) land pattern dimensions

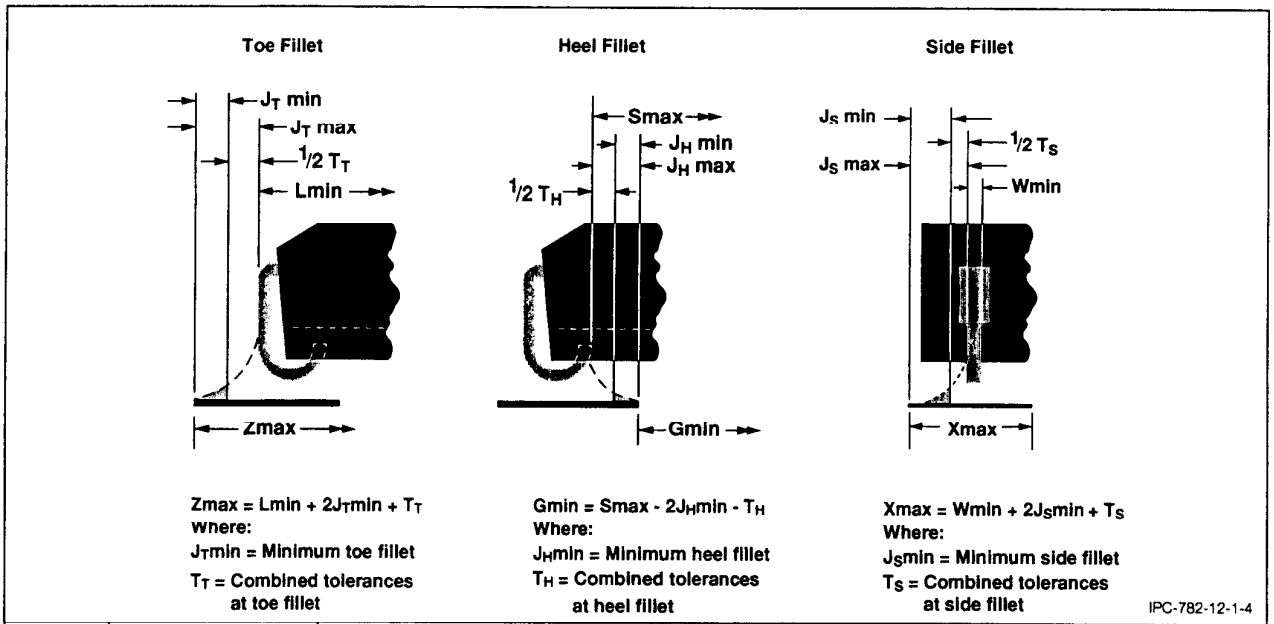
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication ("F") and component placement equipment accuracy ("P") are assumed to be asgiven in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint								
			Heel (mm)			Toe (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_H$min	$J_H$max	C_S	$J_T$min	$J_T$max	C_W	$J_S$min	$J_S$max
790A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
791A	0.10	0.10	0.25	0.40	0.54	0.75	-0.35	0.04	0.20	0.01	0.14
792A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14
793A	0.10	0.10	0.25	0.39	0.53	0.75	-0.34	0.04	0.20	0.01	0.14
794A	0.10	0.10	0.25	0.35	0.49	0.75	-0.30	0.08	0.20	0.01	0.14
795A	0.10	0.10	0.25	0.41	0.55	0.75	-0.36	0.03	0.20	0.01	0.14
796A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
797A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14

Figure 4 Tolerance and solder joint analysis