Actel® Libero™ IDE v2.3 Release Notes

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About this Release

Thank you for upgrading to the Actel Libero Integrated Design Environment (IDE) v2.3. These release notes outline new features and benefits, new device support, known limitations, and other information about this release. Updates are posted on our website, http://www.actel.com/custsup/updates/libero/Libero23rl.html.

Supported Platforms

Libero IDE is available for the PC only. Supported platforms include:

- WinNT 4.0 SP5 & SP6
- Win2000 SP1 and SP2
- Win98, 2nd Edition (except APA750 and APA1000)
- WinXP

Minimum System Requirements

- 300-MHz Pentium processor or greater
- 128 MB RAM
- FAT32 or NTF (NTFS file system STRONGLY recommended)
- 600 MB available hard disk space minimum, 1 GB for full install of Libero IDE and all libraries
- 100 MB free space in C: drive for installation file swapping is recommended
- 5 MB available hard disk space for each VITAL/VHDL device family simulation library
- 5 MB available hard disk space for each Verilog device family simulation library
- CD-ROM drive
- HTML browser
- 800x600 video resolution

Minimum RAM Requirements

The table below contains the minimum and Actel recommended RAM requirements your computer needs to program these Actel devices.

Device	Minimum RAM	Recommended RAM
APA750[a]	500 MB	750 MB
APA1000[a]	750 MB	1 GB
AX500	128 MB	256 MB
AX1000	256 MB	384 MB
AX2000	512 MB	750 MB

a. APA750 and APA1000 devices are not supported on the Windows 98 platform. This is due to memory management limitation with Windows 98AX

Installation Instructions

Installation and Licensing Instructions are included with the software.

You must have a license that matches your software version in order to run Designer vR1-2003 (included w/ Libero v2.3). If you do not have a license to run software v.4.6 or above, your software will not work. Please update your license at http://register.actel.com/RegSerial.asp.

Included Software

Actel Software

- Libero IDE v2.3
- Designer R1-2003
- Silicon Explorer 5.0

OEM Software

- ViewDraw™ for Actel 7.7
- Synplicity® - Synplify® v7.2
- SynaptiCAD™ - WaveFormer Lite™ 8.9
- MentorGraphics® - Model*Sim*™ for Actel 5.6B

New Features and Enhancements

Libero IDE v2.3 features several new tool/project ease of use enhancements, log window and error manager improvements, and a more efficient and comprehensive Help system that immediately puts you in touch with more subjects, applications notes, data sheets, and other useful information.

The detailed list of enhancements and features of Libero IDE v2.3 can be viewed at http://www.actel.com/custsup/updates/libero/index.html. Please check this website for v2.3 update and other information on Libero IDE.

Refer to Libero IDE v2.3 Online Help and the *Libero IDE User's Guide* for specific details on the operations of these new features.

OEM Software

WaveFormer Lite 8.9 from SynaptiCAD

A new version of WaveFormer Lite is included with the Libero IDE v2.3 release.

ModelSim for Actel 5.6B from ModelSim

A new version of Model*Sim* is included with the Libero IDE v2.3 release.

Synplify v7.2 from Synplicity

A new version of Synplify is included with the Libero IDE v2.3 release. Enhancements include:

- Improved ProASIC^{PLUS} performance. Up to 33% improvement is possible, depending on the specific device and design implementation.Some designs may not achieve the same performance as v7.1.
- 17388 & 17642 - RT54SX72S and 32S are now included in the 54SXA family in the Synplify GUI.

Libero IDE Project Manager

22988 - Hierarchical Testbench: A new Select Stimulus Dialog box enables you to view all stimulus files within a project and select hierarchy testbench files into a desired compilation order for simulation.

22986 - OEM Tools Dialog: A new Tool Options Dialog box enables you to specify the location of an OEM tool (i.e. Synplify, ModelSim, WaveFormer Lite). Separate tabs are available for Synthesis, Stimulus, and Simulation. The dialog boxes contain browse and Additional Parameter windows for reference.

Display Project Path: The full path of the project file is now shown in the title bar of the Libero Project Manager.

Display of File Name in Design Hierarchy window: In the Design Hierarchy, the corresponding file name and file type is now displayed next to the block.

Display of Block Properties: A new Block Properties dialog box displays file path, date created, and date of the last modification to the file. To display this dialog box, right- click the Block in the Design Hierarch window and select Block Properties.

Delete File from Disk and Project: A new "Delete from Disk and Project" command is available. In the File Manager, right-click the file and select Delete from Project and Disk.

22626 - Synplify Project File Name: Since the extension *.prj is used by both Libero and Synplify, a Synplify project file that is created in the Libero hdl_sub_folder will be named <root>_syn.prj by Libero, where "<root>" is the name of the block currently set as root.

Importing a File from the File Manager window: Within the File Manager window, right-clicking a file type opens a drop down menu that enables you to import files of the same file type selected.

Online Help: Libero v2.3 and Designer R1-2003 now support HTML Help. The Help content has been reorganized and greatly enhanced. Some of the key features are:

- One integrated online help system covering all software tools within Libero and Designer.
- Instant access to support. Help is available for error messages, specific screens, and menus.
- Expanded content, over 350 topics.
- Extends online help from the desktop to the web. Hyperlinks to Application Notes and actel.com web pages help you quickly find more information.

Access to PDF documents from within Libero: From the Help menu, you can now access all reference manuals shipped with Libero IDE.

Online Access to Technical Support from within Libero: From the Help menu, you can now access all Actel's Online Tech Support web.

Log Window and Error Manager:

- Filtering: Tabs allow you to now see all messages, or just error, warning, or informational messages. The Output window is displays all messages; the Warning window displays only messages that are categorized by Libero IDE as warnings; the Errors window displays only messages that are categorized by Libero IDE as errors; and the Info window displays messages that have been categorized as information only.
- Colors and Symbols: Colors and symbols are used to differentiate between errors, warnings, and informational messages. A Log Window Preferences

Manager allows you to select unique colors for informational, error, warning, and hyperlink text. Messages show up in a color coded style in the Output window.

- Some errors are linked to online help, where you can find more information and workarounds.

Detect Outside Changes in the HDL Editor: If a file that is open in the Libero HDL editor is modified by another text editor, Libero IDE displays the warning "The <file> file was modified by another application" in the Libero Project Manager.

Comment Blocks in the HDL Editor: The new Comment command lets you comment out selected text within the active file opened in the Libero HDL editor. Single line comments ("-" for VHDL, "//" for Verilog) are added at the beginning of each selected line. The Uncomment command lets you remove single line comments from the selected text.

Designer Software

Timer

Timer now supports skew analysis for ProASIC, ProASIC^{PLUS}, and Axcelerator Families.

Violation report now include hold-time checking for ProASIC, ProASIC^{PLUS}, and Axcelerator Families.

Skew is now included into analysis of the clock frequency.

The expanded path window now includes additional skew information for violation analysis.

Timer grays out data that has been outdated by user constraints.

Constraints violations are now flagged on the summary tab.

In the summary and clock tab, the path that is the source of the clock can now be expanded.

For designs with data feeding back in from a BIBUF I/O, Timer now takes the feedback path into account for the reg-reg frequency calculation. This new feature may cause existing designs to show a different reg-reg frequency since this path was previously ignored. To obtain the reg-reg frequency without taking this path into account, either break the path at the enable pin of the BIBUF or set the path through the BIBUF as an exception.

APS

The APS programming software for the discontinued Activator 2 programmers is no longer installed.

SmartPower

SmartPower now supports ProASIC and ProASIC^{PLUS}.

The following modifications can be saved into the design database:

- Modification of a set of pins or a clock domain. These modifications result from removing a pin from the domain or adding a new pin into the domain.
- Modification of frequency values of a domain
- Modification of activity (annotation) of pins
- Deletion of an existing set of pins or a clock domain
- Creation of a new set of pins or a clock domain
- Clock domains, Set-of-Pins, and annotated pins can now be included in the SmartPower text report.

Extended Layout Scripts

The R1-2003 release includes enhanced, extended layout scripts. These Tcl scripts force the layout to run with an extended set of parameters and enable you to optimize for a specific clock. These scripts cause an increase in layout runtime in an attempt to improve performance and routability.

The two scripts available are described below:

Iterate.tcl

This script runs from the GUI and assumes that the design has completed the Compile stage successfully. To execute the script:

1. **From the *File* menu, click *Execute Script*.**
2. **Browse to the "scripts" directory within your Designer installation directory**
3. **Select "iterate.tcl".** This script runs five iterations of the extended parameter layout. To change the number of iterations, add a "-n" and the number of iterations you wish the layout to attempt in the argument box. The maximum value for iterations is 26.

- To specify which a clock to optimize for, add a "-c" and the name of the clock you wish the layout to optimize.

4. **Click Run.**

sh_iterate.tcl

This script is the command line version of the iterate.tcl script and is recommended for UNIX users. This script also requires that the design has been successfully compiled.

Run this script from the acttclsh shell located in the "bin" directory (in your Actel designer installation directory). This script is located in the "script" directory of the Actel installation.

This script runs five iterations of the extended parameter layout. In order change the number of iterations, add a "-n" and the number of iterations you wish the layout to attempt.

To specify which a clock to optimize for, add a "-c" and the name of the clock you wish the layout to optimize.

Netlist Viewer

Netlist Viewer now allows you to switch between pre-optimized and post-optimized design netlists for Axcelerator family.

Page navigation icons have been added to the toolbar. These enable you to move across display pages.

FlashLock

The FlashLock Permanent Lock feature is now enabled for the ProASIC^{PLUS} family.

Simulation

The ProASIC, ProASIC^{PLUS}, and Axcelerator RAM simulation models in Vital and Verilog have been updated to allow pre-loading of memory content for simulation. Please refer to the *Preloading of RAM Models in Simulation* application note.

Log Window

The new Log Window allows you to quickly differentiate between different types of messages, filter for messages, and get more details about particular errors. The new Log Window features include:

- Filtering: Tabs allow you to now see all messages, or just error, warning, or informational messages. The Output window is displays all messages; the Warning window displays only messages that are categorized by Designer as warnings; the Errors window displays only messages that are categorized as errors; and the Info window displays messages that have been categorized as information only.

  Error and warning messages do not appear in the error or warnings tabs for ProASIC and ProASIC^{PLUS} designs. These messages are displayed in the output log tab.

- Colors and Symbols: Colors and symbols are used to differentiate between errors, warnings, and informational messages. A Log Window Preferences Manager allows you to select unique colors for informational, error, warning, and hyperlink text.

- Online Help: Some errors are linked to online help, where you can find more information and workarounds.

Online Help

R1-2003 now supports HTML Help. The Help content has been reorganized and greatly enhanced. Some of the key features are:

- Help for both the UNIX and PC platforms
- One integrated online help system covering all software tools within Libero and Designer.
- Instant access to support. Help is available for error messages, specific screens, and menus.
- Expanded content
- Extends online help from the desktop to the web. Hyperlinks to Application Notes and actel.com web pages help you quickly find more information.

Resolved Issues

19483 - WaveFormer Lite 8.3f Output Signals

Output signals are not grayed out in the WaveFormer Lite window. If any waveform is added to any output, the output signal turns blue. This does not affect the test bench generation.

This problem is resolved in WaveFormer Lite 8.9. Outputs are grayed out in the waveform display whereas inputs are not grayed out. Users can not draw waveforms on outputs.

21578 - Synplify 7.1A Cannot Find Reference Clock

During synthesis of mixed flow designs, you might get errors similar to the one below:

"tacstrt.c:1887 Error: Cannot find reference clock\$1I1284.q2_inferred_clock".

This problem is fixed in Synplify 7.2.

20349 - Synplify 7.1A Compiling with Verilog v1995 and v2000

Libero IDE at this time supports Verilog 1995 and does not support Verilog 2001. In Synplify 7.1a, the default Verilog mode is 2001 and this caused incompatibilities in the Libero design flow. When in Libero, invoking Synplify defaults to Verilog 1995.

Synpify 7.2 when started outside of Libero still defaults to Verilog 2001. In this mode, it is possible to change Synplify 7.2 to use Verilog 1995. To do this, start Synplify outside of Libero. From the Synplify main menu, in Options, select Configure Verilog, and uncheck the V2001 option.

Libero IDE HDL Errors

When there are syntax errors in HDL files, Libero IDE cannot find the top level module/entity and generates an error message, "there may be syntax errors in your HDL files". In Libero v2.3, a note in the message file reports "Unable to recognize top level module in the design. Use Syntax Checker to check your HDL code."

19483 - WaveFormer Lite 8.3f Output Signals

Output signals are not grayed out in the WaveFormer Lite window. If any waveform is added to any output, the output signal turns blue. This does not affect the test bench generation.

This problem is resolved in WaveFormer Lite 8.9. Outputs are grayed out in the waveform display whereas inputs are not grayed out. Users can not draw waveforms on outputs.

22759 - Using ACTgen for Axcelerator Designs

·A problem with Axcelerator Fast Counter flags being reversed has been corrected.

22764 - Using ACTgen for ProASIC^{PLUS} Designs

ACTgen PLLs now function properly in simulation.An error in the output of ACTgen generated FIFO's has been corrected.

22480 - Using ACTgen for SX-A Designs

An issue with the almost full and almost empty flags being reversed resolved for SX-A FIFOs has been corrected.

Known Issues and Workarounds

For complete information about all known issues and workarounds, go to http:

Project Manager/ Design Flow

- 23890 - Libero/Designer Timing, SDF Writer/Timing Library update
- 23753 - Refresh Command with ViewDraw Open
- 23828 - Cannot close ViewDraw with Libero IDE open
- 22993 - Compile VHDL Package Files on by default
- 21913 - Designer audits original directory after move of Project the file using File->Audit Settings.
- 15199 & 22750 - Mixed Flow: Internal array to net conversion inconsistent. Bus Renaming
- 23584 - Design hierarchy display problems with package files
- 23836 - Changing your Top Level Schematic after Synthesis causes simulation problems
- 23823 - Use of ACTgen within Libero (behavioral and structural HDL files)
- 23670 - “Undo” of Comment Out command
- 23913 & 23696 - Pre-loading Memory Arrays for Simulation
- 21888 - File import After Synthesis or Place and Route of Schematic Designs

- 23830 - Cannot push into lower level schematics from top level schematics.

Designer Software

ACTgen

22958 - Attempting to generate FIR-Filters with a width of 16 bits and 64 tabs may cause ACTgen to exit prematurely.

23018 - When specified from a GEN file, FIR filters always have the default value for DataMaxFo and clock frequency regardless of what was specified in the GEN file.

23280 - The accumulator for ProASIC^{PLUS} includes an ACLR pin which has an INOUT property even if no ACLR is selected for the accumulator.

23980 - For an async FIFO, if the empty flag goes low and RDB receives a rising edge (read-shift-register enabled), the read-shift-register advances by 1.

22845 - Register Files generated by ACTgen for SX-A have a port direction of INOUT for the Rclock pin.

22990 - FIR filters for the SX-A family should be generated only from the "Basic Options" Tab.

16038 - Axcelerator CRC Macros must have a width that is a power of 2. Attempting to generate a macro with a width that is not a power of 2 causes ACTgen to return an error, though it still generates a netlist. Do not use the generated netlist. (16038)

24055 - Axcelerator FIFOs created by ACTgen with flags must have Write Enable (WE) and Read Enable (RE). The "none" selection for the WE and RE signals are not legal for FIFOs with flags.

Compile

·23481 - Compile fails if the net and the port in the netlist have the same name.

22420 - Register combining for Axcelerator must be set before the compile stage.

24238 - Existing AX500-FG484 databases with pins that are no longer available in the device, (as described in the device support section above), may cause the Designer software to abort prematurely.

Extended Layout

23509 - The extended layout script runs only in Timing Driven Mode for NON- ProASIC, ProASIC^{PLUS}, and Axcelerator families.

Reporting

23414 - Warning messages from SmartPower are only reported in the Output tab.

23326 - Error and warning messages do not appear in the error or warnings tabs for ProASIC and ProASIC^{PLUS} designs.

23492 - In the expanded Timer window, selecting the grid and clicking Edit -> Copy does not properly copy the entire grid.

FlashLock

23531 - While the FlashLock GUI allows for a security key of 66 characters for all ProASIC^{PLUS} devices, only the largest ProASIC^{PLUS} device allows 66 characters.

PinEdit

24460 - Do not assign a regular I/O macro to a PECL pad position.

SmartPower

23869 - SmartPower GUI does not refresh properly.

23866 - SmartPower cannot accept a negative value for the ambient temperature.

24211 - For the ProASIC and ProASIC^{PLUS} devices, if any changes are made to the capacitance loading in PinEdit, you must close and re-open the design for the changes to be reflected in SmartPower.

Timer

Axcelerator

23922 - On “Register to Output” and “Input to Output” paths, Timer reports a delay that is over 1ns pessimistic.

SX-A/SX-S

23378 - For the A54SX72A and RT54SX72S, the Timer shows three entries for each QCLKBUF used. Timer shows the internal nodes of the QCLK tree as clocks labeled “QCLKBUF_inst:D” and “QCLKBUF_inst:E”.

Simulation

Model Technologies ModelSIM

23906 - Updates to the Vital libraries now require that the entity be compiled before the architecture.

24137 - The CLK2 output of the ProASIC^{PLUS} PLL does not produce an output in simulation. The CLK1 output of the PLL simulates normally. The simulation for both clock outputs simulate correctly in the Cadence NCSIM and the Model Technology ModelSIM.

PLLs for ProASIC^{PLUS}

24462 - The GL (located adjacent to GLMX), GLMX and regular I/O pins may not drive the PLL in real silicon. You can prevent this problem if you do not have fixed pin assignments and use the GL pin adjacent to the PECL pad to drive the PLL.

Online Help

Error and Warning messages for the ProASIC and ProASIC^{PLUS} families appear only in the output tab.

ModelSim

- 20807 - Simulation Cannot Proceed if clock_stop_time= xe+00x ns

WaveFormer Lite

- 23852 - Undesired Deleting of signal

ViewDraw

- 15972 - Windows association for .v and .vhd extensions
- 22363 - Bus Naming in ViewDraw
- 15737 - Save, Save + Check Command in ViewDraw
- 16923 - Use of Inverted Names in ViewDraw

Synplify

- 22815 - Flattening of Netlist in Synplify

Documentation

Libero IDE includes printed and online manuals. The manuals are available from the Libero Start Menu and on the CD-ROM.

From the Start menu choose:

- Programs > Libero 2.3 > Libero 2.3 Documentation

From the CD, insert your CD-ROM and click *Documentation* from the main screen, or look on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you install the Libero software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

Libero IDE comes with online help. Online help specific to each Actel software tool is available for Designer, ChipEdit, PinEdit, and the Libero integrated tool suite- ViewDraw, Model*Sim*, Synplify, and WaveFormer Lite.

The Libero online help is available from the Start menu and the Libero Help menu.

From the Start menu:

- Programs > Libero 2.3 > Libero Help

From Libero:

- Help > Libero Topics