Using JTAG Boundary-Scan with ProASIC™ 500K Devices

Introduction

Due to the increasing complexity of circuit boards, testing loaded boards is becoming prohibitively expensive and more difficult to perform. Board complexity has resulted from the rapid development of surface-mount technology and from the use of multi-layered boards. Finer pin spacing, high pin counts, and the use of double-sided mounted boards have also contributed to the increased cost and difficulty of traditional testing. This motivated the creation of the Joint Test Action Group (JTAG) which developed and proposed the JTAG boundary-scan method and was later adopted by IEEE as the "IEEE Standard Test Access Port and Boundary-Scan Architecture", also referred to as IEEE Std. 1149.1.

The IEEE standard defines the hardware architecture and mechanisms for cost-effective methods of board level testing using the boundary-scan technique. Actel's ProASIC family of FPGAs is compliant with the IEEE Standard 1149.1. This application note describes the various aspects of JTAG boundary-scan as it is implemented in the ProASIC FPGAs.

Note that all references in this application note to "JTAG" and "boundary-scan" indicate the JTAG boundary-scan method described by IEEE Std. 1149.1.

JTAG Boundary-Scan Test Logic Circuit

Figure 1 illustrates the components that make up the basic ProASIC JTAG boundary-scan test logic circuit. It is composed of the Test Access Port (TAP), TAP Controller, Test Data Registers, and Instruction Register. The JTAG boundary-scan test logic circuit supports all the mandatory JTAG instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instructions. In addition, the circuit also supports private instructions that are used for device programming and factory level testing.

Test Access Port

Each test logic function is accessed through the Test Access Port (TAP). There are five pins associated with the TAP: Test Clock Input (TCK), Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), and Test Reset Input (TRST) (Table 1, "Test Access Port," on page 2). TMS, TDI, and TRST are all equipped with a pull-up resistor to guarantee the proper operation of the JTAG circuitry when no inputs are applied on these ports. In ASICmaster's Design Options window (V5p2 or later), the user can select from various boundary-scan pin usage options. Table 2, "JTAG Boundary-Scan Design

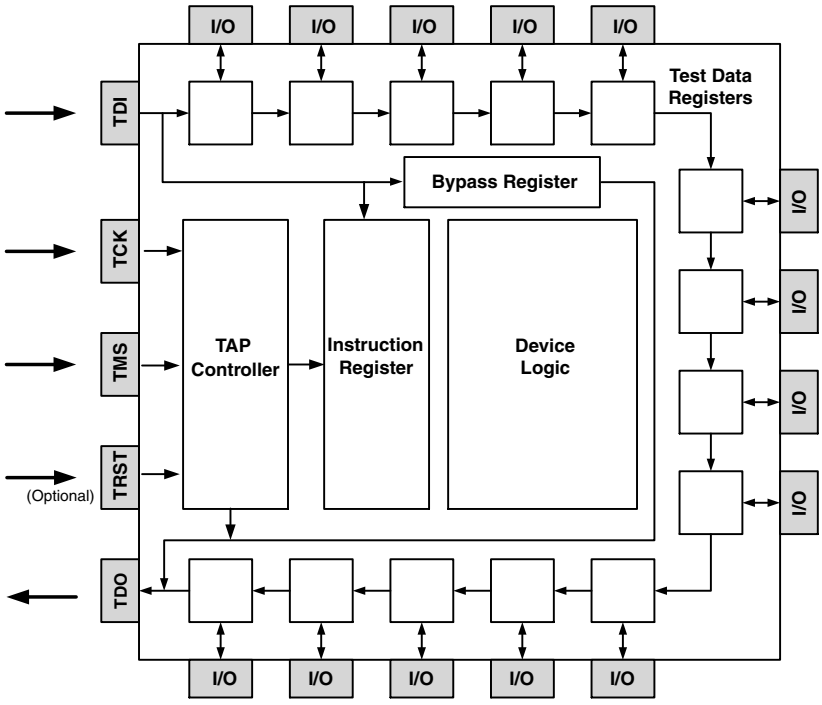

Figure 1 • ProASIC JTAG Boundary Scan Test Logic Circuit

Options," on page 2 shows the three options available in the Design Options window and their corresponding descriptions. By default, the "Extended JTAG pins" option is selected. The TDI, TDO, TMS, TCK, and TRST pins are restricted for JTAG boundary-scan purposes. In comparison, the "Use JTAG pins" option reserves TDI, TDO, TMS, and TCK. ASICmaster treats these pins as regular I/Os when the "No JTAG pins" option is selected. This means that these pins are equally likely to be used as any other user I/O to achieve the best possible layout. Additionally, in this mode, the JTAG boundary-scan circuitry is disabled.

Because the JTAG ports are equipped with a pull-up resistor, they may be left floating when not used.

Configuration of the JTAG Boundary-Scan Port

The JTAG port is configured based on the V_{DDP} voltage, as shown in Table 3. When V_{DDP} is equal to 2.5V, the JTAG port is configured using the 2.5V I/O buffers. The JTAG input pins (TDI, TMS, TCK, and TRST) use the ProASIC I/O buffer, IB25LPU, and the TDO pin is configured as a bi--directional buffer, IOB25LPLLU. Similarly, when V_{DDP} is equal to 3.3V, the JTAG port is configured using the 3.3V I/O buffers, where the JTAG inputs are configured as an IB33U and the TDO pin is configured as an IOB33LLU.

Because the JTAG circuitry is also utilized for programming, the JTAG port is automatically configured when the device is biased for programming. This is accomplished by placing V_{DDL} at 0.0V and V_{DDP} at 2.5V.

Table 1 • *Test Access Port*

Pin	Description
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. TCK's maximum clock frequency is 10 MHz.
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock. This pin is equipped with a pull-up resistor to place the test logic in the Reset state when no input is present.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. This pin is equipped with a pull-up resistor.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. This pin is equipped with a pull-up resistor. TDO drives out valid data on the falling edge of TCK.
TRST (Test Reset Input)	An asynchronous active low reset used to initialize the TAP controller. This optional pin is equipped with a pull-up resistor.

Table 2 • *JTAG Boundary-Scan Design Options*

JTAG Usage	Description
No JTAG Pins	JTAG pins are used as user I/Os.
Use JTAG Pins	Restricts the TDI, TDO, TMS, and TCK pins for JTAG usage.
Extended JTAG Pins	Restricts the TDI, TDO, TMS, TCK, and TRST pins for JTAG usage.

Table 3 • *JTAG Port Configuration*

JTAG Pins	Normal Operation (V_{DDP} = 2.5V)	Normal Operation (V_{DDP} = 3.3V)	Programming (V_{DDP} = 2.5V)
TCK	IB25LPU[1]	IB33U[2]	IB25LPU
TDI	IB25LPU	IB33U	IB25LPU
TMS	IB25LPU	IB33U	IB25LPU
TDO	IOB25LPLLU[3]	IOB33LLU[4]	IOB25LPLNU
TRST	IB25LPU	IB33U	N/A

Notes:

1. *IB25LPU is a 2.5V CMOS level input buffer, low power, with pull-up resistor.*
2. *IB33U is a 3.3V LVCMOS level input buffer, with pull-up resistor.*
3. *IOB25LPLLU is 2.5V CMOS level bi-directional buffer, low power, low drive strength, low slew rate, with pull-up resistor.*
4. *IOB33LLU is 3.3V LVCMOS level bi-directional buffer, low drive strength, low slew rate, with pull-up resistor.*

TAP Timing Specification

Figure 2 shows the timing waveform of the JTAG boundary-scan interface and Table 4 lists the timing values of all the parameters shown in the timing waveform. The specified values in the table must be met to ensure proper operation of the JTAG circuitry. As shown in the timing diagram, changes on TMS and TDI are clocked on the rising edge of TCK. Test data inputs entering the test logic through the user I/Os are also clocked by TCK on the rising edge.

Data from the instruction or data registers are shifted out of TDO on the falling edge of TCK. Test data driven out of the user I/Os are also clocked on the falling edge of TCK.

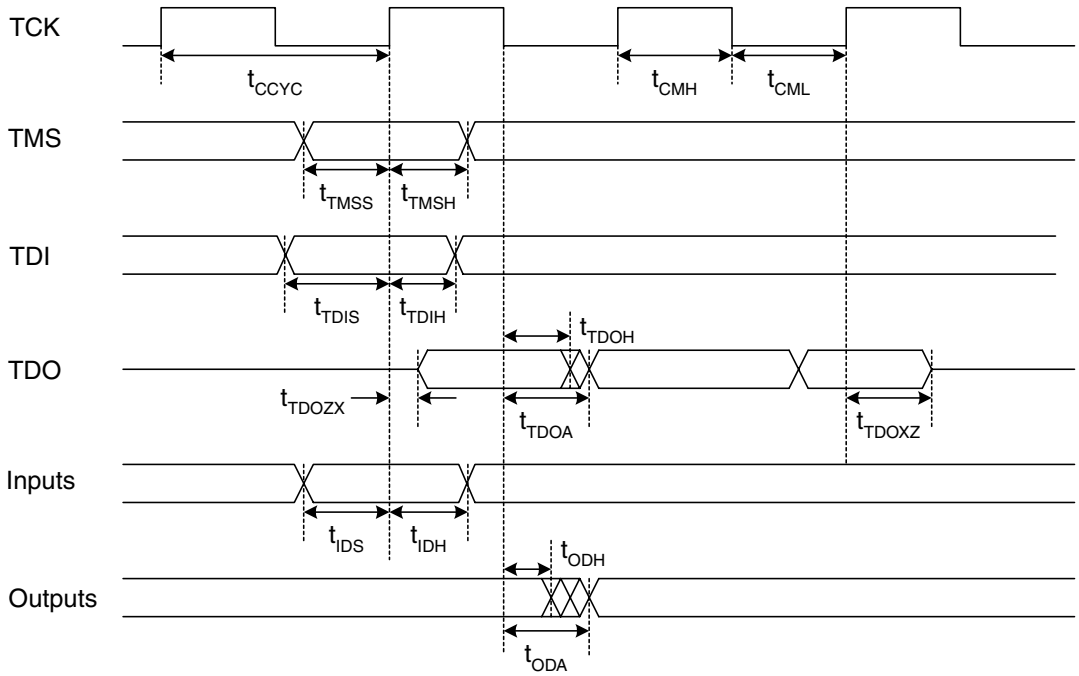

Figure 2 • *Timing Waveform for the JTAG Boundary-Scan Interface*

Table 4 • *Timing Values for the JTAG Boundary-Scan Signals*

Symbol	Description	Min (ns)	Max (ns)	Comment
t_{CCYC}	TCK Clock Cycle Time	100		
t_{CMH}	TCK Clock Cycle Minimum High Phase	40		
t_{CML}	TCK Clock Cycle Minimum Low Phase	40		
t_{TMSS}	TMS to TCK Setup Time		5	
t_{TMSH}	TMS from TCK Hold Time	0		
t_{TDIS}	TDI to TCK Setup Time		5	
t_{TDIH}	TDI from TCK Hold Time	0		
t_{TDOZX}	TDO High Impedance to Valid Delay		15	Load dependent
t_{TDOH}	TDO Old Data Hold Delay	1		Load dependent
t_{TDOA}	TDO New Data Valid Delay		15	
t_{TDOXZ}	TDO Valid to High Impedance Delay		15	
t_{IDS}	Input Signals to TCK Setup Time		5	
t_{IDH}	Input Signals from TCK Hold Time		15	
t_{ODH}	Output Signals Old Data Hold Delay	1		Extest Instruction
t_{ODA}	Output Signals New Data Valid Delay		35	Extest Instruction

TAP Controller

The TAP controller is a 4-bit state machine that operates according to the state diagram shown in Figure 3.

The 1's and 0's shown adjacent to the state transitions represent the TMS values that must be present at a rising edge of TCK, in order for the given state transition to occur. In the states that include the letters "IR", the instruction register is operating. In the states that contain the letters "DR", the test data register is operating (bypass, boundary-scan, and ID registers).

The TAP controller receives two control inputs, TMS and TCK, and generates control and clock signals for the rest of the test logic architecture. The TAP controller's state changes based on the value of TMS at the rising edge of TCK, or on power-up. On power-up, the TAP controller enters the TEST-Logic Reset State. Because the TMS pin is equipped with a pull-up resistor, the TAP controller will remain in, or return to, the Test-Logic-Reset State when there is no input or when a logical 1 is on the TMS pin. To guarantee a reset of the controller from any of the possible states, TMS must be high for five TCK cycles. The optional TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Test Data Registers

ProASIC 500K devices support three types of test data registers, bypass, boundary-scan, and device identification. The test circuitry is shown in Figure 4 on page 5.

Bypass Register

This register is selected when no other test data register needs to be accessed in a device during a board-level test operation. The bypass register is used to speed up test data transfer through a particular device to other devices in a daisy-chained board-level test data path.

Device Identification Register

The device identification register (ID-register) is a 32-bit shift register composed of four fields, as shown in Figure 5 on page 5. The first field is the mandatory least significant bit that is equal to 1. The second field (bits 1–12) is ProASIC's identification number. This number is defined as 00011100111. The third field (bits 13–27) is the part number. Table 5, "Part Number," on page 5 shows the 16-bit part number for ProASIC 500K devices. The fourth field (bits 28–31) is the version identifier. Figure 6 on page 5 shows an example ID-register for an A500K130 device. This example illustrates version number 1. The IDCODE instruction is used to read the contents of the ID-register. The IDCODE instruction is further discussed in the "IDCODE Instruction" section on page 8.

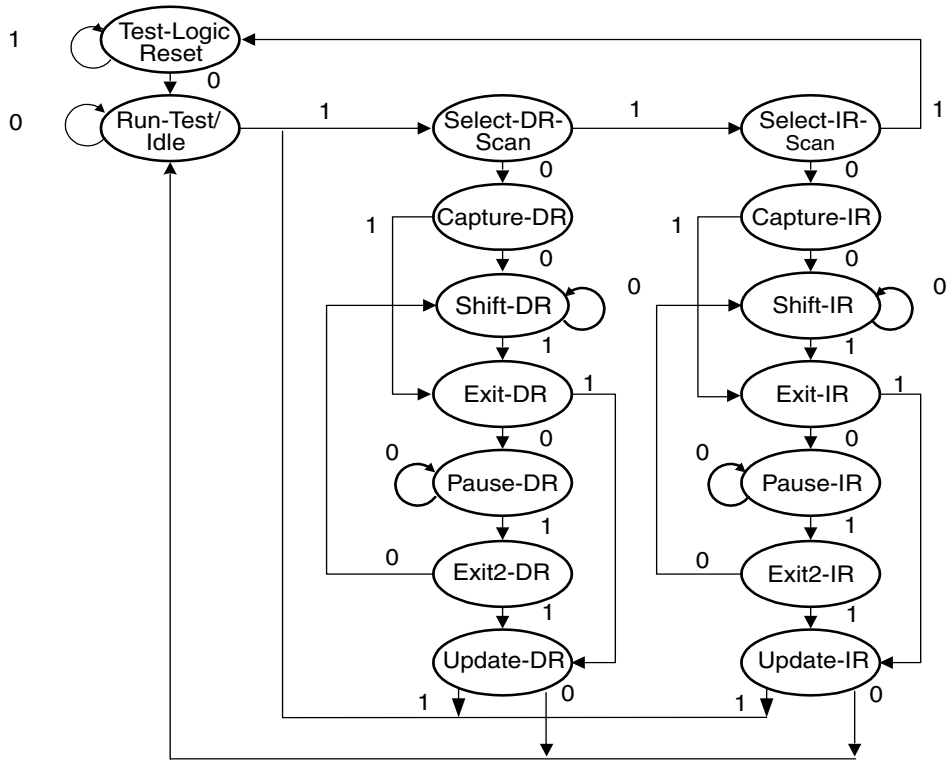

Figure 3 • *TAP Controller State Diagram*

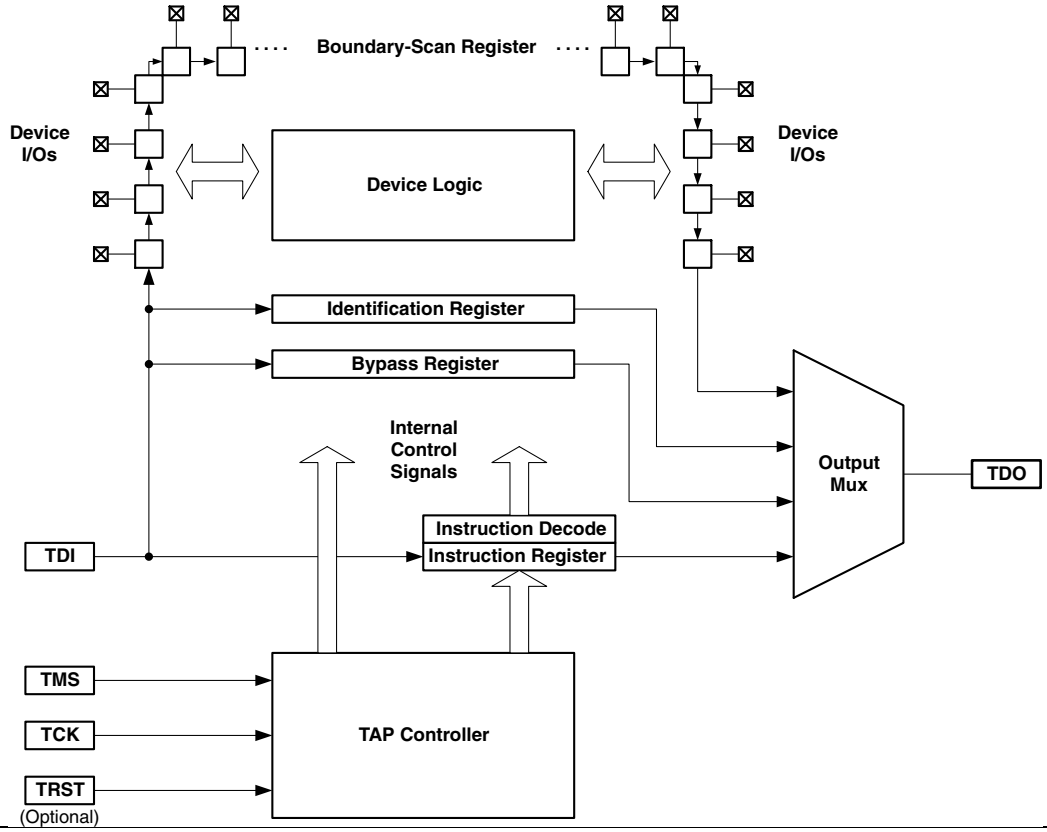

Figure 4 • *JTAG Boundary-Scan Test Circuitry*

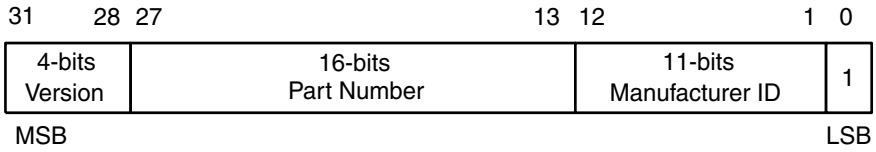

Figure 5 • *The Generic Device Identification Register*

Table 5 • *Part Number*

Device	Part Number (Hexadecimal)
A500K050	01A7
A500K130	02CA
A500K180	034C
A500K270	03CF

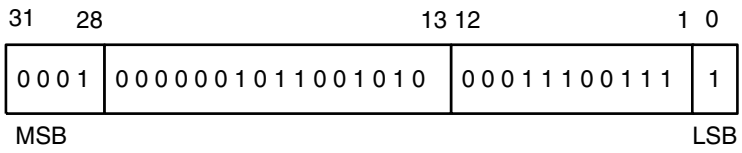

Figure 6 • *Example Identification Register for an A500K130 Device*

Boundary-Scan Register

The boundary-scan register is used to observe and control the state of each I/O pin. Use of the boundary-scan register allows testing of on-chip system logic, as well as circuitry external to a device.

Each I/O cell of the ProASIC device has three boundary-scan register cells, as shown in Figure 7. The actual implementation of the boundary-scan register cell is shown in Figure 8. Each register cell has four ports, serial input (SI), serial output (SO), parallel in (PI), and parallel out (PO). The SI and SO ports of each cell are used to serially connect all of the boundary-scan registers cells in the device forming a long boundary-scan register chain. The boundary-scan chain starts from the TDI pin and ends at the TDO pin. Test data is transferred in and out of the boundary-scan chain via the TDI and TDO ports. The PI and PO ports on each boundary-scan register cell are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer. Data from the core tiles or I/O can be captured and loaded into the register cell to control or observe the logic state of each I/O.

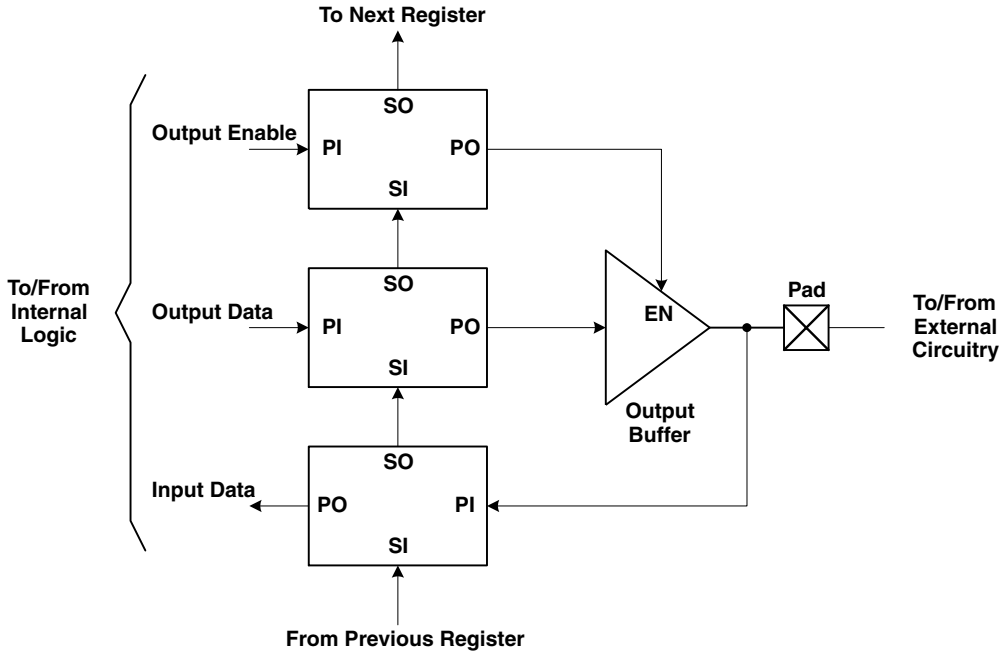

Figure 7 • *Boundary-Scan Setup for all I/Os*

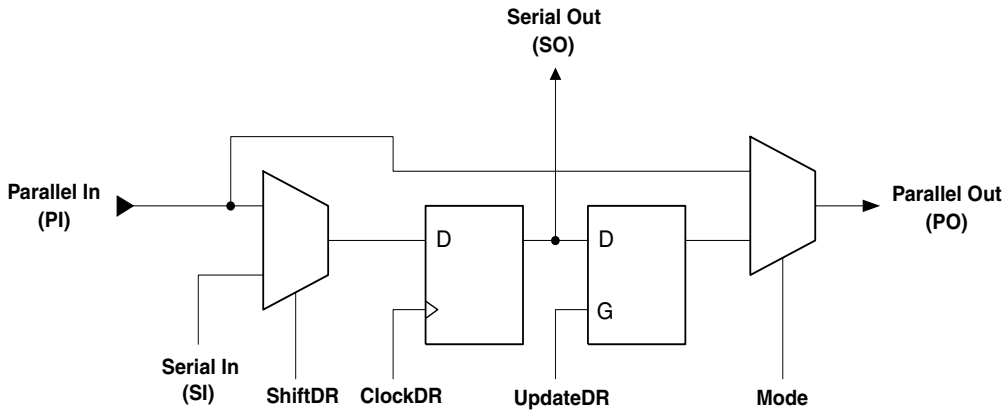

Figure 8 • *Boundary-Scan Cell Implementation*

Because ProASIC dies are assembled in various packages (PQFP, PBGA, etc.), some of the I/O buffers are not bonded to a package pin. These I/O buffers are treated as unused I/Os and are configured by the software as inputs with a pull-up resistor. The inputs from the die to the boundary-scan cells of these I/Os are connected to ground (GND), as shown in Figure 9.

Similar to the regular I/O buffer, the global buffers are designed with three boundary-scan cells, as shown in Figure 10. Because the ProASIC global buffers can only be configured as inputs, the parallel input of the top and bottom boundary-scan cells are tied to ground and the parallel outputs are left unconnected.

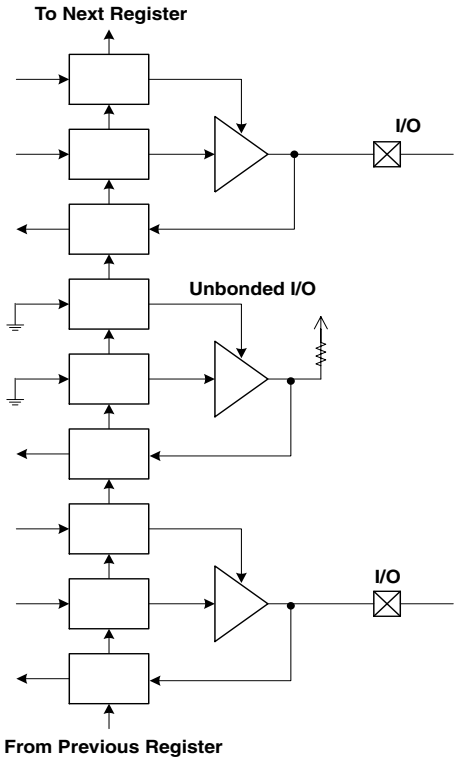

Figure 9 • *Boundary-Scan Register of an Unbonded I/O Buffer.*

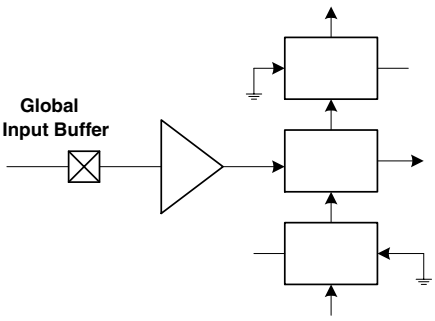

Figure 10 • *Boundary-Scan Register of Global Input Buffer*

Instruction Register

The instruction register of the ProASIC 500K devices is 8 bits wide, allowing the JTAG controller to support a large number of instructions. The following mandatory JTAG instructions are supported:

- **EXTEST (Binary op-code: 00000000)**
- **SAMPLE/PRELOAD (Binary op-code: 00000001)**
- **BYPASS (Binary op-code: 11111111)**

In addition to these mandatory instructions the optional IDCODE instruction is supported:

- **IDCODE (Binary op-code: 00001111)**

All other instructions are private. These private instructions are used for programming the device and conducting internal tests. These instructions should not be used for boundary-scan activities during normal operation.

SAMPLE/PRELOAD Instruction

This instruction as defined by the IEEE 1149.1 standard has two functions, SAMPLE and PRELOAD. During this instruction, the boundary-scan register is connected between TDI and TDO.

SAMPLE loads a snapshot of the running system into the boundary-scan register. This means the boundary-scan cells capture data from the input pins or data coming from the on-chip logic. The sample is taken during the “Capture-DR” state of the TAP controller. After capturing the sample, it can be shifted out for analysis by putting the TAP controller into the “Shift-DR” state.

PRELOAD latches the data loaded into the Boundary-Scan register turning the sample shift instruction into the Parallel Output Registers. This operation does not switch the Boundary-Scan cell output to the Parallel Output register. The on-chip logic is still driven by the outside signals and the on-chip logic still drives the outputs. The PRELOAD instruction gets executed in the “Update-DR” state of the TAP controller.

EXTEST Instruction

This instruction allows the user to both sample and drive external data onto device pins. During this instruction, the Boundary-Scan register is selected between TDI and TDO. The external data on the input signals is captured in the “Capture-DR” state of the TAP controller and on the rising edge of the TCK signal. The captured data can then be shifted out and be replaced with the next test pattern for the outputs of the device. The data shifted into the Boundary-Scan register will be switched onto the outputs of the Boundary-Scan cells during the “Update-DR” state of the TAP controller.

Note: *Since loading incorrect values into the Boundary-Scan register can potentially destroy a device, the user is advised to take special care when selecting the values used with this instruction.*

Normally the EXTEST instruction is preceded by the SAMPLE/PRELOAD instruction to bring the tested system into a known state. This prevents potential damage to the tested system.

BYPASS Instruction

This instruction puts the device into bypass mode. This results in only one flip-flop being connected between the TDI and TDO pins. This instruction is used within JTAG daisy chains of devices. If just one device is to be tested all other devices can be put into BYPASS mode, reducing the length of the scan data.

IDCODE Instruction

Actel has implemented the IDCODE instruction for the ProASIC 500K devices. This instruction places the IDCODE register between TDI and TDO to be read. The IDCODE register is 32 bits wide and gives the user information about the device family. See the "Device Identification Register" section on page 4 for a detailed description of the IDCODE contents.

JTAG Boundary-Scan Interconnect Topology

The JTAG standard does not have a specific configuration for multiple JTAG devices. The TAP input and output connections may be interconnected at the board level appropriate to the assembled product. The most common method is shown in Figure 11.

In this configuration, the TCK and TMS signals are broadcast to all devices. The TDO of one device links to the TDI of the next device. This configuration requires the least amount of interface signals from external tester.

Figure 12 shows another possible way to connect multiple JTAG compliant devices. The TCK and TMS signals are still shared by all devices, while each device has independent TDI and TDO signals.

Testing for this configuration is faster than the daisy-chain configuration, because all devices can be tested simultaneously. However, more interface signals are required.

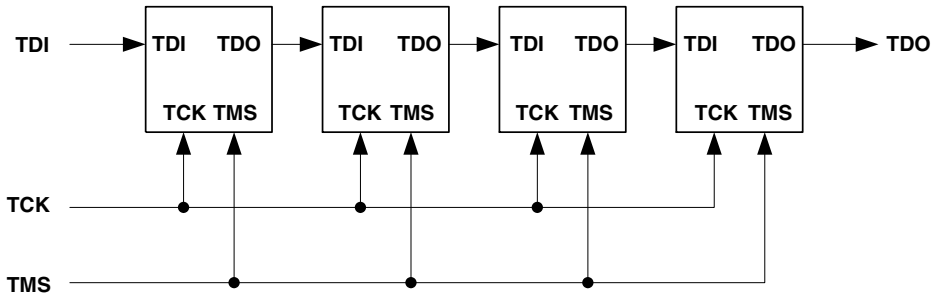

Figure 11 • *Interconnect Topology Example 1*

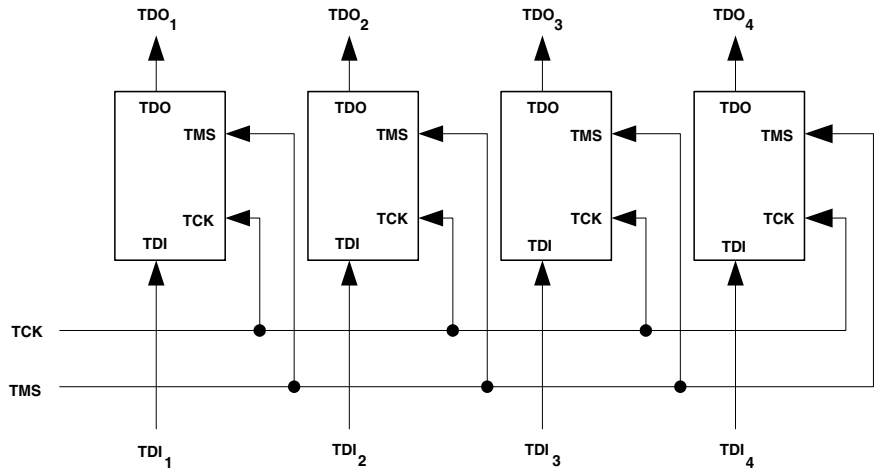

Figure 12 • *Interconnect Topology Example 2*

Boundary-Scan Description Language (BSDL) File

Conformance to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. BSDL files provide the standard format to describe the JTAG components, which can be used by the automatic test equipment software.

BSDL files for the ProASIC 500K devices are generated from the ASICmaster software. Refer to the *ASICmaster User's Guide* for information about generating BSDL files from ASICmaster.

A sample BSDL file generated from ASICmaster is shown on page 9. Refer to the IEEE specification "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" for additional information about BSDL files. The file includes instructions that are supported, the instruction bit pattern, and the boundary-scan register chain order.

Sample BSDL file

```
--
-- Boundary-Scan Description for
arcmega_1.dtf generated by gfreport V5p1.1
--
entity A500K130BG456 is

   generic(PHYSICAL_PIN_MAP: string :=
"BG456");

-- enumerate all pins ...

 port (S_162 : inout bit;
       S_161 : inout bit;
       S_160 : inout bit;
       S_159 : inout bit;
       S_158 : inout bit;
       S_157 : inout bit;
       S_156 : inout bit;
       S_151 : inout bit;
       S_150 : inout bit;
       S_149 : inout bit;
       S_148 : inout bit;
       S_147 : inout bit;
       .
       .
       .

       E_2 : inout bit;
       E_1 : inout bit;
       TDO : out bit;
       TMS, TDI, TCK : in bit);

use STD_1149_1_1994.all;

attribute COMPONENT_CONFORMANCE of
A500K130BG456 : entity is "STD_1149_1_1993";

attribute PIN_MAP of A500K130BG456 : entity is
PHYSICAL_PIN_MAP;

constant BG456: PIN_MAP_STRING:=
      "TDO:AC22,"&
      "TMS:AC21,"&
      "TDI:AF23,"&
      "TCK:AD21,"&
      "S_162:AA23,"&
      "S_161:AD25,"&
      "S_160:AC25,"&
      "S_159:AB23,"&
      .
      .
      .
      "E_7:Y24,"&
      "E_6:AA25,"&
      "E_5:Y23,"&
      "E_4:AA24,"&
      "E_3:AB25,"&
      "E_2:AB26,"&
      "E_1:AB24";

attribute TAP_SCAN_IN    of TDI   : signal is
true;
attribute TAP_SCAN_MODE  of TMS   : signal is
true;
attribute TAP_SCAN_OUT   of TDO   : signal is
true;
attribute TAP_SCAN_CLOCK of TCK   : signal is
(10.0e6, BOTH);

attribute INSTRUCTION_LENGTH of A500K130BG456
: entity is 8;

attribute INSTRUCTION_OPCODE of A500K130BG456
: entity is
    "BYPASS (11111111)," &
    "IDCODE (00001111)," &
    "EXTEST (00000000)," &
    "SAMPLE (00000001)";

attribute INSTRUCTION_CAPTURE of
A500K130BG456 : entity is "XXXXXX01";

attribute IDCODE_REGISTER of A500K130BG456 :
entity is
    "00000000001011001010000111001111";

attribute REGISTER_ACCESS of A500K130BG456 :
entity is
     "BOUNDARY (SAMPLE,EXTEST),BYPASS (BY-
PASS), DEVICE_ID (IDCODE)";

attribute BOUNDARY_LENGTH of A500K130BG456 :
entity is 1476;

attribute BOUNDARY_REGISTER of A500K130BG456
: entity is

-- Package Pin AA23 Scan Cell 0
"     0 (BC_1, S_162, output3, X, 1, 1, Z)," &
"     1 (BC_1, *, control, 1)," &
"     2 (BC_1, S_162, input, X)," &
-- Package Pin AD25 Scan Cell 1
"     3 (BC_1, S_161, output3, X, 4, 1, Z)," &
"     4 (BC_1, *, control, 1)," &
"     5 (BC_1, S_161, input, X)," &
-- Package Pin AC25 Scan Cell 2
"     6 (BC_1, S_160, output3, X, 7, 1, Z)," &
"     7 (BC_1, *, control, 1)," &
"     8 (BC_1, S_160, input, X)," &
```

```
-- Package Pin AB23 Scan Cell 3
"    9 (BC_1, S_159, output3, X, 10, 1, Z)," &
"     10 (BC_1, *, control, 1)," &
"     11 (BC_1, S_159, input, X)," &
-- Package Pin AC24 Scan Cell 4
"    12 (BC_1, S_158, output3, X, 13, 1, Z),"
&
"     13 (BC_1, *, control, 1)," &
"     14 (BC_1, S_158, input, X)," &
-- Package Pin AD23 Scan Cell 5
"    15 (BC_1, S_157, output3, X, 16, 1, Z),"
&
"     16 (BC_1, *, control, 1)," &
"     17 (BC_1, S_157, input, X)," &
-- Package Pin AE24 Scan Cell 6
"    18 (BC_1, S_156, output3, X, 19, 1, Z),"
&
"     19 (BC_1, *, control, 1)," &
"     20 (BC_1, S_156, input, X)," &
-- Package Pin Not Bonded Scan Cell 7
"     21 (BC_1, *, control, 1)," &
"     22 (BC_1, *, control, 1)," &
"     23 (BC_1, *, control, 1)," &
-- Package Pin Not Bonded Scan Cell 8
"     24 (BC_1, *, control, 1)," &
"     25 (BC_1, *, control, 1)," &
"     26 (BC_1, *, control, 1)," &
-- Package Pin Not Bonded Scan Cell 9
"     27 (BC_1, *, control, 1)," &
"     28 (BC_1, *, control, 1)," &
"     29 (BC_1, *, control, 1)," &
-- Package Pin Not Bonded Scan Cell 10
"     30 (BC_1, *, control, 1)," &
"     31 (BC_1, *, control, 1)," &
"     32 (BC_1, *, control, 1)," &
-- Package Pin AE22 Scan Cell 11
"    33 (BC_1, S_151, output3, X, 34, 1, Z),"
&
"     34 (BC_1, *, control, 1)," &
"     35 (BC_1, S_151, input, X)," &
.
.
.
-- Package Pin AB26 Scan Cell 489
"     1467 (BC_1, E_2, output3, X, 1468, 1,
Z)," &
"     1468 (BC_1, *, control, 1)," &
"     1469 (BC_1, E_2, input, X)," &
-- Package Pin AB24 Scan Cell 490
"     1470 (BC_1, E_1, output3, X, 1471, 1,
Z)," &
"     1471 (BC_1, *, control, 1)," &
"     1472 (BC_1, E_1, input, X)," &
-- Package Pin Not Bonded Scan Cell 491
"     1473 (BC_1, *, control, 1)," &
"     1474 (BC_1, *, control, 1)," &
"     1475 (BC_1, *, control, 1)";


end A500K130BG456;
```

http://www.actel.com

Actel Europe Ltd.
Daneshill House, Lutyens Close
Basingstoke, Hampshire RG24 8AG
United Kingdom
Tel: +44-(0)125-630-5600
Fax: +44-(0)125-635-5420

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Tel: (408) 739-1010
Fax: (408) 739-1540

Actel Asia-Pacific
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Tel: +81-(0)3-3445-7671
Fax: +81-(0)3-3445-7668

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