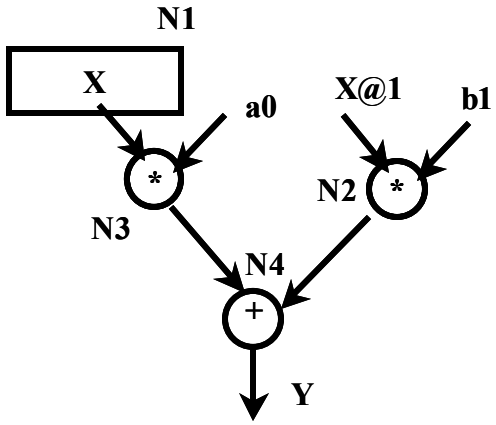
All problems refer to the following flowgraph (Y = x* a0 + x@1 * b1)

Figure 1



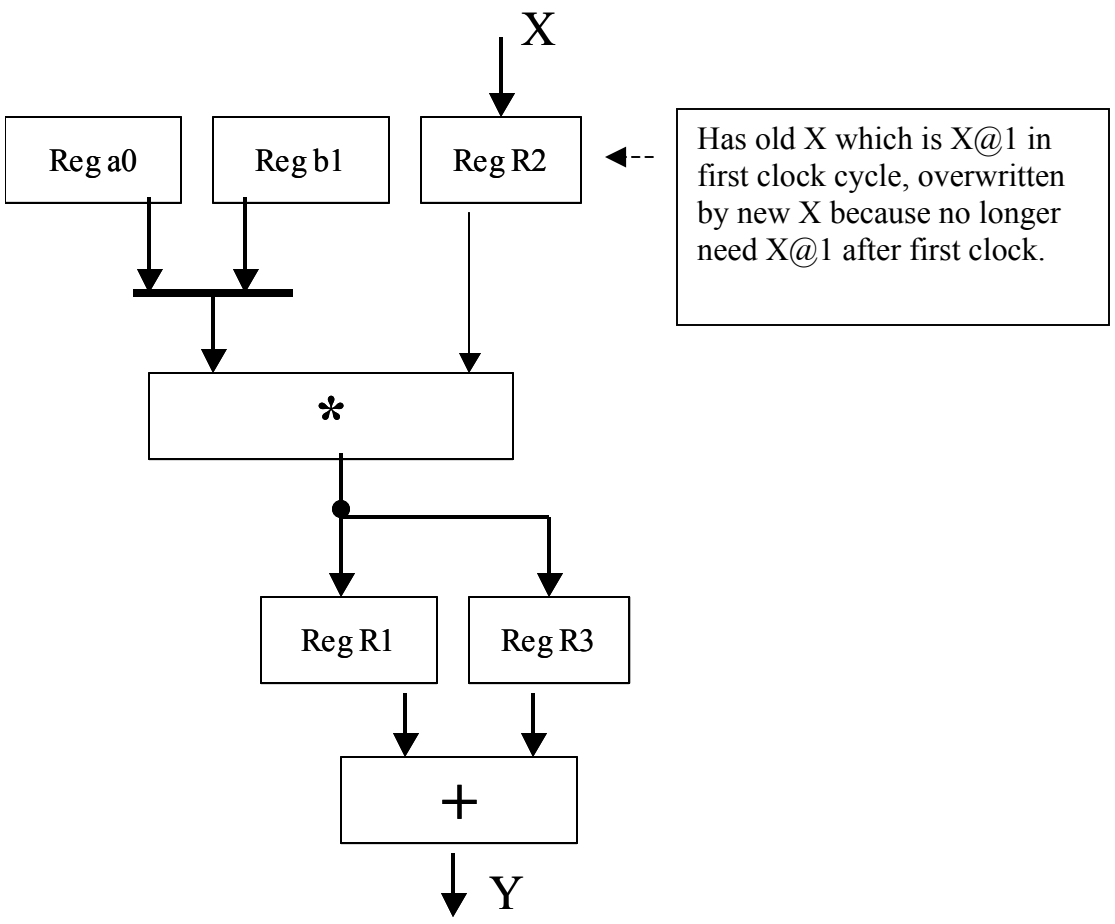
1. Show a schedule for a minimum resource implementation

Some entries may not be filled out!!! Values 'b1', 'a0' are already present in registers.

	Mult A	**Add A**	**Register transfer ops**
Clk 1	N2 R1 ←X@1 (R2)*b1		N1 R2 ←X
Clk 2	N3 R3← X (R2)*a0		
Clk 3		N4 Y = R1 +R3	
Clk 4			
Clk 5			
Clk 6			

How many multipliers ? _____
How many adders? _____
How many registers?
Notes:
Assume R2 initially has X@1 value.

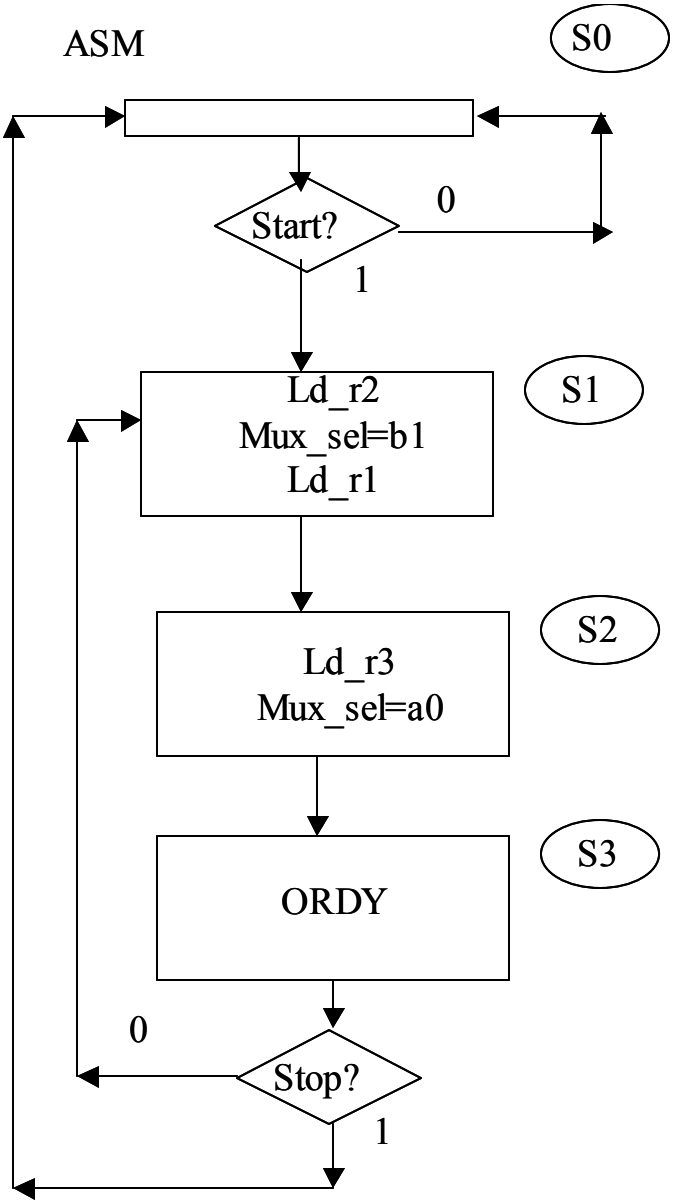
2. Draw a Datapath with registers for minimum resource implementation.



3. ASM Chart Specification

Draw an ASM Chart for your datapath. Your initial state should be a loop which waits for a START signal. After start is received, perform computations until a start signal is received. The number of clocks to perform a computation should match your minimum resource schedule. Assume that the external system provides new input on the first clock cycle of your computation loop without the need for external handshaking.

Assert a ORDY line for one clock each time a result is ready from your datapath.



4. VHDL Entity for ASM Chart

Write the VHDL entity for the FSM required for your design (do not write the architecture, I assume that you can do this).

```
entity  myfsm is
        port (
                clk, aclr:   in std_logic;
                start, stop:        in std_logic;
                ld_r1, ld_r2, ld_3:  out std_logic;
                mux_sel:  out std_logic;
                ordy  :  out std_logic
           );
end myfsm;
```