

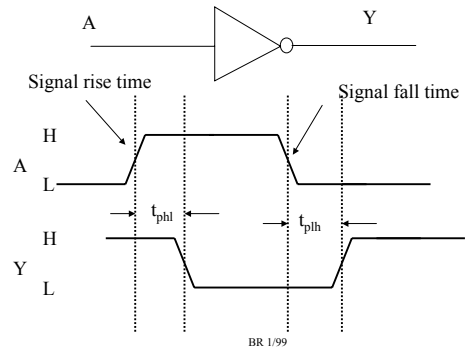
Gate Delay

- Transistors within a gate take a finite amount of time to switch. This means that a change on the input of a gate takes a finite amount of time to cause a change on the output.
- This time is known as **Propagation Delay**
- Smaller transistors means faster switching times. Semiconductor companies are continually finding new ways to make transistors smaller, which means transistors are faster, and more can fit on a die in the same area.

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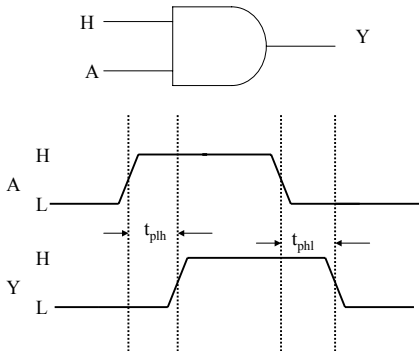
Propagation Delay (inverting)



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Propagation Delay (non inverting)



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Propagation Delay Definitions

- t_{plh} -- time between a change in an input and a low to high change on the output. Measured from 50% point on input signal to 50% point on the output signal. The 'lh' part (low to high) refers to OUTPUT change, NOT input change
- t_{phl} -- time between a change in an input and a high to low change on the output. Measured from 50% point on input signal to 50% point on the output signal. The 'hl' part (high to low) refers to OUTPUT change, NOT input change

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Propagation Delay (non inverting)



Each Input to Output path has its own delay:

$A2Y_{tplh}$, $A2Y_{tphl}$, $B2Y_{tplh}$, $B2Y_{tphl}$

These delays can be different.

For simplicity, may just assign one delay for entire gate:

Y_{tpd}

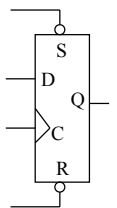
Databooks give typical and maximum propagation delays for combinational outputs.

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DFF Timing

- Propagation Delay**
 - $C2Q$: Q will change some propagation delay after change in C. Value of Q is based on D input for DFF.
 - $S2Q$, $R2Q$: Q will change some propagation delay after change on S input, R input
 - Note that there is NO propagation delay $D2Q$ for DFF!
 - D is a Synchronous INPUT, no prop delay value for synchronous inputs



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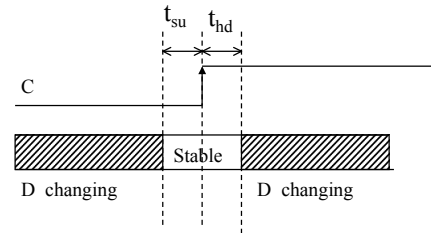
Setup, Hold Times

- Synchronous inputs (e.g. D) have Setup, Hold time specification with respect to the CLOCK input
- Setup Time: the amount of time the synchronous input (D) must be *stable before* the active edge of clock
- Hold Time: the amount of time the synchronous input (D) must be *stable after* the active edge of clock.

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Setup, Hold Time



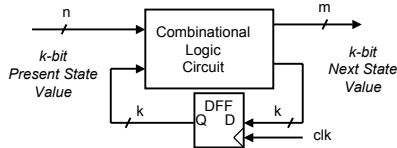
If changes on D input violate either setup or hold time, then correct FF operation is not guaranteed.

Setup/Hold measured around active clock edge.

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Sequential System Timing



Question: What is the MAXIMUM frequency of operation of this system?

Maximum Frequency = $1 / (\text{longest delay path})$

What are longest paths???

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Longest Paths in Sequential System Diagram

Paths to check:

A. Clock to Output delay: $T_{c2q} + T_{comb_Q2O} \text{ max}$
 T_{comb_Q2O} is longest path from Q output to any output

B. Register to Register delay: $T_{c2q} + T_{comb_Q2D} \text{ max} + T_{setup}$
 T_{comb_Q2D} is longest path from Q dff output to D dff input

C. Pin to Pin combinational delay: $T_{comb_I2O} \text{ max}$
 (input pin to output pin, no intervening registers)

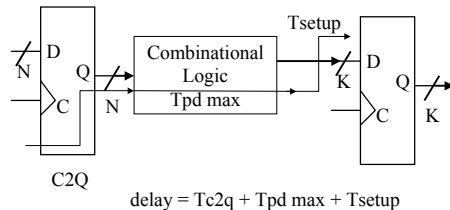
Typically, path "B" is the worst case.

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Inputs/Outputs Registered

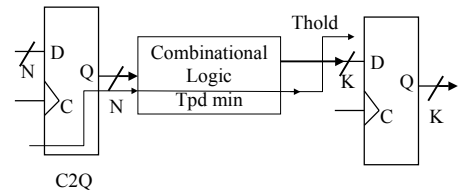
Very often, all inputs and outputs are registered. Then register-to-register delay will almost always determine maximum frequency.



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Hold Time and Shortest Paths



To satisfy hold time:

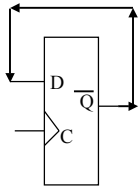
$$T_{c2q} + T_{pd} (\text{minimum}) \geq T_{hold}$$

This is normally easily satisfied in a sequential system.

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Toggle Frequency



$$\text{toggle frequency} = 1 / (C2Q + T_{\text{setup}})$$

assume wire delay is negligible

What about setup time?

$$T_{c2q} + T_{pd}(\min) \geq 0$$

$$T_{cq} > T_{hold}$$

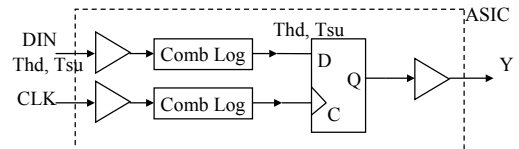
assuming zero wire delay

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Setup, Hold Time for External Inputs

External inputs are buffered through pad drivers and may go through combinational logic before they reach a synchronous input. This buffering adds propagation delay. How does this propagation delay affect the EXTERNAL setup and hold time????

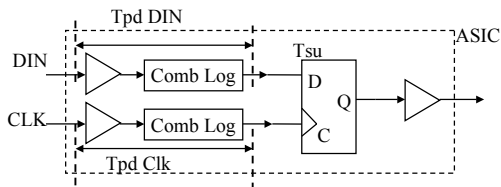


What is T_{hd} , T_{su} for DIN? It is NOT the same as for T_{hd} , T_{su} of the internal D FF!!!!!! T_{hd} , T_{su} for DIN is specified in the DATASHEET for design.

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Calculating External Setup times



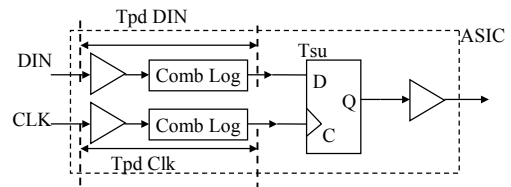
Worst case setup time for DIN occurs when 'DIN' is **DELAYED** relative to CLK. Means clock edge arrives early, requiring DIN to be ready sooner.

$$\text{Din Setup} = T_{su} + T_{pd} \text{ DIN (max)} - T_{pd} \text{ CLK (min)}$$

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Calculating External Hold times



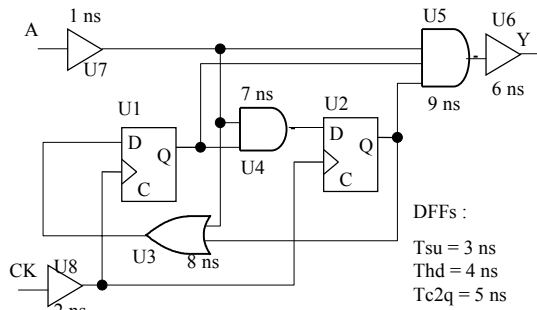
Worst case hold time for DIN occurs when 'CLK' is **DELAYED** relative to DIN. Means clock edge arrives late, requiring DIN to hold its value longer.

$$\text{Din Hold} = T_{hd} + T_{pd} \text{ CLK (max)} - T_{pd} \text{ DIN (min)}$$

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A Timing Example



DFFs :

$$T_{su} = 3 \text{ ns}$$

$$T_{hd} = 4 \text{ ns}$$

$$T_{c2q} = 5 \text{ ns}$$

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Timings

Max Register to Register Delay

$$U2 T_{c2q} + U3 T_{pd} + U1 T_{su} = 5 + 8 + 3 = 16 \text{ ns.}$$

$$\begin{aligned} \text{A setup time} &= T_{su} + A2D T_{pd} \text{ max} - \text{Clk } T_{pd} \text{ min} \\ &= T_{su} + (T_{pd} U3 + T_{pd} U7) - T_{pd} U8 \\ &= 3 + (8 + 1) - 2 = 10 \text{ ns} \end{aligned}$$

$$\begin{aligned} \text{A hold time} &= T_{hd} + \text{Clk } T_{pd} \text{ max} - A2D T_{pd} \text{ min} \\ &= T_{hd} + T_{pd} U8 - (T_{pd} U4 + T_{pd} U7) \\ &= 4 + 2 - (7 + 1) = -2 \text{ ns} \end{aligned}$$

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Timings (Cont)

Clock to Out

$$= U8 \text{ Tpd} + U2 \text{ Tc2q} + U5 \text{ Tpd} + U6 \text{ Tpd}$$

$$= 2 + 5 + 9 + 6 = 22 \text{ ns}$$

Pin to Pin Combinational Delay (A to Y)

$$= U7 \text{ Tpd} + U5 \text{ Tpd} + U6 \text{ Tpd}$$

$$= 1 + 9 + 6 = 16 \text{ ns}$$

$$\text{Max Clock Freq} = 1 / \text{Max (Reg2reg, Clk2Out, Pin2Pin)}$$

$$= 1 / \text{Max (16, 22, 16)}$$

$$= 45.5 \text{ Mhz}$$

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DataSheet

Parameter	Description	Min	Max	Units
Tclk	Clock Period	22		ns
Fclk	Clock Frequency		45.5	Mhz
Atsu	A setup time	10		ns
Athd	A hold time	-2		ns
A2Y	A to Y Tpd		16	ns
Ck2Y	Clock to Y tpd		22	ns

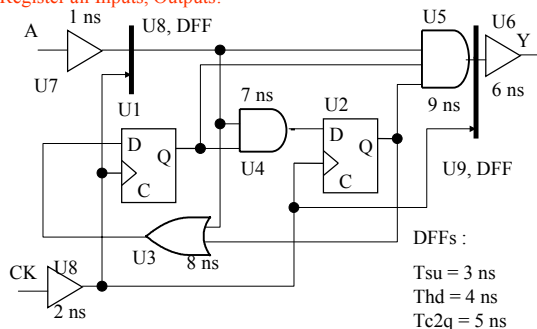
Negative hold times are typically specified as 0 ns.

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How do we improve timings?

Register all Inputs, Outputs!



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New Timings

Max Register to Register Delay

$$U2 \text{ Tc2q} + U5 \text{ Tpd} + U9 \text{ Tsu} = 5 + 9 + 3 = 17 \text{ ns.}$$

$$\text{A setup time} = \text{Tsu} + \text{A2D Tpd max} - \text{Clk Tpd min}$$

$$= \text{Tsu} + (\text{Tpd U7}) - \text{Tpd U8}$$

$$= 3 + (1) - 2 = 2 \text{ ns}$$

$$\text{A hold time} = \text{Thd} + \text{Clk Tpd max} - \text{A2D Tpd min}$$

$$= \text{Thd} + \text{Tpd U8} - (\text{Tpd U7})$$

$$= 4 + 2 - (1) = 5 \text{ ns}$$

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New DataSheet

Parameter	Description	Min	Max	Units
Tclk	Clock Period	17		ns
Fclk	Clock Frequency		58.8	Mhz
Atsu	A setup time	2		ns
Athd	A hold time	5		ns
Ck2Y	Clock to Y tpd		13	ns

Most designs have all inputs, outputs registered.

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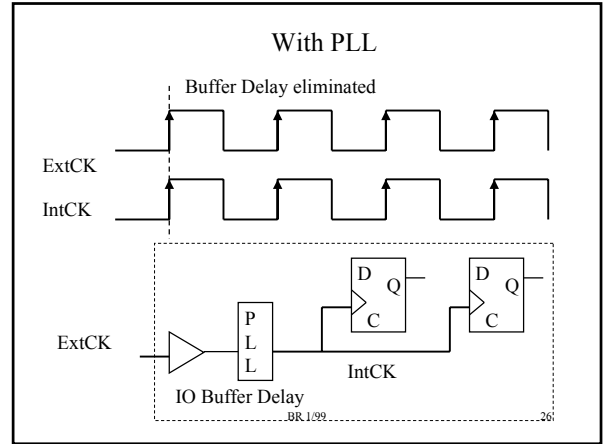
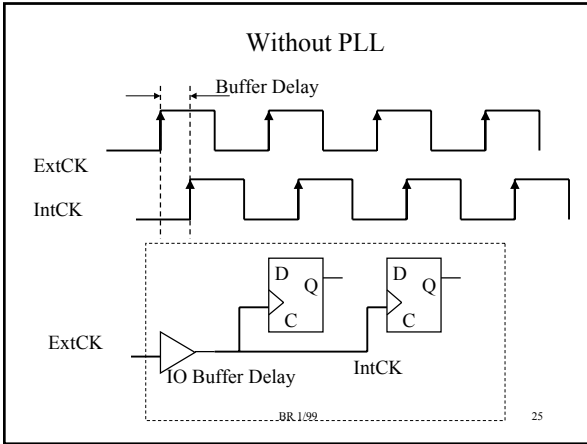
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How does a PLL/DLL help?

- A Phased Locked Loop or Delay Locked Loop circuit is used to align the external clock edge at the pin with the internal clock edges at the DFF clk pins
 - Some clock skew due to clock routing network from PLL will still be present, but input buffer delay eliminated.
- This means that we can drop out the Clk Tpd term from the equations
- How does this change things?

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New Timings (PLL, Inputs/Outputs Reg)

Max Register to Register Delay
 $U2\ Tc2q + U5\ Tpd + U9\ Tsu = 5 + 9 + 3 = 17\ ns.$

A setup time = $Tsu + A2D\ Tpd\ max - Clk\ Tpd\ min$
 $= Tsu + (Tpd\ U7) - 0\ (due\ to\ PLL)$
 $= 3 + (1) - 0 = 4\ ns$

A hold time = $Thd + Clk\ Tpd\ max - A2D\ Tpd\ min$
 $= Thd + 0\ (due\ to\ PLL) - (Tpd\ U7)$
 $= 4 + 0 - (1) = 3\ ns$

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New Timings (PLL, Inputs/Outputs Reg)

Clock to Out
 $= U8\ Tpd + U9\ Tc2q + U6\ Tpd$
 $= 0\ (due\ to\ PLL) + 5 + 6 = 11\ ns$

NO pin to Pin combinational delay! All inputs/outputs registered!

Max Clock Freq = $1 / \text{Max} (Reg2reg, Clk2Out, Pin2Pin)$
 $= 1 / \text{Max} (17, 11, 0)$
 $= 58.8\ Mhz$

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New DataSheet (PLL, Inputs/Outputs Reg)

Parameter	Description	Min	Max	Units
Tclk	Clock Period	17		ns
Fclk	Clock Frequency		58.8	Mhz
Atsu	A setup time	4		ns
Athd	A hold time	3		ns
Ck2Y	Clock to Y tpd		11	ns

Clock to Output improved; important in multiple chip designs. External Setup/Hold times closer to setup/hold times of internal DFFs.

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Chip to Chip Timing Calculation

Need to know external setup/hold times all inputs, clk to out of all outputs, all pin to pin combinational delays.

ASIC = Application Specific Integrated Circuit

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Max Register to Register Delay 2 ASIC System

Assume no pin to pin combinational delays and that inputs/outputs of both ASICs are registered.

For any outputs from ASIC #1 which are Inputs to ASIC #2 find maximum of ASIC #1 Clk to out + ASIC#2 Setup time.

For any outputs from ASIC #2 which are Inputs to ASIC #1 find maximum of ASIC #2 Clk to out + ASIC#1 Setup time.

The maximum of these two times will be the minimum clock period.

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Other Factors that effect Timing

- Voltage: the higher the voltage, the faster that gates switch
- Temperature: the lower the temperature, the faster that gates switch
- Process Technology (transistor gate width). The shorter the transistor gate length, the faster the transistor will switch (I.e. 0.5u process versus 0.35u process).
- In a given process run, may get fast N transistors, fast P transistors, slow N transistors, slow P transistors

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Device Characterization

- Do timing analysis on ASICs at four extreme corners to make sure they meet timing specs under all conditions
- Fastest Case: Fast N transistors, Fast P transistors, High Vdd, Low temperature
- Slowest Case: Slow N transistors, slow P transistors, low Vdd, high temperature
- Other two corners can vary but two possible corners are:
 - Fast N, Slow P, Typical Temperature
 - Slow N, Fast P, Typical Temperature

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Speed Grades

- Databooks often list different **speed grades** for a part at the same temperature
- Simply test parts that come off the fabrication line and see how fast they are
 - Divide the parts into different speed bins
 - For three speed grades, a design goal might be to have 15% of your parts fall in the upper bin, 50% in the middle bin, and 25% in the lower bin.
 - As the process matures, more and more fabricated parts will move into the upper speed bin, at which point you make a new upper speed bin.
 - Obviously, faster parts cost more (and are more profitable)

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Static Path Analysis

- After your gate netlist has been mapped to the FPGA, a timing analysis tool will analyze the paths in the design and compute the timings we have discussed
- The timing analyzer takes into account the routing delays in the physical routing and the speed grade of the part you have mapped to.
 - Because routing can sometimes change somewhat drastically for even small changes, often try run multiple device mappings to try to get a 'good route'.

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Static Timing Analysis Reports

- The static timing analyzer will report the following times
 - Register to Register delays
 - Setup times of all external synchronous inputs
 - Clock to Output delays
 - Pin to Pin combinational delays
- The clock to output delay is usually just reported as simply another pin-to-pin combinational delay
- Timing analysis reports are often pessimistic since they use worst case conditions

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Timing Simulation

- The timings extracted by the Timing analysis tool (routing delays, gate delays for a particular speed grade, etc) are used in the simulation
- It may be tempting to simply ignore the delays reported by the timing analyzer, and simply simulate the design 'at speed' to see if it works.
 - If the design simulates correctly, only means that it works for the particular test vectors that you used!
 - Different test vectors exercise different delay paths - you must use test vectors that exercise the LONGEST paths