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Routing Results For:

Silicore SLC1657 Evaluation Board for Altera FLEX 10KE FPGA

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Test conditions:

Project:	CALCDEMO
Device:	Altera: epf10k50eqc208-3
Synthesis tool:	Altium Accolade PeakFPGA 5.30a
Router:	Altera MAX+PLUS II

For more information, please refer to the SLC1657 Technical Reference Manual.

Timing Results (as reported by router):

Timing constraint (MIN):	5.000 MHz (MIPS)
Actual speed (MAX):	7.830 MHz (MIPS)

Device Utilization Results (as reported by router):

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	Memory Bits	Memory % Utilized	LCs	LCs % Utilized
AF10EVAL	epf10k50eqc208-3	7	4	24	25600	62 %	574	19 %

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