The RASSP Integrated Systems Tool Set Provides a Concurrent Engineering Environment for Design Trade-Offs

Gregory Barnett • Lockheed Martin • Camden
Charles Fry, PE • Lockheed Martin • Camden

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SUMMARY

The goal of the DARPA/Tri-Service-sponsored Rapid Prototyping of Application Specific Signal Processors (RASSP) program is to reduce development and manufacturing time and cost of signal processors by a factor of four. Lockheed Martin's Advanced Technology Laboratories (ATL) RASSP team has developed an integrated systems engineering tool set which forms the basis for a concurrent engineering design environment. This design environment, which consists of Ascent Logic's RDD-100, PRICE Systems parametric cost estimation models, and Management Sciences RAM-ILS tools, provides the integrated product development team with cost and reliability estimation data within a systems engineering tool. The concurrent engineering design environment is described and an example is provided which demonstrates the value of the tool integration within the design environment. This design environment enables the integrated product development team to estimate the life-cycle costs and reliability early in the design process.

1. INTRODUCTION

The goal of the DARPA/Tri-Service-sponsored Rapid Prototyping of Application Specific Signal Processors (RASSP) program is to reduce digital signal processor development and manufacturing time and cost by a factor of four. Systems engineering decisions early in a project significantly impact schedule and cost. Decisions are typically based on the impact to the current phase of a project rather than the project's overall life cycle. Figure 1 shows a typical comparison of cost incurred to cost committed. To help the integrated product development team (IPDT) make these trade-offs, the ATL RASSP team developed a concurrent engineering environment consisting of Ascent Logic Corporation's (ALC) RDD-100 tool with PRICE Systems parametric cost estimation models and Management Sciences' (MSI) RAM-ILS tool set, as shown in Figure 2. Design information is passed among these tools in this concurrent engineering environment to provide design, cost, reliability, availability, and maintainability support to the IPDT.

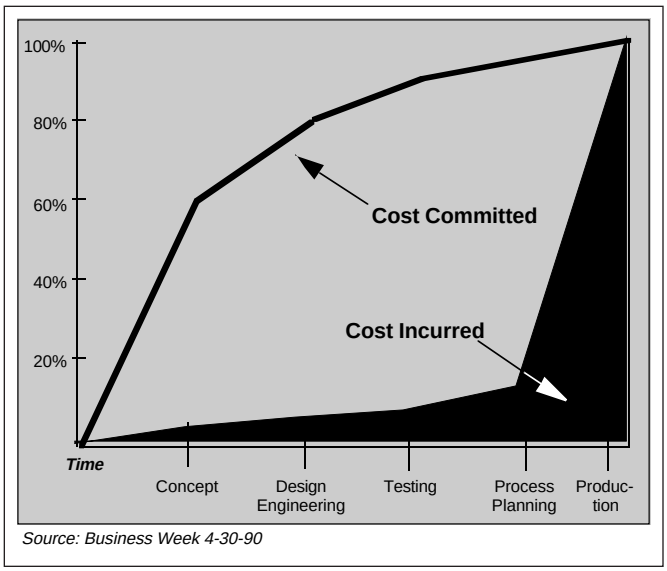

Figure 1. Project costs.

The RASSP concurrent engineering environment provides the IPDT with the information they need to make decisions early, while making changes is still easy and inexpensive. This environment will allow engineers to make decisions based not only on the current effect of a change, but on the predicted long-term impacts. This information is essential to significantly reducing life-cycle costs.

2. DESIGN ENVIRONMENT OVERVIEW

The RASSP concurrent engineering environment consists of ALC's RDD-100, PRICE System's cost estimating tools and MSI's RAM-ILS toolset as shown in Figure 3. The capabilities for each individual tool and for the integrated tool set are described next.

2.1 RDD-100

The ATL RASSP team selected Ascent Logic Corporation's RDD-100 tool as the central tool of its integrated tool set. This tool provides requirements analysis, functional analysis,

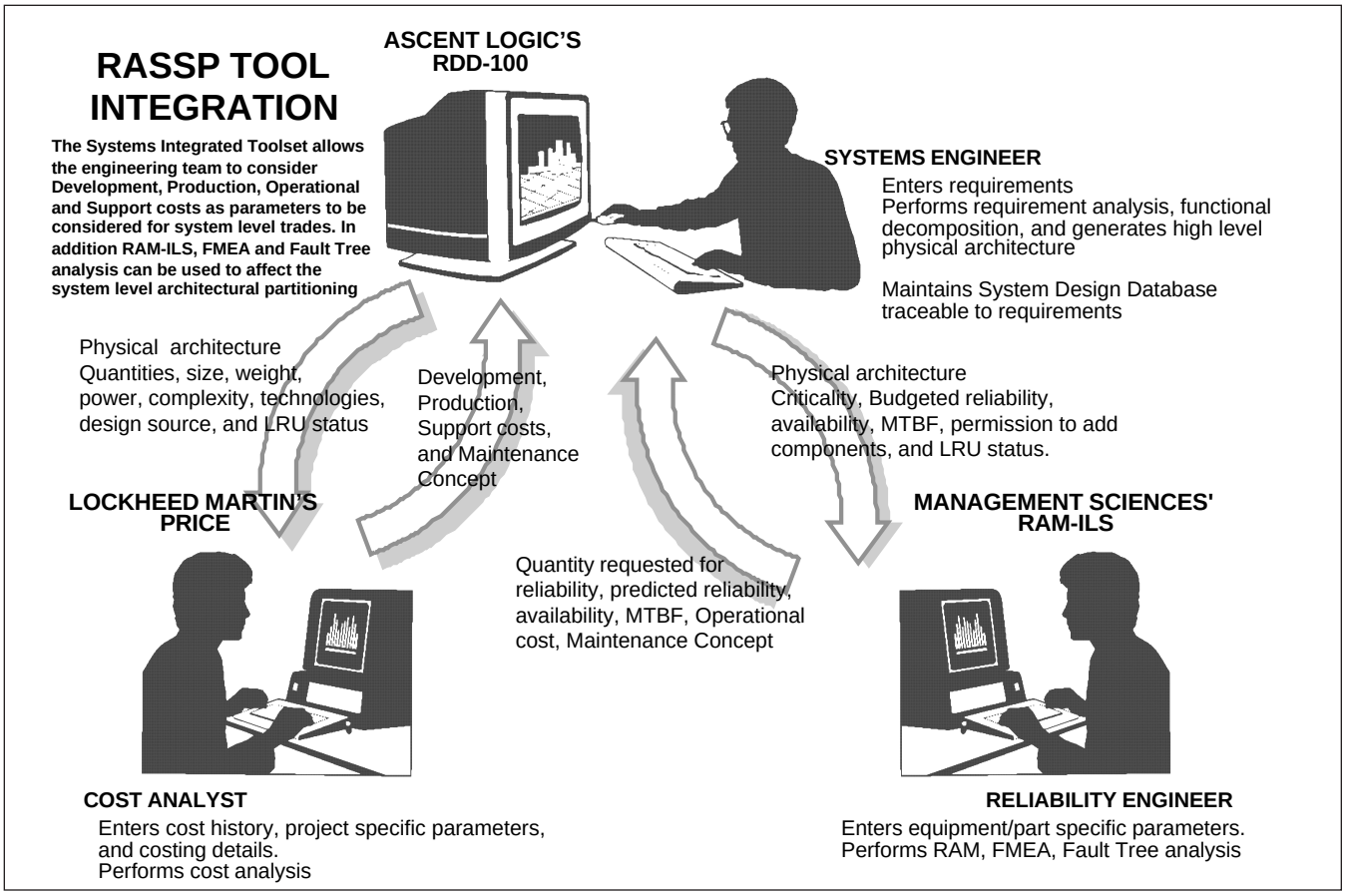

Figure 2. RASSP concurrent engineering environment.

and physical decomposition. It is an Entity, Relationship, Attribute (ERA) database tool with a substantial graphical data entry user interface. RDD-100's database capability enables it to be the primary data storage tool for the tool set. The ATL RASSP Team defined a set database extensions that can support the IPDT through the life of a project.

The RDD-100 tool provides the IPDT with three different views of a system: a requirements view, a functional view, and a physical view. The requirements can be related to the functions and the functions can be allocated to the physical architecture. The interrelation of these three views enables users to automatically generate the lower specification documents from the RDD-100 database. The physical view enables cost analysis and reliability and maintainability analyses.

2.2 PRICE Systems Cost Estimation Models

The ATL RASSP team selected PRICE Systems' parametric cost estimation models as the cost analysis tool. These models were originally intended to be used by a cost analyst. PRICE Systems modified them to allow access to the PRICE models through parameters in the RDD-100 and to provide costing information back to the RDD-100 database. The PRICE Systems' tools are a set of four parametric cost estimation models, each with a different specialty areas. Three of the models focus on hardware costing and the fourth model focuses on software costing.

1. Hardware Costing
   a. PRICE H: This model specifically addresses the costs associated with development and production of hardware. This tool can use outputs of the PRICE M tool.
   b. PRICE HL: This model uses data generated by PRICE H and calculates the hardware life-cycle costs, including sparing for a deployment environment.
   c. PRICE M: This model specifically addresses electronic-module-level hardware development and production costs. It allows engineers to specify individual ASIC and FPGA components to get a detailed cost estimate at the lowest levels.
2. Software: This model can estimate both initial development costs and life-cycle support costs for software.

The PRICE models are based on historical models and can be calibrated to match any company's process.

2.3 Reliability, Availability, Maintainability:Integrated Logistics Support (RAM-ILS)

Management Sciences' RAM-ILS tools calculate reliability, maintainability, and availability of a system. This tool set performs MTBCF, MTBF, and availability calculations using

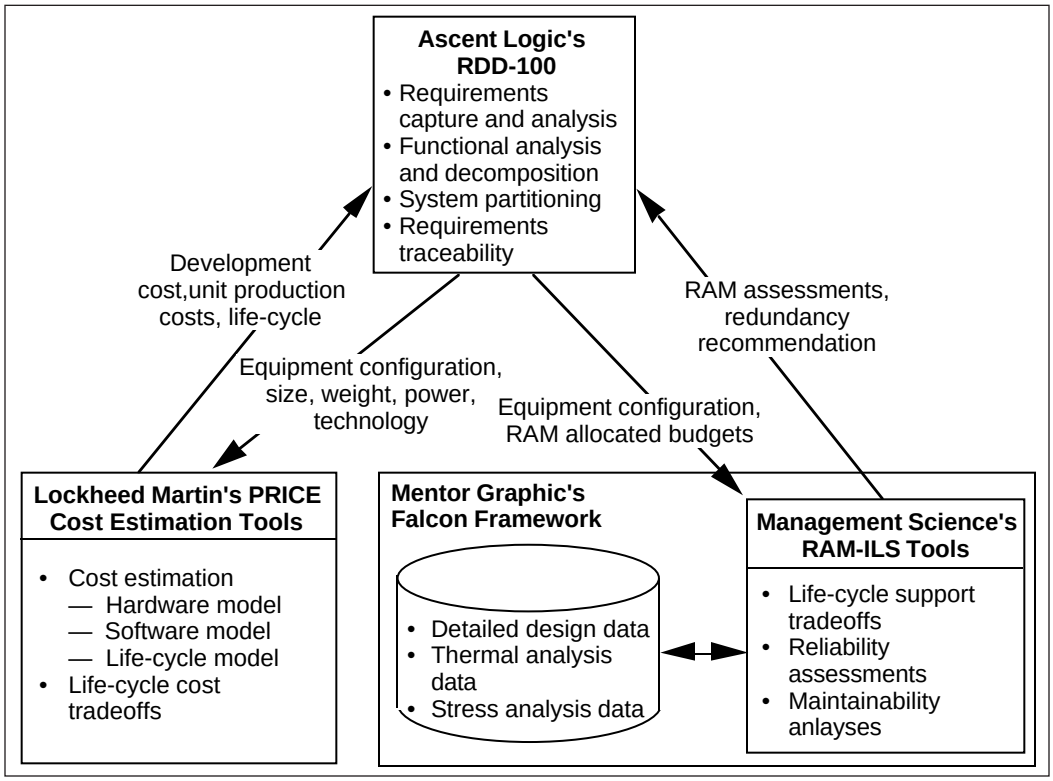

Figure 3. RASSP system tool integration.

several methods, including Mil-Hdbk-217 and BelCore. If the system doesn't meet MTBCF requirements, RAM-ILS will perform a cost driven trade-off and recommend where redundancy should be added to meet the system MTBCF requirement. RAM-ILS was integrated with the Mentor Falcon Framework, which allows it to access the detailed design database to continually improve its estimates as the detailed design progresses.

2.4 Integrated Tools

As a part of the RASSP program, RDD-100, PRICE and RAM-ILS have been integrated so that design information can be passed among the tools when performing system, costing and reliability analyses. These integrated tools provide the capabilities needed by the IPDT. The approach used to integrate these tools within the concurrent engineering design environment was to pass data normally resident within one tool to another tool if that data can be used for analyses within the receiving tool. There has been no attempt to build a graphical user interface within any tool for another tool. All data exchanges for these tools are file based.

3. EXAMPLE TRADE-OFF

The following example problem shows how the concurrent engineering environment can be applied to a trade-off study.

The ATL RASSP team selected a Synthetic Aperture Radar Digital Signal Processor (SAR-DSP) for a trade-off between two different architecture candidates. The Candidate 1 architecture uses a mature technology. As shown in Figure 4, the architecture consists of a single-board computer (used as a controller), five processor elements (PE1-5), a cross bar, a fiber interface, and a VME Bus. Each processor elements contains four separate computational elements (CE1-4). As shown in Figure 5, the Candidate 2 architecture is similar to the first, except that it uses three state-of-the-art processor elements. In addition, PE2 and PE3 contain only two computational elements rather than four.

During the development phase, the trade-off is difficult because a mature technology is less expensive per module and is lower risk, while the state-of-the-art technology has fewer modules, is more compact, and consumes less power. The team followed these steps with each of the candidate architectures while performing the trade-off:

1. Requirement Capture and Analysis

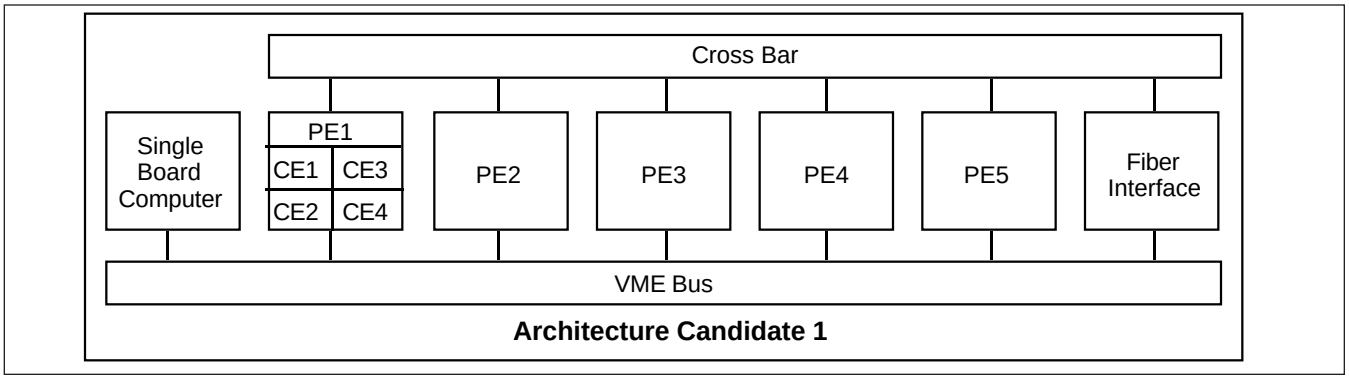

Figure 4. Architecture Candidate 1.

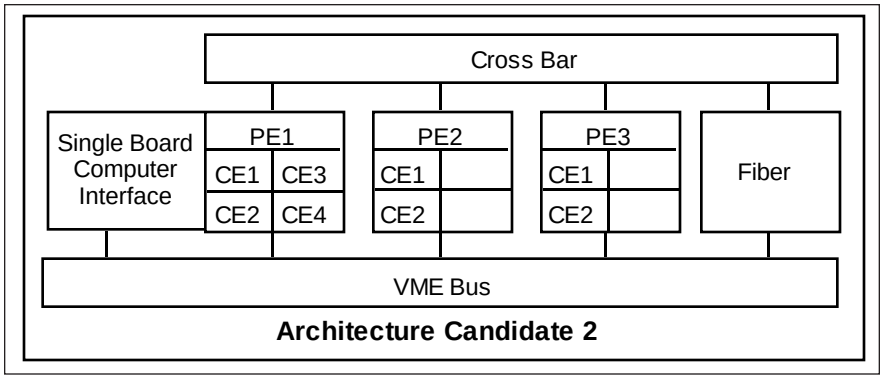

Figure 5. Architecture Candidate 2.

2. Functional Analysis
3. Physical Decomposition
4. Preliminary Cost Calculation
5. Preliminary Reliability Calculation
6. Compute Updated Costing
7. Architecture Trade-Off.

3.1 Requirements Capture and Analysis

The initial requirements capture and most of the requirements analysis were essentially identical for both candidate architectures. The originating requirements came from a Technical Description Document. The team reworded and reordered these requirements to create a B2 document for the signal processor. After completing the initial requirements decomposition, the team performed a functional analysis.

3.2 Functional Analysis

The functional analysis for both candidate architectures was the same since both architectures are functionally equivalent. The functions were decomposed down to the point where each leaf-level function could be allocated to a hardware or software element. At this point, some information about the hardware/software partition may help minimize future changes to the functional decomposition.

3.3 Physical Decomposition

The physical decomposition is the only information required to perform cost and reliability analysis. The team developed an equipment/software tree for both candidates that was essentially identical. The primary difference was in the quantities of processor element assemblies. Table I shows an element tree for each of the candidates.

While generating the equipment/software tree, the following information must be populated in the RDD-100 database for each element:

1. Component type (enumerated list: system, system segment, subsystem, hardware element, part, FWCI, FWU, FWC, CSCI, CSU, or CSC)
2. Component subtype (enumerated list: high-level assembly, cabinet, drawer, enclosure, multiple-board assembly, board, backplane/cabling, power supply, ASIC, or FPGA)
3. Quantity in next higher assembly
4. Quantity required for operation
5. Redundancy mode (enumerated list: operational or standby)
6. Budgeted length, width, and depth (in feet)
7. Budgeted weight (in pounds)
8. Budgeted power (Watts)
9. Technology (enumerated list: digital discretes, digital IC, digital LSI, digital hybrid, digital VLSI, digital VHSIC,

Table I. Architecture Candidate Module Complement.

Item	Architecture 1			Architecture 2		
	QTY NHA	Design	Maturity	QTY NHA	Design	Maturity
Fiber Interface Assembly	1	—	—	1	—	—
— Data IO Module	1	New	Leading Edge	1	New	Leading Edge
— Fiber Optic Daughter Card	1	COTS	Mature	1	COTS	Mature
— FIR Filter Daughter Card	1	NEW	Leading Edge	1	NEW	Leading Edge
Host Interface	1	COTS	Mature	1	COTS	Mature
Processor Element Assembly	5	—	—	3	—	—
— Mother Board	1	COTS	Leading Edge	1	COTS	Leading Edge
— CE Daughter Card 1	2	COTS	Mature	1 or 0	COTS	Mature
— CE Daughter Card 2		—		1	COTS	SOA
Chassis	1	COTS	Mature	1	COTS	Mature
Backplane Assembly	1	—-	—	1	—	—
— VME Backplane	1	COTS	Mature	1	COTS	Mature
— Crossbar	1	COTS	Mature	1	COTS	Mature

COTS : Commercial off the Shelf SOA : State of the Art QTY NHA: Quantity in Next Higher Assembly

analog discretes, analog IC, analog VLSI, analog VHSIC, or analog MMIC)
10. Technology maturity (enumerated list: state-of-the-art, leading edge, mature, or obsolete)
11. Design source (enumerated list: new, COTS, furnished, reuse, modified COTS, modified furnished, or modified reuse).

Where possible, the team placed the data entry in enumerated lists to guide the IPDT in how to use these fields. Most cost, reliability, availability, and maintainability fields in the RDD-100 database have places for both budgeted and predicted values. As predicted values are available, the cost and RAM tools will use the predicted values instead of budgeted values. This approach leaves the budgets intact while still getting updated information.

3.4 Preliminary Cost Calculations

The team calculated the preliminary cost using the PRICE H and PRICE HL tools. The PRICE tool was configured previously with company-specific calibrations and a deployment environment and scenario. The deployment scenario included two prototypes and 500 production units over a 20-year mission, with 20 organization sites and one depot maintenance site. An export to PRICE was run from the RDD-100 tool and an import was then run in the PRICE tools. Table II shows the calculated costs for Candidate 1. This data was exported from the PRICE tools back to RDD-100. The whole cost analysis and back population can be done in less than 1/2 hour. This process allows the IPDT to quickly assess several similar architectures.

3.5 Preliminary Reliability Calculation

After completing the first costing, an export can be performed from RDD-100 to the RAM-ILS tool set. This tool set then calculates the overall MTBCF and compares it to the budgeted value. In this case, Candidate 1 only achieved a 2069-hour MTBCF for a 2400-hour requirement. Based on a cost trade-off performed within the RAM-ILS tool, this tool then recommends that the requirement can be met if a redundant fiber interface is added. RAM-ILS generates the back population results for transfer into the RDD-100 tool. Each component has an attribute "quantity requested for RMA" that will indicate where RAM-ILS suggests redundancy. Note that this is just a recommendation from the RAM-ILS tool; systems engineers must determine the feasibility of this recommendation. All the RMA calculations were performed against the original system. If users believe that this suggestion is proper and feasible given the hardware and software configuration, they can change the "quantity in next higher level assembly" and run the RAM-ILS tool on the new configuration. The final MTBCF for Candidate 1 with the recommended redundancy was 2607 hours.

Table II. Candidate 1 Preliminary Cost.

Cost Cycle	Predicted Cost ($K)
Development Cost	376
Production Cost	86,832
Life Cycle Support Cost	30,568
Total Cost	117,776

3.6 Cost Updates

At this point, the architecture had changed and more accurate MTBF numbers were available in the database. The team ran the PRICE tools a second time, which provided a more accurate cost assessment, as shown in Table III.

Table III. Candidate 1 Updated Costs.

Cost Cycle	Predicted Cost ($K)
Development Cost	376
Production Cost	90,479
Life Cycle Support Cost	35,011
Total Cost	125,866

3.7 Architecture Trade-Off

The team performed similar cost analysis and RMA analysis for Candidate 2. The costing and reliability results for both candidates are shown in Table IV. During a typical project, the development costs would be the primary criteria to select the best architecture. Therefore, the life-cycle costs would not be minimized. With the concurrent engineering design environment, the IPDT can pick the most cost-effective solution based on the total life-cycle costs. In the past, Candidate 1 would typically have been selected because there was no easy process to determine life-cycle costs. It is clear from this example that Candidate 2 is the better solution because it is less expensive and more reliable.

With the tools in the concurrent design environment, this information is easily estimated, even during a proposal effort.

Table IV. Trade-Off Table.

Cost Type	Candidate 1 ($K)	Candidate 2 ($K)
Develop Cost	376	422
Production Cost	90,479	72,482
Life Cycle Support Cost	35,011	25,468
Total Cost	125,866	98,372
MTBCF	2607 hours (Redundancy Required)	3296 hours (No Redundancy)

4. DETAILED DESIGN SUPPORT

After the architecture candidate is selected, the detailed design can begin. As the detailed design progresses, the RAM-ILS integration with the Mentor Falcon Framework permits more accurate reliability predictions based on the design specifics. The team completed the detailed design for the data I/O module and performed a thermal analysis. The results of the thermal analysis indicated junction temperatures as high as 130C. The RAM-ILS tools then predicted an MTBF of 13,320 hours; 30,000 hours was budgeted.

The team then used the RAM-ILS and PRICE tools to support an impact assessment, which is summarized in Table V. The entire signal processor MTBF was budgeted at 2400 hours; the predicted value was 5001 hours due to better-than-predicted performance in other parts of the system. Previously, this would end the trade-off study and the MTBF budget would be re-allocated. Now, the life-cycle cost impacts can be assessed with the new integrated tool set. This assessment showed the life-cycle support costs increased by $2,319K, which is more than 9% of the total support costs. This tool integration provides the information required to include long-term impacts on trade-off studies.

Table V. Candidate 1 Updated Costs.

Cost Type		
Data I/O Module MTBF	30,000 hours	13,230 hours
System MTBF	3,296 hours	5,001 hours
Develop Cost	$422K	$422K
Production Cost	$72,482K	$72,482K
Life Cycle Support Cost	$25,468K	$27,787K
Total Cost	$98,372K	$100,691K

5. CONCLUSION

The ATL RASSP team developed a concurrent engineering environment consisting of three existing computer tools (RDD-100, Price Cost Estimating, and RAM-ILS).

This system design environment quickly provides more detailed and accurate information to the IPDT, and enables them to make better informed decisions early in a system's life cycle and even in the proposal process. Since these early decisions have the largest impact on the overall life-cycle costs of a system, it is important that these decisions be based on all life-cycle costs and not just the cost of the initial development. The tools in this design environment also provide information to support detailed designers throughout the design process.

As shown in the example, it is possible to select the wrong architecture if the decision is only based on the development costs. The life-cycle costs in this example were reduced by over 20% just by understanding these costs early in the development phase. This information is critical in achieving the RASSP goal of a reducing life-cycle costs by a factor of four. The team is evaluating other technologies to further reduce design-cycle times and costs on the RASSP program.

Although ATL developed the RASSP concurrent system engineering environment to work well in the signal processing domain, many of these concepts can be extended into higher-level systems.

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Richard Whitman
Ascent Logic Corporation
Mountainside, NJ
email: whitman@alc.com

Thomas J. Walter
Lockheed Martin PRICE Systems
Mount Laurel, NJ
email: Jim.Walter@PRICEsystems.com

Peter Blemel
Management Sciences
Albuquerque, NM
peter@mgtsciences.com

BIOGRAPHIES

Gregory Barnett
Lockheed Martin Advanced Technology Laboratories
1 Federal Street, A&E Building, 2W
Camden, NJ 08102 USA
email: gbarnett@atl.lmco.com

Mr. Barnett is a Principal Member of the Engineering Staff at Lockheed Martin Advanced Technology Laboratories. He holds a BSEE from Virginia Tech and an MSEE from Syracuse University. He is currently the project engineer and cost account manager developing an integrated system engineering toolset for the RASSP program that will enable systems engineers to estimate life-cycle costs and reliability early in the design process. Mr. Barnett has been developing algorithms and signal processing concepts for the past 17 years.

Charles Fry, PE
Lockheed Martin Advanced Technology Laboratories
1 Federal Street, A&E Building, 2W
Camden, NJ 08102 USA
email: cfry@atl.lmco.com

Mr. Fry is a licensed Professional Engineer who works as a Senior Member of the Engineering Staff at Lockheed Martin Advanced Technology Laboratories. He has a BSEE and an MS in Bioengineering from Penn State University. His current assignment include supporting the RASSP Systems Engineering Effort and participation in the UYS-2A RASSP benchmark. He was previously the Lead Subsystems engineer on a large phase-array radar system. His experience includes: hardware design, firmware design, subsystem integration and test, and radar systems engineering.