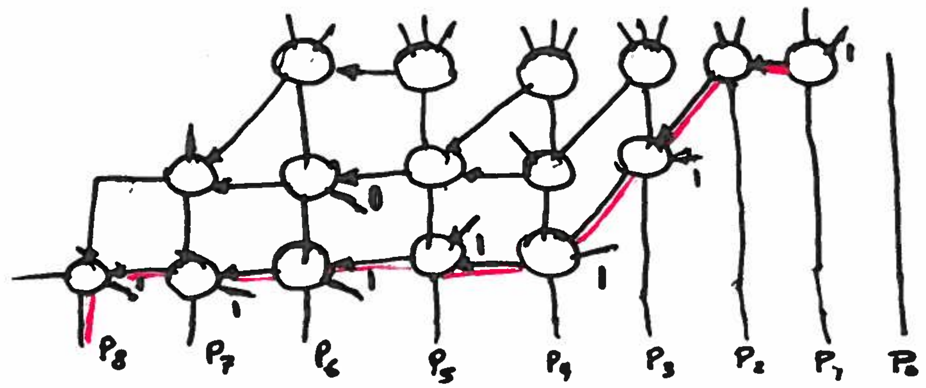
Q1 COEN 6501 Midterm 2015

5 = 00000101
    11111010
           1
-5 11111011

+(-5)

				x_3	x_2	x_1	x_0	
				y_3	y_2	y_1	y_0	
	0	0	0	x_3y_0	x_2y_0	x_1y_0	x_0y_0	
	0	0	x_3y_1	x_2y_1	x_1y_1	x_0y_1	0	
	0	x_3y_2	x_2y_2	x_1y_2	x_0y_2	0	0	
	x_3y_3	x_2y_3	x_1y_3	x_0y_3	0	0	0	
								0
1	1	1	1	1	1	0	1	1



Architecture to calculate 2XY - 5

To check

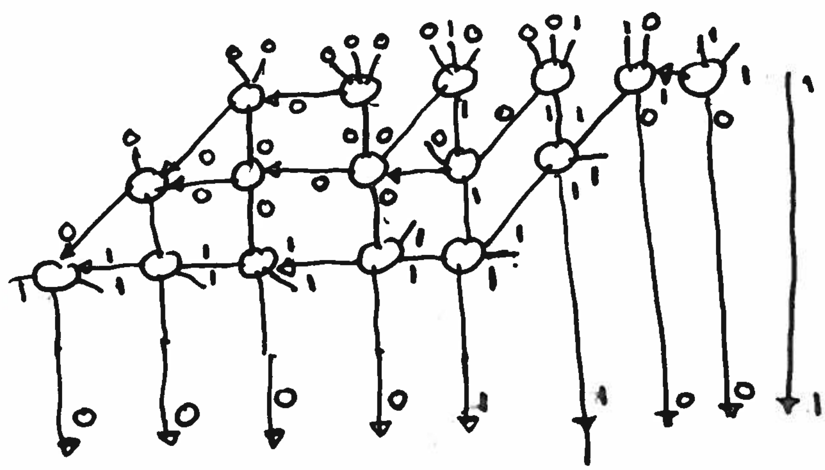
5 0101
3 0011

0101
0101
0000
0000

3 × 5 00001111

2 × 3×5 000011110
        111111011

2× 3× 5 - 5 000011001



Checking with X = 0101 & Y = 0011

Q2

A = 7.25 , $M_A = 111.01_2$, $= 1.1101 * 2^2$, $S_A = 0$, $e_A = 01111111 + 00000010$

$e_A = 10000001$

B = −0.75 $M_B = 0.11$ $= 1.10 * 2^{-1}$, $S_B = 1$ $e_B = 01111111 - 00000001$

$e_B = 01111110$

A = | 0 | 1000 0001 | 1101 ---- 0 |

B = | 1 | 0111 1110 | 100 ---- 0 |

Exp A + Exp B − Bias

Exp A · 1000 0001

Exp B + 0111 1110

1111 1111 .

bias − 1000 0001

1000 0000

2' Complement of 127

0111 1111

1 000 0000

1000 0001

A * B :

1.1101 *

1.1000

11101

11101

10.10111 $= 1.0101111 * 2^1$ normalize exponent

$= M_R$

new exponent 1000 0000 + 0000 0001 = 1000 0001 e_R

Sign of Results $S_R = S_A \oplus S_B = 1 \oplus 0 = 1$

| 1 | 1000 0001 | 01011100...0 |

← A * B

Rounding methodology in IEEE 754 is to the nearest even. Advantage is assuming 50% occurrence of 0 or 1 then error is minimized. disadvantage is extra hardware and the delay produced due to the add.

the rounding method is in accordance with the following Table

	e	M	M_0	R	S

add a "1" if the following condition is statified

R (M_0 + S)

Significand	Rounding	error	Significand	Rounding	error
X0.00	X0	0	X1.00	X1	0
X0.01	X0	−1/4	X1.01	X1	−1/4
X0.10	X0	−1/2	X1.10	X1+1	+1/2
X0.11	X1	+1/4	X1.11	X1+1	+1/4

See notes for architecture

Q3 midterm 2015

Advantage of carry save adders is its speed in comparison to other adders. Disadvantages are high area and power consumption. The best measures for Adders are its Delay-Power, DP or AT^2 where A is the area and T is the delay.

To make the 17-bit adder several alternative exist, some are listed below:

assume $\tau_{MUX} = \frac{1}{2}\tau_{FA}$ i.e. delay of a 2:1 MUX is half of that of a Full Adder:

① 2 2 | 2 | 2 | 3 | 3 | 3 | 1 — $2 + \frac{6}{3} = 5\,\tau_{FA}$ — 32 FA + 21 MUX — * Selected

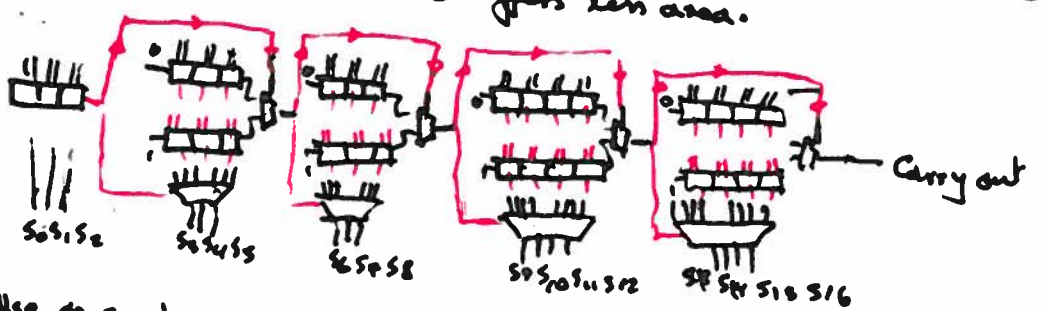
② 3 3 | 3 | 4 | 4 | 1 — $4 + \frac{2}{2} = 5\,\tau_{FA}$ — 31 FA + 18 MUX

③ 4 4 | 4 | 5 | 1 — $5 + \frac{1}{2} = 5\frac{1}{2}\,\tau_{FA}$

④ 3 3 | 3 | 3 | 3 | 2 | 2 | 1 — $3 + \frac{5}{2} = 5\frac{1}{2}\,\tau_{FA}$

⑤ 5 6 | 6 | 1 — $6 + \frac{2}{2} = 7\,\tau_{FA}$

The selection also affect the amount of Full Adders and Muxes used. as shown ① and ② have the same delay but ① offers less area.



Also as can be seen Complexity of the design has increased.