Digital Design COEN 6501
Answer all questions.
All questions carry equal mark

Midterm exam. Oct 13th, 2011
Time allowed 1 hr 30 min.
A.J. Al-Khalili.

Question-1:

Give a logic level design for calculation of Y

$Y = 4\,N^2$,

where N is a 4-bit unsigned binary number.

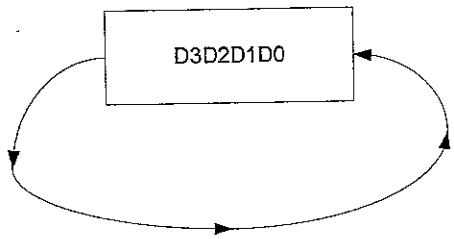
Show this implementation for N=1011. Show the input to each adder clearly. Use "0" when an input is not connected.

Question-2:

Design a minimum delay **14-bit Carry Select Adder**. Give area and delay performance of your adder. Show how you calculated your delay.

Question-3:

a) Design a barrel shifter to do the roll(rotate left logically) instruction for 4-bits of Data $D = D_3\ D_2\ D_1\ D_0$. Use 4 to 1 MUX for this circuit, for shifts of 0, 1, 2, 3. Show your input, output signals clearly and draw the selection table.



b) Using distributed shifting(Using 2 to 1 MUXs) design barrel shifter that can shift $D = D_3\ D_2\ D_1\ D_0$ by up to 3 places. Shifts are to the left. Substitute 0 for data shifted.. Mark all input, output and control lines clearly.

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Question 1

$n_3\ n_2\ n_1\ n_0$

$n_3\ n_2\ n_1\ n_0$

$n_3 n_0$ $n_2 n_0$ $n_1 n_0$ $n_0 n_0$

$n_3 n_1$ $n_2 n_1$ $n_1 n_1$ $n_0 n_1$

$n_3 n_2$ $n_2 n_2$ $n_1 n_2$ $n_0 n_2$

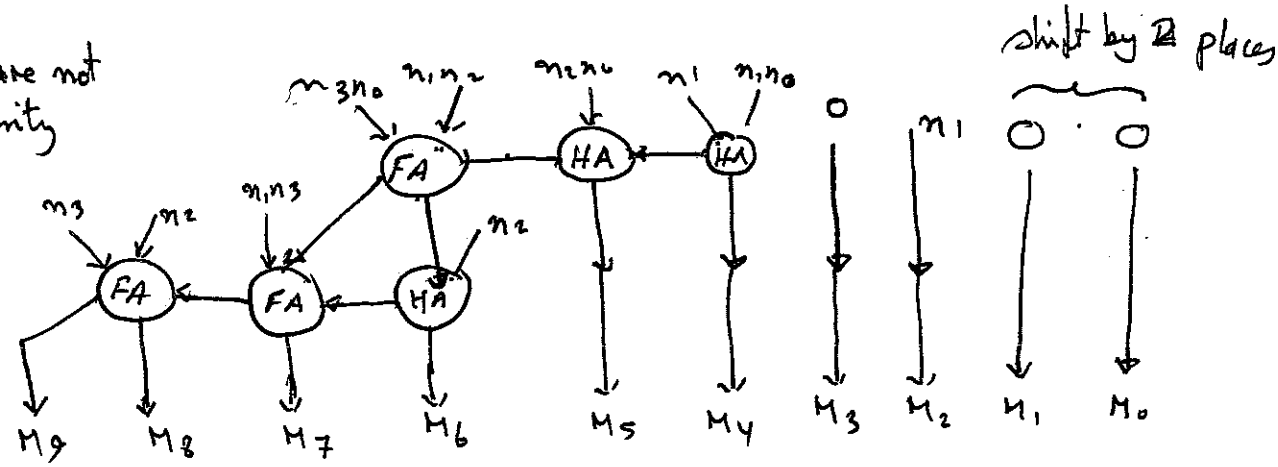
$n_3 n_3$ $n_2 n_3$ $n_1 n_3$ $n_0 n_3$

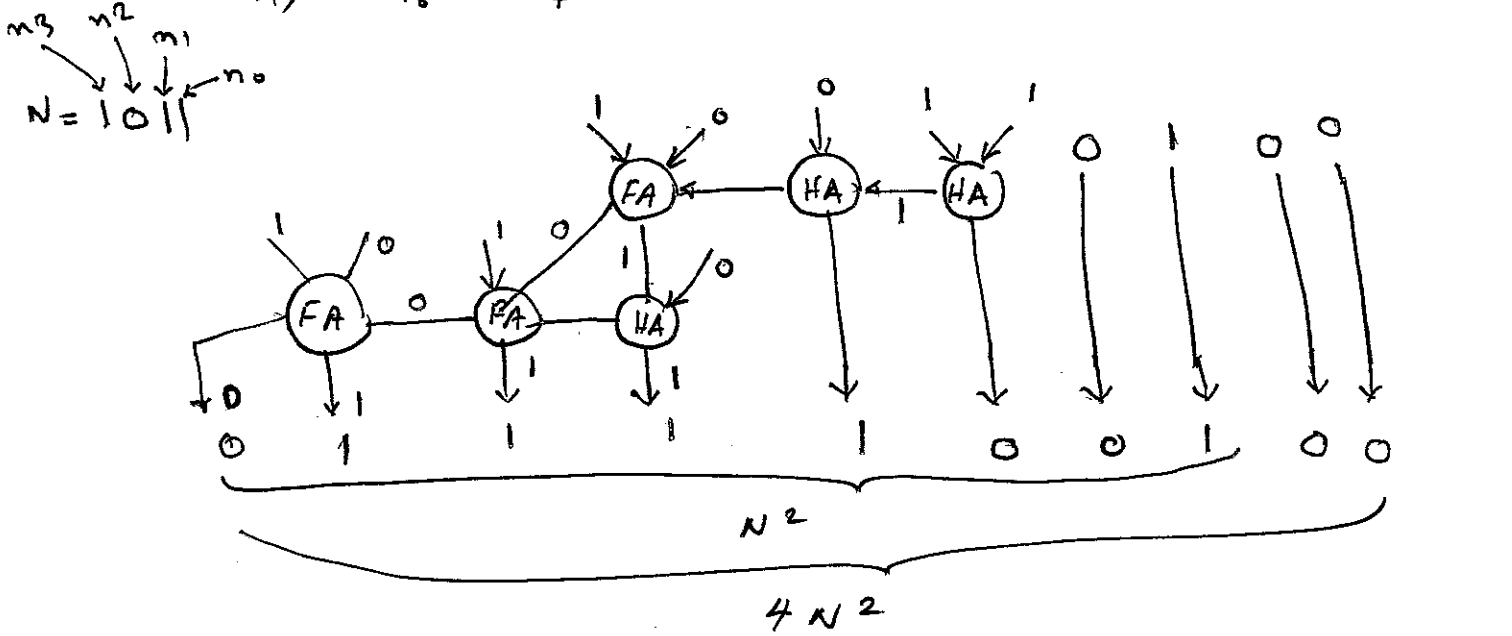
$n_3 n_2$ $n_3 n_1$ $n_3 n_0$ $n_2 n_0$ $n_1 n_0$ 0 n_0

n_3 $n_3 n_2$ n_1

n_2

AND gates are not shown for clarity





Total area required —— 3 FA + 3 HA

Delay of the circuit ——→ $3\tau_{FA} + 3\tau_{HA}$

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Q 2

There is many ways that this CSA can be divided:

		delay
2 2 2 2 2 2 2		$2+6/2=5$
3 3 2 2 2 2 2		$3+6/2=6$
3 3 3 3 2		$3+4/2$ 5
* 2 2 2 2 3 3		$2+5/2$ $4\frac{1}{2}$
2 3 3 3 3		$3+4/2$ 5
* 2 2 3 3 4		$4+1/2$ $4\frac{1}{2}$
4 4 4 2		$4+3/2$ $5\frac{1}{2}$
5 5 4		$5+2/2=6$
3 3 4 4		$4+2/2=5$
etc		

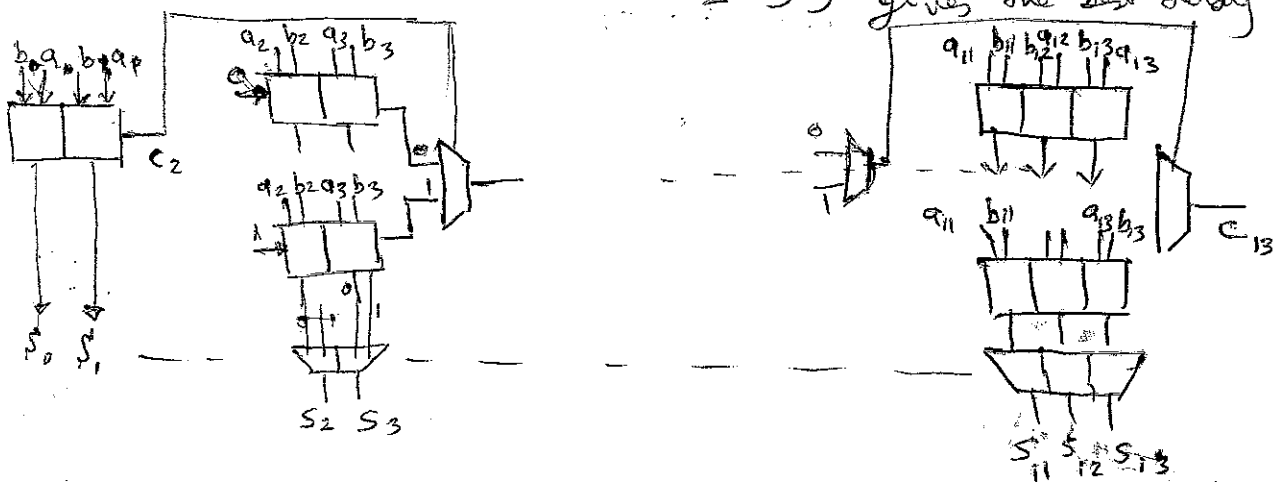
Added: $[2+(4*6)]^{FA}+[6+6*2+6]^{2\to1\,MUX}$

Assuming $\tau_{MUX}=1/2\,\tau_{FA}$

* $[2+[3*4]]+[3*2*2]^{FA}+[3\times2+2*]^{MUX}$

(14, 12)

According to the above search 2 2 2 2 3 3 gives the best delay



Total Delay $\longrightarrow 4\frac{1}{2}\,\tau_{FA}$

Total Area $\longrightarrow$ 26 FA + 17 MUX $_{2\to1}$

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Q1

a)

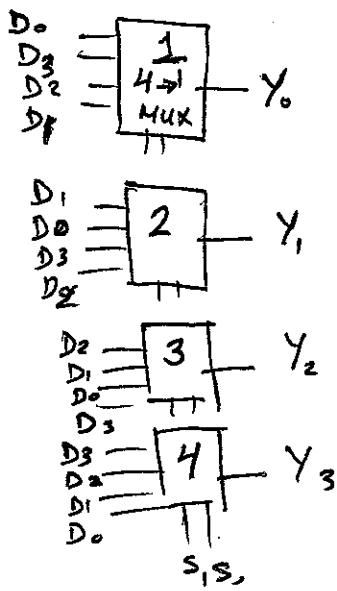
S_1 S_0	Y_3 Y_2 Y_1 Y_0
0 0	D_3 D_2 D_1 D_0
0 1	D_2 D_1 D_0 D_3
1 0	D_1 D_0 D_3 D_2
1 1	D_0 D_3 D_2 D_1

Input to MUX 4

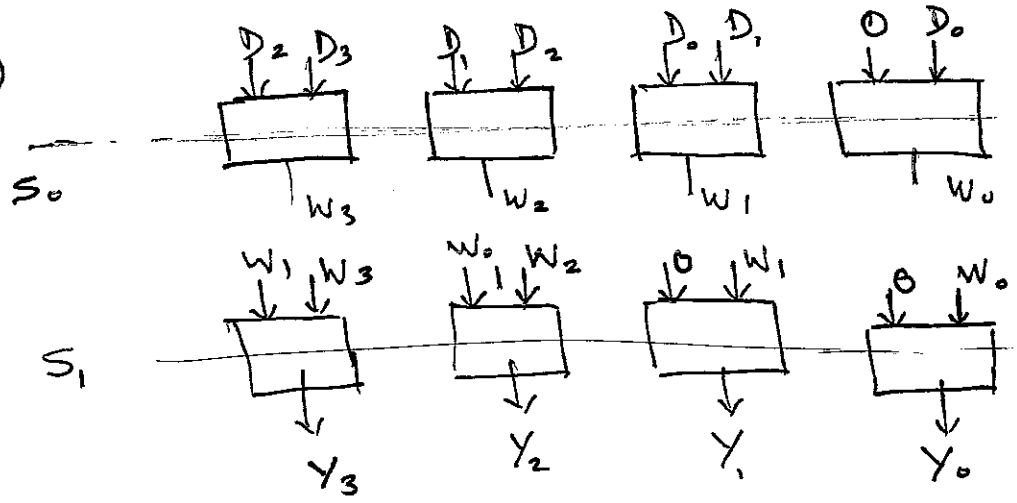
Input to Max 3

Input to Mux 1

Input to Mux 2



b)



S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	D_3	D_2	D_1	D_0
0	1	D_2	D_1	D_0	0
1	0	D_1	D_0	0	0
1	1	D_0	0	0	0