COEN-6501 DIGITAL SYSTEMS AND SYNTHESIS

Final Examination, Dec. 13, 2012 — Examiner: A. J. Al-Khalili
Official Calculators are allowed
Time Allowed: 3hrs — Answer all questions
All questions carry equal weight

Question 1

The following VHDL model illustrates embedded code for generate statements to describe a two dimensional structure.

a. Correct all syntax and semantic errors.
b. Draw the logic diagram described by the VHDL model.
c. Generate the Boolean expression for X = F(A,B).

```
L1   Entity Logic is;
L2   port (A,B: in BIT (3 downto 0) X: out bit);
L3   end LOGIC
L4   architecture STRUCTURE of LOGIC is
L5   component AND2-GATE
L7   port
L6   (A,B: in BIT; Z: out BIT); end component;
L7   component OR_2GATE port (A,B: in BIT; Z out out bit); end component
L8   OR2_GATE;
L9   signal ASIG , OSIG: BIT_VECTOR( 3 downto 0) : = X"0";
L10  begin
L11  R: for COL in 1 to 2 generate
L12      C: for ROW in 3 downto 0 generate
L13          R1: if (COL=1) generate
L14            AX: AND2_GATE portmap (A(ROW), B(ROW), ASIG(ROW));
L15      end generate R1;
L16      R1C: if (COL=2 and ROW/=0) generate
L17          OX: OR_2GATE portmap(ASIG(ROW), O(ROW), OSIG(ROW-1));
L18      end generate RIC;
L19      R1C0: if (COL=2 and ROW=0) generate
L20          O0: OR_2GATE portmap (ASIG(ROW), OSIG(ROW),X);
L21      end generate R1C0;
L22  end generate C;
L23  end generate R;
L24  end STRUCTURE;
```

Question 2

The circuit shown in Fig. 1 given below is a Controller. The timing characteristic of the gates and the flip-flops are listed below. The circuit operates at a supply voltage of 5V±10% in an ambient temperature range of 0 to 25 °C with a power dissipation 0f 1.0 W. The thermal resistance of the package is 40 °C/W and the process variation factor is ±20%. Determine:

a) All the paths in the circuit.

b) The critical path in the circuit. What will be the typical delay of the path?

c) Maximum speed of operation for the worst conditions.

Notes:

1. Arrival times of inputs: Start, Zero, External is at -∞ and all are registered inputs.
2. Temperature degrading factor M=1.5
3. K1, K2 are input and output degrading factors.

Component	Tp (ns)	Input Loading (UL)	K1 (ns/UL)	K2 (ns/fo)
Inverter	0.15	1	0.08	0.1
NAND	0.3	1.5	0.12	0.15
AND	0.8	2.5	0.12	0.15
D-FF (tsu=0.5, th=0.2ns)	0.7	2	0.10	0.2

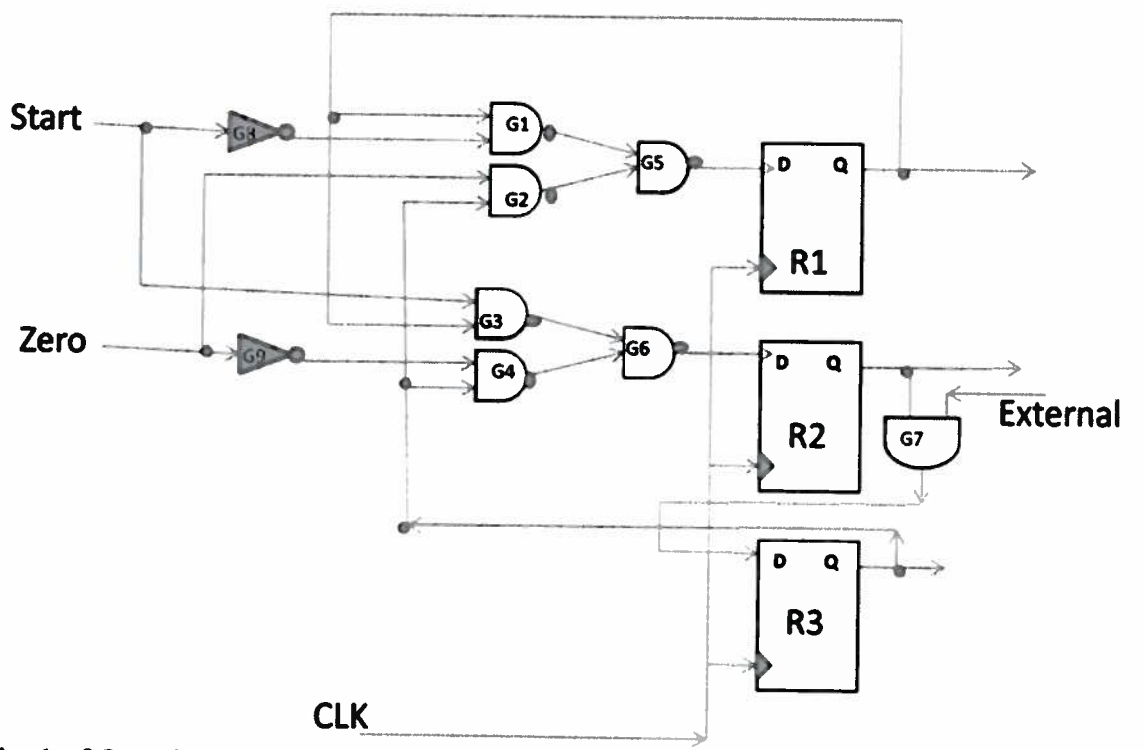


Fig. 1 of Question 2

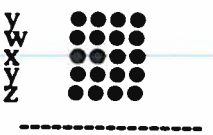
Question 3

a) Design a full Subtractor
b) Implement the subtractor in an FPGA with 2 input Look-Up Tables. Implement the same with a 3 input Look-Up Tables. Compare the two results

Question 4

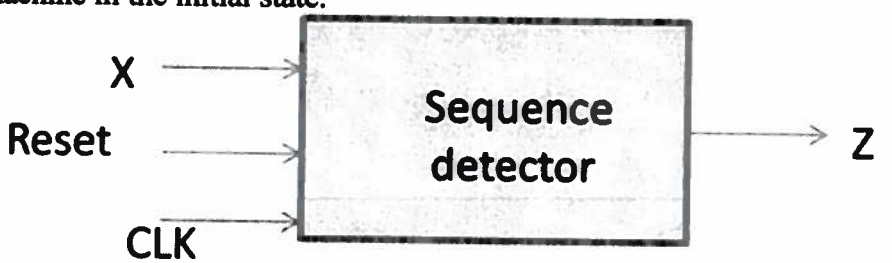
It is required to design a multi-operand adder based on Carry Save Adder (CSA) architecture. Assume the number of operands is equal to five (v,w,x,y,z), each with a width of 4 bits as shown below.

a) Construct the adder using a Manchester carry adder for the output stage.
b) Evaluate the area in terms of equivalent Full Adder, A and delay in terms FA delay D. assume a MUX is 0.5A, 0.5D and any gate is 0.25A,0.25D
c) Insert a pipeline before the Manchester Carry Adder. Perform the necessary analysis to show the impact of addition of the pipeline register on the speed and area. Assume the following parameters for each Flip Flop in the register: Clock to output delay, $T_{CQ} = 1.5D$, Set up time $T_{su} = D$ and Hold time, $T_h = 0.5D$.



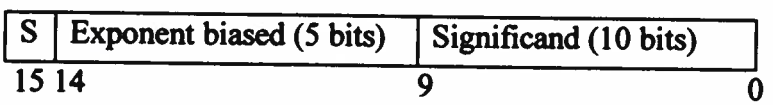
Question 5

Design a Finite State Machine (FSM) to be used as start of a message detector. Serial data, one bit at a time, in packets of 4 bits entering the FSM on line x, are synchronized with the clock and analyzed. The start of data is indicated with arrival of either "1010" or "0101" where an output, z=1 is generated. A separate reset mechanism will put the machine in the initial state.



Question 6

a) Represent A= 0.25 and B= −10 in a floating point format given below assuming a hidden '1'



b) Add, A+ B in a floating point format and give your result in packaged format.
c) Explain the IEEE, rounding method of "to nearest even"
d) Give an architecture for floating point Adder.

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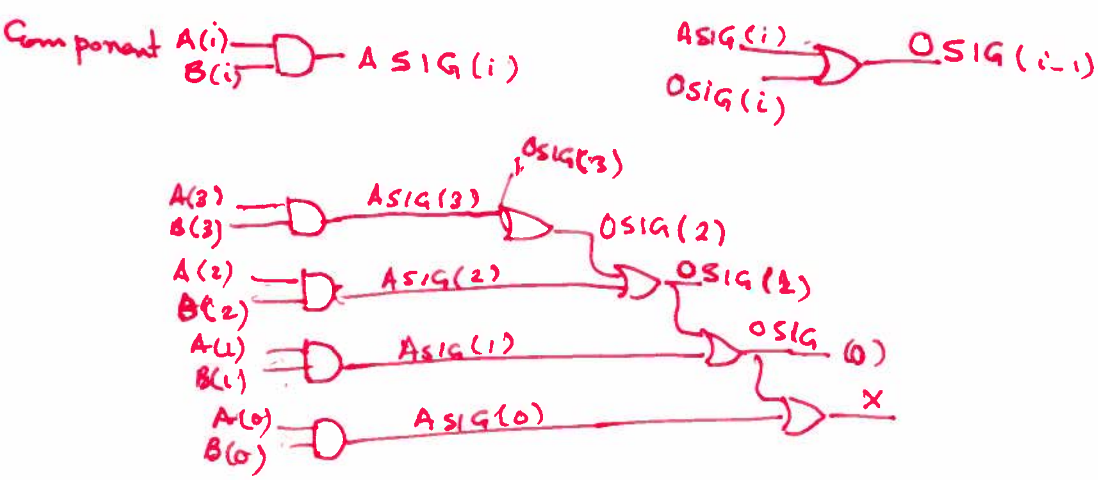
i (4)

```
①     L1   Entity Logic is;          ← remove ";"
②, ③  L2   port (A,B: in BIT (3 downto 0) X: out bit);   ← should be BIT_VECTOR ; Add ";" after (3 downto 0)
④     L3   end LOGIC                 ← Add ;
      L4   architecture STRUCTURE of LOGIC is
⑤     L5   component AND2-GATE       ← underscore
      L7   port
      L6   (A,B: in BIT; Z: out BIT); end component;
⑥     L7   component OR_2GATE port (A,B: in BIT; Z out out bit); end component   ← remove "out"
      L8   OR2_GATE;
      L9   signal ASIG , OSIG: BIT_VECTOR( 3 downto 0) : = X"0";
      L10  begin
      L11  R: for COL in 1 to 2 generate
      L12        C: for ROW in 3 downto 0 generate
      L13           R1: if (COL=1) generate
      L14              AX: AND2_GATE portmap (A(ROW), B(ROW), ASIG(ROW));
      L15        end generate R1;
      L16        R1C: if (COL=2 and ROW/=0) generate
⑦     L17           OX: OR_2GATE portmap(ASIG(ROW), O(ROW), OSIG(ROW-1));   ← O → OSIG
⑧     L18       end generate RIC;           ← I → 1
      L19       R1C0: if (COL=2 and ROW=0) generate
      L20           O0: OR_2GATE portmap (ASIG(ROW), OSIG(ROW),X);
      L21        end generate R1C0;
      L22    end generate C;
      L23   end generate R;
      L24   end STRUCTURE;
```

ii (9)



iii (3)

$$X = (((A(3) \cdot B(3) + \underbrace{OSIG(3)}_{=0}) + A(2)\,B(2)) + A(1)\,B(1)) + A(0)\,B(0)$$

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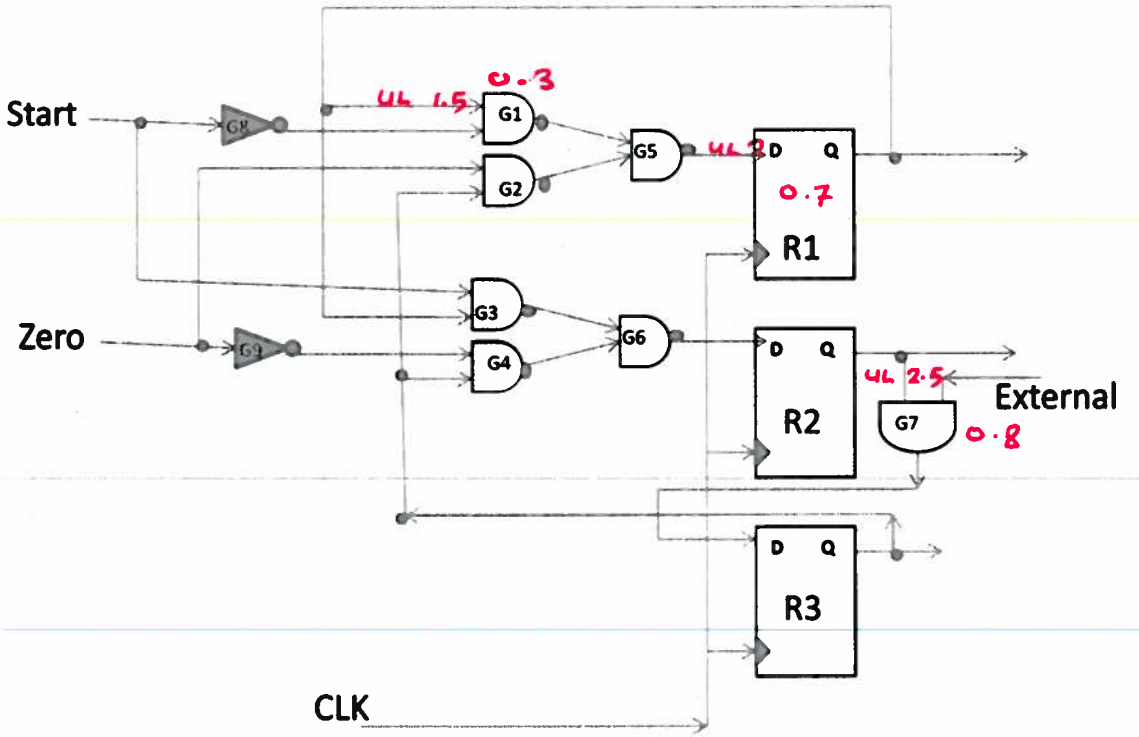

d) (3)

There are 5 paths

① $R_1 \rightarrow G_1 \rightarrow G_5 \rightarrow R_1$
② $R_1 \rightarrow G_3 \rightarrow G_6 \rightarrow R_2$
③ $R_3 \rightarrow G_4 \rightarrow G_6 \rightarrow R_2$
④ $R_3 \rightarrow G_2 \rightarrow G_5 \rightarrow R_1$
⑤ $R_2 \rightarrow G_7 \rightarrow R_3$

Paths ① ② ③ ④ are EQUAL

b) (4)

Path ①

$0.7 + 0.2(3) + 2 * 0.1(1.5)$
$0.3 + 0.15(1) + 0.12(1.5)$
$0.3 + 0.15(1) + 0.12(2)$

$+ 0.5 = 3.42$ ns

Path ⑤

$0.7 + 0.2(1) + 0.1(2.5)$
$0.8 + 0.15(1) + 0.12(2)$

$+ 0.5 = 2.84$ n

Critical path is path 1. With max frequency of $\frac{1}{3.42} \Rightarrow \underline{292.4}$ MHz

6) (3) Worst case

$T_a = 25^\circ C$ $\theta = 40^\circ C/W$ $P = 1W$

$P = \frac{T_J - T_a}{\theta}$ $T_J = 65^\circ C$

$f_t = \left(\frac{T_J}{T_a}\right)^{-1.5}$ $\left(\frac{338}{298}\right)^{1.5} = 1.20$

Voltage

$$K_V = \frac{1}{(1 \pm 0.01\% V_d)}$$ with ±10% worst case is 90%.

$$= \frac{1}{1 - 0.1} = \frac{1}{0.9} = 1.11$$

Process

$$K_p = (1 + 0.01 K_p)$$ with ±20%

$$= 1 + 0.2 = 1.21$$

$$K = K_p * K_V * K_T = 1.11 * 1.21 * 1.20$$

$$\approx 1.6$$

Worst Case frequency $\approx$ 182.75

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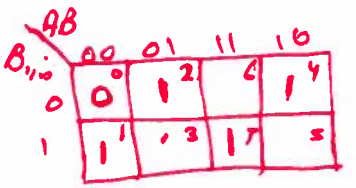
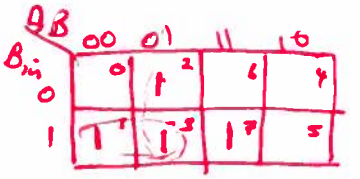
a) ④

	A	B	B_{in}	D	B_{out}
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1



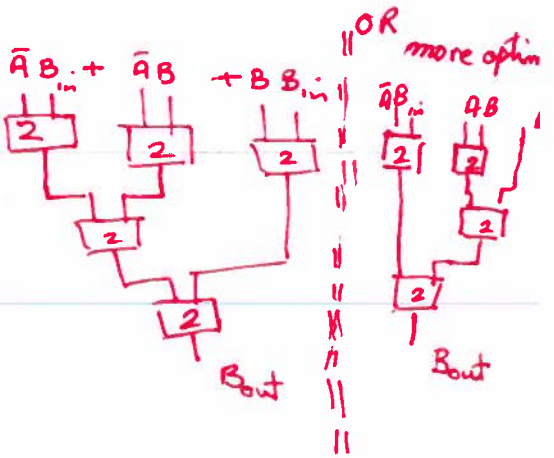
$D = A \oplus B \oplus B_{in}$



$B_{out} = \bar{A}B_{in} + \bar{A}B + BB_{in}$ ✓

Or $B_{out} = \bar{A}B + B_{in}(A \oplus B)$ ✓

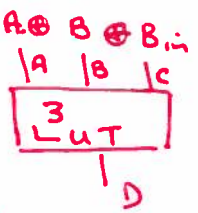
Two input table

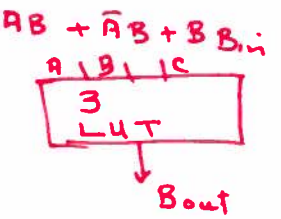


Implementation

b) ③

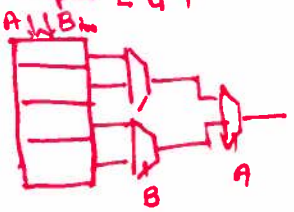
Three input Table





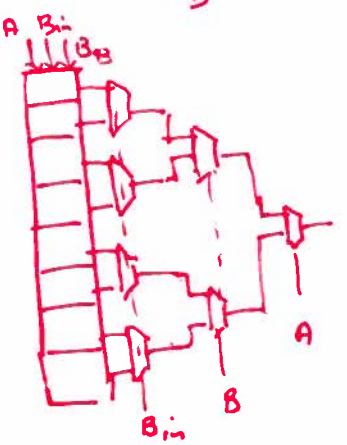
c) ③

2 input LUT



A2
Area of 2 variable LUT:
4 Cell + 3 MUX

D2
Delay Read:
1 Cell + 2 MUX



A3
Area of 3 variable LUT:
8 Cell + 7 MUX

D3
Delay Read:
1 Cell + 3 MUX

Comparison

Area of 2 LUT
7 A2 = 28 Cell + 21 MUX

Delay of 2 LUT
1 Cell + 6 MUX

Area of 3 LUT
8 Cell + 7 MUX

Delay of 3 LUT
1 Cell + 3 MUX

Comparison

Using 3-input LUT is faster and more saving in area

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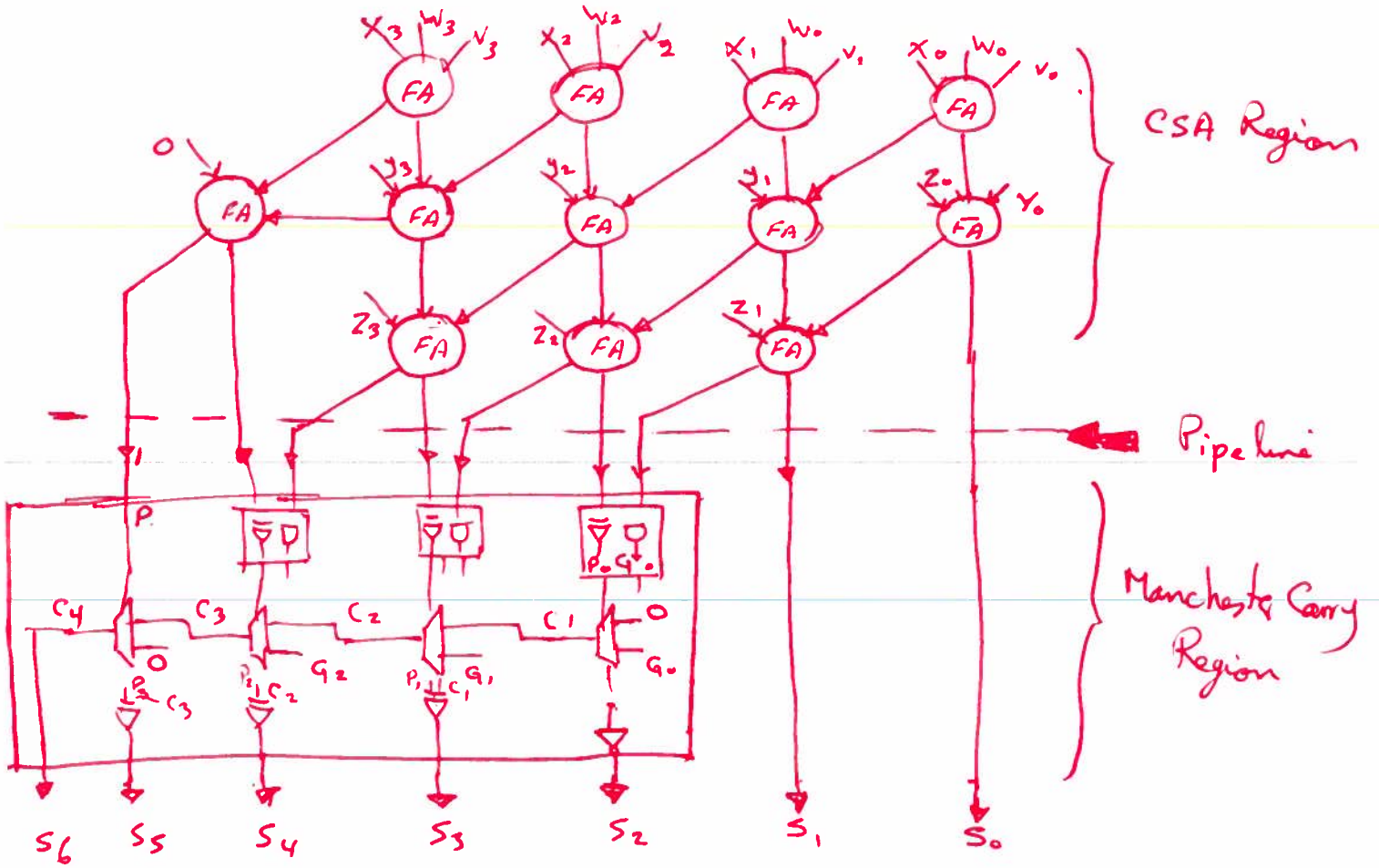

b) Delay = 3D + 0.25D + 4 * 0.5D + 0.25 = 5.5D
CSA PG MUXs XOR

Area = 12A + 10 * 0.25A + 5 * 0.5A = 17A
FA Gates Muxes

c) When we insert the pipeline, the Combinational logic is broken into 2 parts

First part will be the CSA = 3D

Second " " " Manchest = 4 * 0.5D + 0.25D + 0.25D = 2.5D

Second part is less than the first part delay wise so

T = 1.5D + 3D + D = 5.5
T_{cq} CSA t_{su}

Delay is not improved yet, the area is increased by 9 FF.

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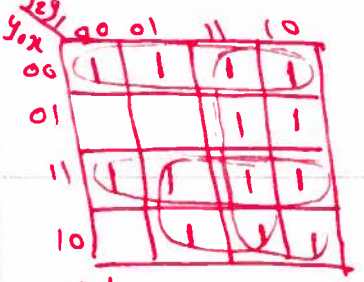
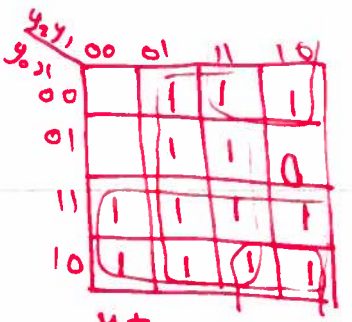
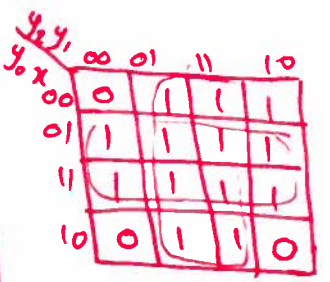
min term	Present State y_2	y_1	y_0	x	Next State y_2^+	y_1^+	y_0^+	output z
0	0	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	1	0
3	0	0	1	1	1	0	0	0
4	0	1	0	0	0	0	1	0
5	0	1	0	1	0	1	1	0
6	0	1	1	0	1	0	0	0
7	0	1	1	1	1	1	0	1
8	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	0
10	1	0	1	0	0	0	0	0
11	1	0	1	1	0	0	0	1
12	1	1	0	0	0	0	0	0
13	1	1	0	1	0	0	0	1
14	1	1	1	0	0	0	0	0
15	1	1	1	1	0	0	0	1



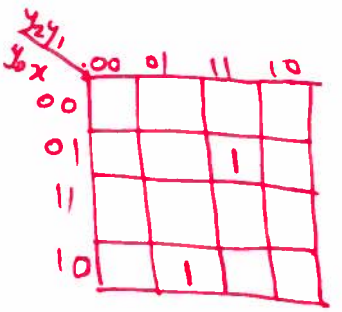
$y_2^+ = y_2 + \bar{y}_0\bar{x} + y_0x + y_1y_0$



$y_1^+ = y_1 + y_0 + y_2\bar{x}$

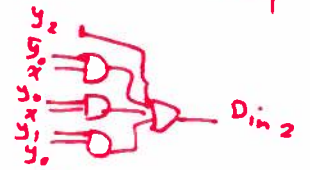


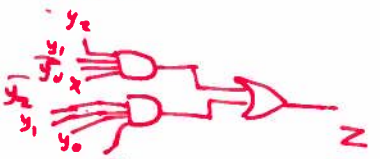
$y_0^+ = y_1 + x + y_2\bar{y}_0$

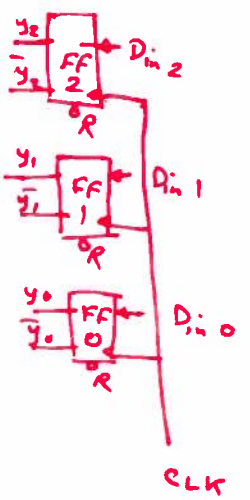


$z = y_2y_1\bar{y}_0x + \bar{y}_2y_1y_0\bar{x}$

Using D Flip Flop $y^+ = D_{in}$







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a) ③ Bias $= 2^{n-1} - 1 = 2^{5-1} - 1 = 15$

$A = 0.25_{10} = 0.01_2 = 1.0 * 2^{-2}$

$B = 10_{10} = 1010.0_2 = 1.010\ 2^3$

$e_A = 15 - 2 = 13_{10} = 1101_2$

$e_B = 15 + 3 = 18_{10} = 10010_2$

Representation:

A → 0 | 01101 | 0000000000

B → 1 | 10010 | 0100000000

b) ③

A+B exp2 − exp1 = 3 − (−2) = 5 shift A 5 places to the right

B is −ve Complement it 01.01000 2's Complement

$$\begin{array}{r} 110.10111 \\ .00001 \\ \hline 110.11000 \end{array} +1$$

−B →

Now add A+B

$$\begin{array}{r} 110.11000 \\ .00001 \\ \hline 110.11001 \end{array}$$

−ve number Complement & add 1

$$\begin{array}{r} 001.00110 \\ \hline 1.00111 \end{array} * 2^3 = 1001.11_2 = 9.75$$

A+B

1 | 10010 | 0011100000

② c) We round the numbers if R(M0+S) is true. this translate to the following table

Number	rounded	error	Number	Rounded	error
X0.00	X0.	0	X1.00	X1	0
X0.01	X0.	−1/4	X1.01	X1	−1/4
X0.10	X0.	−1/2	X1.10	X1+1	+1/2
X0.11	X1	+1/4	X1.11	X1+1	+1/4

This gives zero error assuming there are equal even and odd numbers

d) ② check notes: