CDEN 6501 Final 2018

Question 1

a) There are 6 errors as follows:

L1 entity demo is remove ;

L2 missing ;

L3 missing ; and Vector out1 : out std_logic_Vector ;

L8

L9 missing process before a case statement

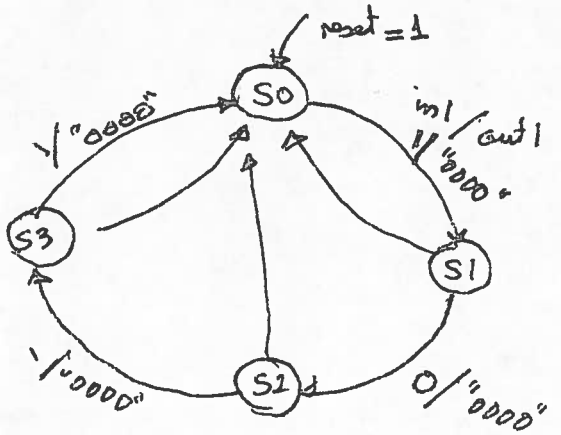
Line 19 remove end if

b) This is a finite state machine

There are 4 states : S0, S1, S2, S3

Reset = 1 system starts at S0

Depending on in1 input the next state is decided upon rising edge of the clock



## Q2

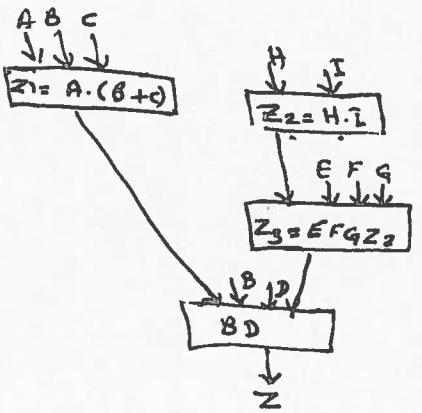
a) Three most common logic implementation in FPGAs are

Look up Tables - SRAM and EPROM - 2-1 MUX

the look up table using memory and 2-1 MUX is a convient way of applying any function. The 2-1 MUX is simple and fast needing 2 Transistors and one inverter. It can implement any logic gates required.

b)

i)




4 Variable LUT

Total Area

4 Variable LUT requires $2^4 - 1$ 2→1 MUX

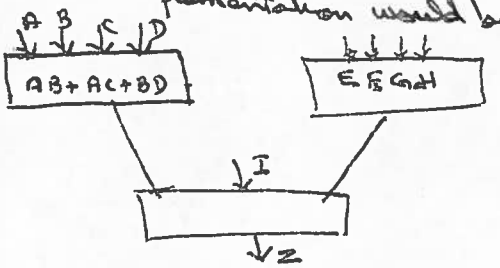
* Area = $4(2^4 - 1) = \underline{60}$ 2-1 MUX

Delay

4 Variable LUT has 4 2-1 MUX delay

* $3 * 4 = \underline{12}$ 2-1 MUX delay

ii) A better Implementation would be * 4 Variable LUT

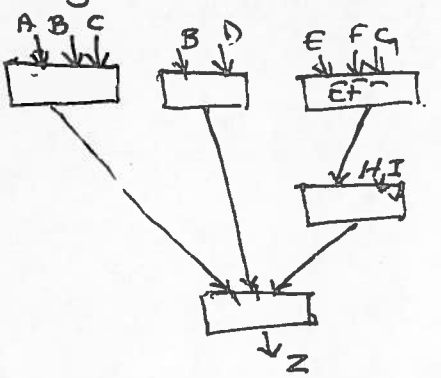



Area $3 * 2^4 - 1 = 45$ MUX delay

Depth $2 * 4 = 8$ MUX speed

iii) 3 Variable LUT

Using a 3 Variable LUT




Area = $5 * 2^3 - 1 = \underline{35}$ 2-1 MUX delay

Delay = $3 * 3 = 9$ 2-1 MUX delay

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Q 3

a) Advantage of Booth Algorithm is many folds including:
applicable to sign & unsigned number multiplication.
It reduces the number of rows to be added, hence

b) 20 = 0010100 −20 = 1101100 −40 = 1101 1000
15 = 001111 −25 = 110001 −30 = 1100010

−20 1101100
15 001111

−0
0 0 1 1 1 1 0
+1 −1

−1 * 20
0000 00101100
0000000000
1101100
Result 1101101 0100 A negative number = 0 0 1 0 0 1 0 1 1 0 0 =

So the results is 0 0 1 0 0 1 0 1 1 0 0 = −300

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
1 0 1 1 0 1 0 1 0 0 No. adders are needed

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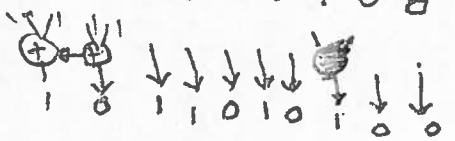
b) If we take 15 as the multiplicant then

−20 1101100 adding "0"

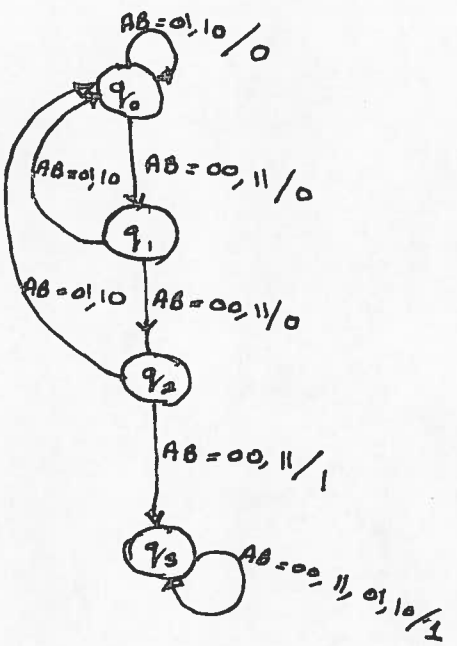
"0" 0000000000000
"−15" 1111 1 0001
"−15" 1110001
Result ⟹ 1 1 1 0 1 1 0 1 0 1 0 0 taking the Complement of the number
0 0 0 1 0 0 1 0 1 1 0 0 = 300

−1
1 1 0 1 1 0 0 0
−1 0



## Q4

State Diagram




Transition Table

| $y_1y_0$ \ AB | Next States 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 01 | 00 | 01 | 00 |
| 01 | 10 | 00 | 10 | 00 |
| 11 | 11 | 11 | 11 | 11 |
| 10 | 11 | 00 | 11 | 00 |

| $y_1y_0$ \ AB | output 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 0 |

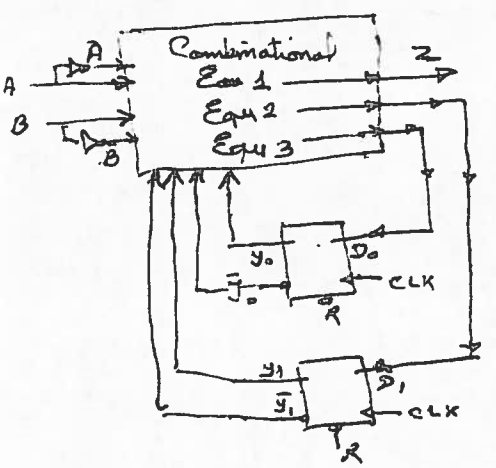
$$Z = y_1y_0 + y_1\bar{y}_0(A \odot B) \quad \text{Equ 1}$$

| $y_1y_0$ \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 |

$$y_1 = y_1y_0 + (A \odot B)(y_1 \oplus y_0) \quad \text{Equ 2}$$

| $y_1y_0$ \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 |

$$y_0 = y_1y_0 + (A \odot B)(y_1 \odot y_0) \quad \text{Equ 3}$$



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## Q5

Given information

Cycle $T = 20\,ns$, Clock skew $\alpha = 2\,ns$, FF $t_{cq} = 6\,ns$, $t_{su} = 4\,ns$, $t_h = 2\,ns$

gate delays: NAND 0.2 ns, Inverter 0.15 ns, XOR 0.3 ns, MUX 0.4 ns

d)

| Node | Arrival time (ns) | Required Time (ns) | Slack (ns) |
|---|---|---|---|
| a | 6 | 17.3 | 11.3 |
| b | 6 | 17.1 | 11.1 |
| c | 6 | 16.95 | 10.95 |
| d | 6.05 | 17.6 | 10.95 |
| e | 7.05 | 18 | 10.95 |
| f | 8 | 16 | 8 |
| g | 8 | 15.45 | 7.45 |
| h | 8.55 | 16 | 7.45 |

There is no problems as all slacks are +ve.

b) Maximum speed of operation

$T_{max} = t_{cq} + t_{comb} + t_{su} - t_{cs} = 6 + (0.15 + 0.2 + 0.3 + 0.4) + 4 - 2 = 9.05\,ns$ 1.05

$or.\ f = \frac{1000}{9.05}$ MHz

c) If the clock skew is $-7\,ns$

Then the signal at e will arrive at 7.05 the Required time now changes to

$T - t_{su} - t_{skew} = 20 - 4 + (-7) = 9\,ns$

There will be no problem as data will arrive at 7.05 ns and there will be a slack of $9 - 7.05 = 1.95\,ns$

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## Q6

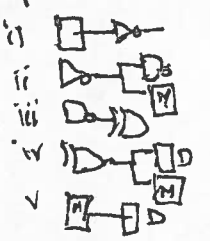
a) There are 5 Paths in this circuit

i) $Q_1$ X M $Q_4$, ii) $Q_2$ N X M $Q_4$, iii) $Q_4$ M $I_2$ $Q_1$, iv) $Q_5$ $Q_3$ and finally

v) $Q_3$ $I_1$ N X M $Q_4$ ← This path clearly is the critical path.

delay of this path in ns:

| | fo | |
|---|---|---|
| i) FF | 1 * 0.2 + 1 * 0.15 | 0.35 |
| ii) INV | 2 * 0.1 + 0.08 (2.5+1.5) + 0.15 | 0.67 |
| iii) NAND | 1 * 0.12 + 2 * 0.1 + 0.2 | 0.52 |
| iv) XOR | 2 * 0.13 + 0.12 (1.5+2) + 0.3 | 0.98 |
| v) MUX | 1 * 0.15 + 2 * 0.14 + 0.4 | 0.83 |
| | | 3.35 ns |




Total delay 0.7 + 3.35 = 4.05

Frequency of operation $= \frac{1}{4.05+0.5} = \frac{1000}{4.55}$ MHz

b)

$W = \frac{T_J - T_a}{\theta}$ ... $T_J = 40 * 1.5 + 70 = 130°C$ $\quad J = 403°K$

$K_T = \frac{T_J}{T_a} = \left(\frac{403}{70+273}\right)^{1.5}$ $\quad K_T = 1.27$

$K_p = (1 + 0.01 * 30) = 1.3$

$K_V = \frac{1}{(1 - 0.01 * 10)} = 1.11$

$K = K_t K_p K_V = 1.27 \times 1.3 * 1.11 = 1.83$

Total delay = 4.55 * 1.83 = 8.32 ns

Maximum speed $\frac{1}{8.32} = 120.2$ MHz