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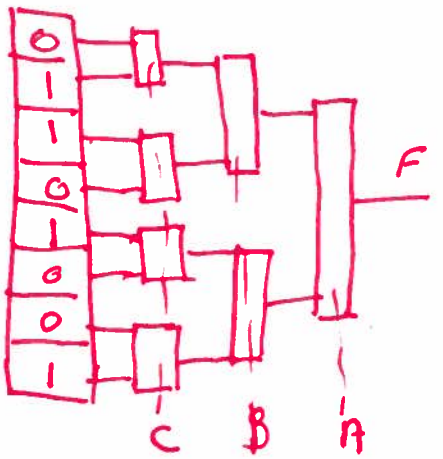
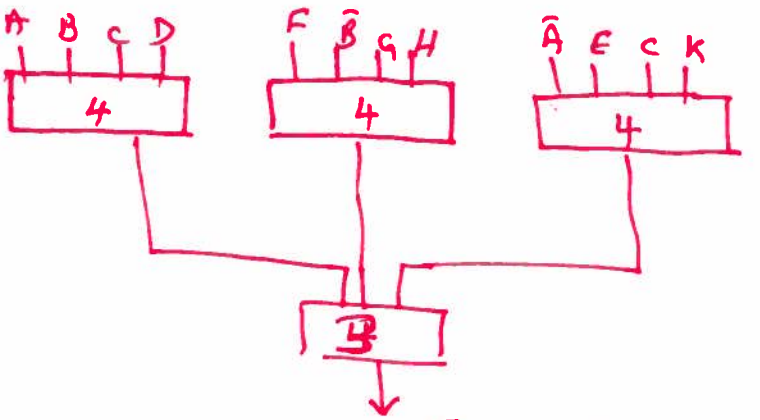
Question 1

a) $F(A,B,C) = \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C = \Sigma m(1,2,4,7)$



b)



16*3 + 8 = 56 bits storage

$3 * 2^4_{-1} + 1\,2^3$ Muxes

(4)+(3) Mux Delay

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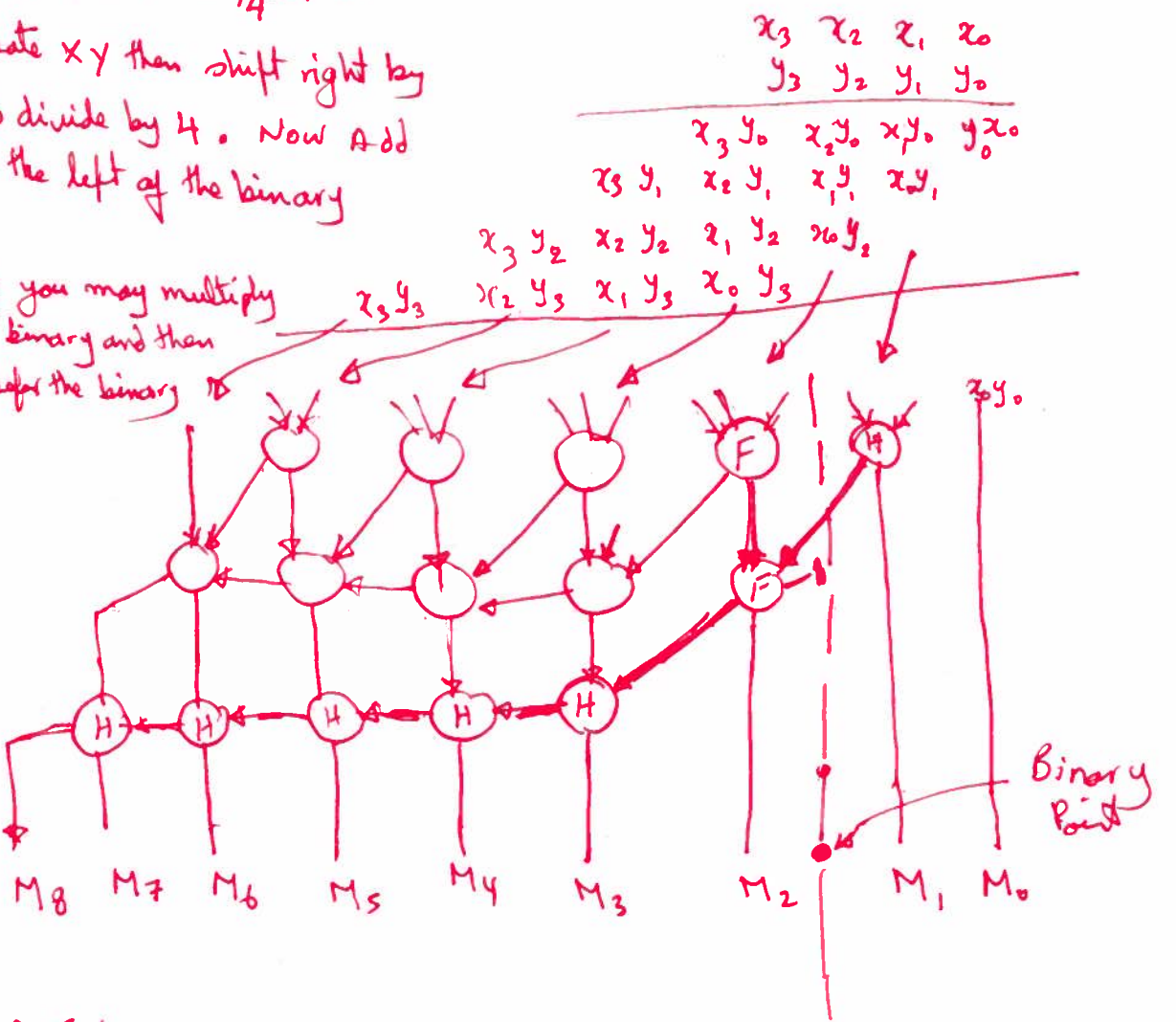
$Z = 0.25XY + 1 = \frac{1}{4}XY + 1$

First Evaluate XY then shift right by 2 places to divide by 4. Now Add the '1' to the left of the binary Point.

Alternatively you may multiply XY by 0.01 binary and then add the 1 befor the binary Point



Area 9 Full Adders + 16 AND gate

Delay 2 Full Adder + 5 Half Adder delay + AND gate delay

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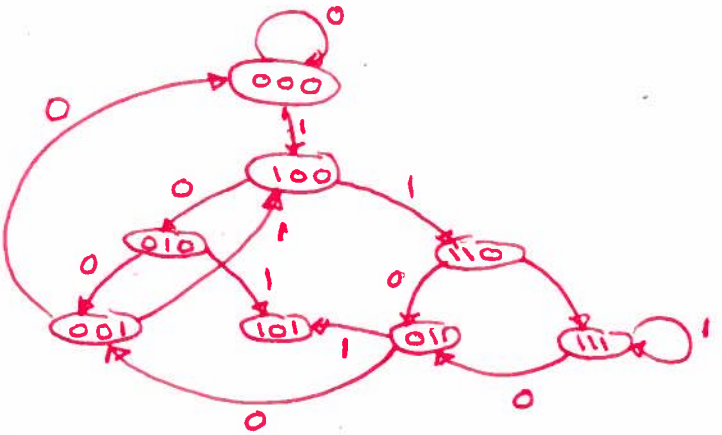
Question 3



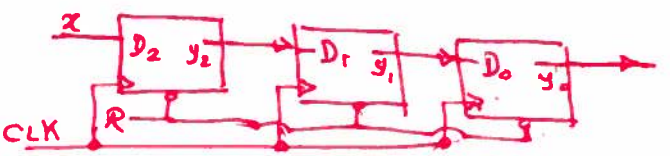
Present state			Next state					
			x=0			x=1		
y_2	y_1	y_0	y_0^+	y_1^+	y_2^+	y_2^+	y_1^+	y_0^+
0	0	0	0	0	0	1	0	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	1	0	1
0	1	1	0	0	1	1	0	1
1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	1	0
1	1	0	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1

From the Transition Table

$y_2^+ = x = D_2$

$y_1^+ = y_2 = D_1$

$y_0^+ = y_1 = D_0$



Question 4

a) There are 3 paths: Path 1 $U_4 \rightarrow U_3 \rightarrow U_5$
Path 2 $U_5 \rightarrow U_2 \rightarrow U_4$
Path 3 $U_5 \rightarrow U_4$

b) Evaluating the paths, path 3 can be neglected

$\tau = \tau_{CQ} + \tau_{CL} + \tau_{SU}$

For path 1 $\tau_1 = 1.5 + 0.15(2) + 0.2 \times 2 + 0.2 + 0.05(2+1) + 0.14 \times 2 + 1 = 3.83$ ns

Path 2 $\tau_2 = 1.5 + 0.15(1.5+2) + 0.2 \times 2 + 0.4 + 0.12 \times 2 + 0.18 + 1 = 4.24$ ns

So path 2 is the critical path $\tau_{max} = 4.245$

$f_{max} = 236$ MHz

c) For K input of FF-U_5 the path is path 1 $U_4 \rightarrow U_3 \rightarrow U_5$

Set up time slack = $T_{required} - T_{arrival}$

$T_{required} = T_{max} - T_{SU} = 4.245 - 1 = 3.245$ ns

$T_{arrival} = \tau_{CQ} + \tau_{CL} = 1.5 + 0.15 \times 2 + 0.2 \times 2 + 0.2 + 0.05(2+1) + 0.14 \times 2$

$= 2.83$ ns

$T_{set\ up\ slack} = 3.245 - 2.83 = 0.415$ ns

or $= 0.615$ if fan out output neglected

hold time slack = $\tau_{arrival} - \tau_{hold} = 2.83 - 0.5 = 2.33$

or $= 2.13$

if fan out of output is neglected

No violation

Q5

a) Two paths D4 – U3 – D5
D5 – U2 – D4

Path 1 . 2 + 0.45 * 3 + 0.4 + 0.35 * 4 = 5.15 ns
Path 2 . 2 + 0.45 * 1 + 0.2 + 0.15 * 4 = 3.25 ns

Arrival at Point F = Delay of D4 = $t_{CQ} + t_{CL}$ + Fanout = 3.35

Required time at A = 20 ns – t_{su} – Delay of U3
= 20 – 1 ns – 1.8 ns = 17.20 ns

Slack time @ F = 17.20 – 3.35 = 13.85 ns

b) Path 1 is the critical path D4 – U3 – D5

$T_{i\,max} = T_{CL} + T_{CL} + T_{CQ} = 5.15 + 1 = 6.15$ ns

Temp effect, $k_t = \left(\frac{T_J - 25^\circ C}{30^\circ C/W}\right)^{-M} = \left(\frac{273+70}{273+25}\right) = \left(\frac{343}{298}\right)^{1.5} = 1.235$

Voltage effect $k_v = \frac{1}{1-0.05} = 1.0526$

$K = k_t * k_v = 1.235 * 1.0526 \simeq 1.3$

overall Delay = $K \times T_{i\,max} = 1.3 * 6.15 \simeq 8$ ns

worst case frequency, $f = \frac{1}{8\,ns} = 125$ MHz

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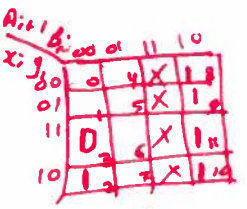
Question 6 P1

Assume the following decoding

x	y	
0	0	x = y
0	1	y > x
1	0	x > y
1	1	X

Than

	A_{i+1}	B_{i+1}	x_i	y_i	A_i	B_i
0	0	0	0	0	0	1
1	0	0	0	1	0	0
2	0	0	1	0	1	0
3	0	0	1	1	0	0
4	0	1	0	0	0	1
5	0	1	0	1	0	1
6	0	1	1	0	1	0
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	0	1
10	1	0	1	0	1	0
11	1	0	1	1	0	0
12	1	1	0	0	0	1
13	1	1	0	1	0	1
14	1	1	1	0	1	0
15	1	1	1	1	X	0



$A_i = A_{i+1} + \bar{B}_{i+1} x \bar{y}$

$B_i = B_{i+1} + \bar{A}_{i+1} \bar{x} y$

Now that we have the Boolean expression for A_i & B_i we can proceed and the VHDL code for the bit comparator and the easiest would be a behavioral description.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL ; -- other use statements of STD library if needed
entity Component_1 is
Port (Ain, Bin, x, y: in std_logic; Ao, Bo: out std_logic);
end Component_1
architecture behavioral of Component_1 is
begin process (Ain, Bin, x, y)
    begin if (Ain ='1' and Bin ='0') than Ao<='1'; Bo<='0';
    elsif (Ain ='0' and Bin ='1' than Ao<='0' Bo<='1';
    elsif (x='1' and y='1' than Ao<='0' Bo<='0';
    else Ao<=x ; Bo<=y
    end if;
    end process;
    end behavioral;
```

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Question 6 - Continued P2

```
-- library statements here ..

entity Componant_8 is
    Port (Ain, Bin : in std_logic;
          x, y : in std_Logic_Vector 7 downto 0); Ao, Bo : out std_logic);
end Componant_8;

architecture structural of Componant_8 is
  Componant_1
  Port (Ain, Bin, x, y : in std_logic; Ao, Bo: out std_logic);
  end Componant_1
  signal sa, sb : std_logic_vector (7 downto 0);
begin
  for com7 : comparator_1 use entity work comparator_1 (behavioral);
      comp7: Comparator_1 Portmap (Ain, Bin, x(7), y(7), sa(7), sb(7));
  for comp6-1 : Comparator_1 use entity work. comparator_1 (behavioral);
  stages: for i in 6 downto 1 generate
      comp6-1 : comparator_1 portmap (sa(i+1), sb(i+1), x(i), y(i), sa(i), sb(i));
  end generate;
      Comp 0 : Comparator_1 Portmap (sa(1), sb(1), x(0), y(0), Ao, Bo);
  end structural;
```