ECE 4170

Quiz I
February 20th, 2007

1. The Georgia Tech Honor Code governs this examination. Please note you are not to discuss this examination with anyone. Your signature below attests to the same.
2. There are 4 questions. Make sure you have all of them.
3. Please write/draw **legibly**.
4. State any assumptions you feel you have to make or ask for clarification
5. Keep in mind it is difficult to give partial credit without written material. Please make sure you document any partial solutions.
6. **The points are shown next to each problem. Plan your work!**
7. I will be available most if not all of Wednesday. Contact me if you have any questions or just come by**.**
8. Turn in your exam as follows.
    a. The answers to questions 2-4 should be in separate directories.
    b. One text (e.g., Word) file with answers to each question
    c. One zip file of all of the directories.
    d. Email time stamped by 7:30pm February 21st.
    e. No late submissions will be accepted.

Problem	Max Points	Graded
1	15	
2	15	
3	25	
4	45	
Total	100	

Student Name: _____

Student Number: _____

I have neither received nor given assistance on this examination.

_____

Signature

Question 1

1. Why are the concepts of delta events and delta delays necessary for the correct discrete event simulation of circuits? Provide simple example to explain the problem delta delay models solve.
2. When would you use a configuration specification vs. a configuration declaration?
3. In evaluating the speed of simulation models, should you be sensitive to the number of transactions that the model generates, the number of events the model generates, or does it matter? Provide a short justification for your answer.

Question 2

Construct a VHDL model that generates the following signals.

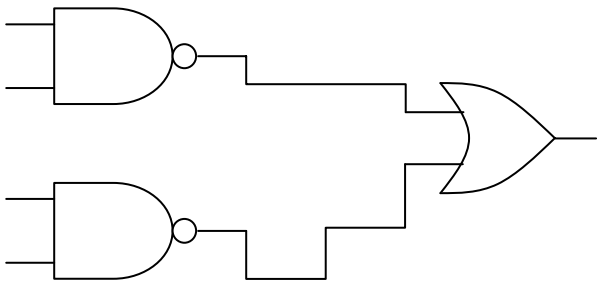
1. A 10 ns reset pulse: reset is '1' for 10 ns and '0' thereafter
2. Two phase non-overlapping clocks with a duty cycle of 25% and a period of 20 ns.

Print and attach the trace.

Question 3

Write a VHDL model of the following circuit that has the following characteristics.

1. Each gate has a delay of 10 ns.
2. Each wire, including wires from input ports to the gate inputs and from gate outputs to output ports, have a delay of 4ns.
3. The input signals are sequences of pulses with pulse widths of no more than 6 ns.
4. No pulses are rejected by the circuit elements. The effects of all input signals are propagated to the output.



Attach a trace to demonstrate the correct functioning of the circuit.

Question 4 (Read the whole question carefully before starting)

Using **only two input NAND gates**, construct and simulate a parametric VHDL model of register file comprised of 32, 32-bit registers, with two read ports and 1 write port. The gate delay and width of the register file should be specified as part of the register file interface. The register file entity should be as shown below (`rwe` is the read/write enable signal where `rwe` = '1' signifies as write operation.)

Construct a behavioral model of a register that is parametric in delay and width.

Provide a configuration declaration for the register file. Show how the configuration declaration would be modified to generate a simulation of the register file that uses this behavioral register model rather that the complete structural hierarchy down to gates. *This should involve no changes to the architecture of the register file*! The only file that must be changed is the configuration declaration.