3200DX Quadrant Clocks

The need for high-drive signals in large Field Programmable Gate Arrays (FPGAs) is clear. As FPGA devices continue to increase in size, the demand for high-drive signals used for clocking and resets will continue to rise. Applications with multiple clocks, enables, and resets often can use a few more high-drive lines than the FPGAs offer, and using regular routed signals for these applications can mean higher skew and lower predictability. However, the impact on the FPGA die area has always been a significant roadblock to providing a large number of high-drive signals. Actel's ACT 2 family provides two global clocks that can be used for high-drive signals. The 3200DX builds upon that base by offering four additional quadrant clocks at minimal die cost. This document details the architecture and usability of the 3200DX quadrant clocks. For more information on other 3200DX features, such as SRAM blocks, and Wide Decode modules, refer to *Actel's FPGA Application Guides*.

Clock Networks

High-drive signals create a dilemma for the routing resources of FPGAs—the higher the fanout on an ordinary net, the more skew between its destination points. In addition, the higher fanout on a net can cause the net to be slower. To remedy this situation, Actel FPGAs (specifically 3200DX devices) provide global clock networks within chips. These networks are high-speed, low-skew routes dedicated to providing suitable paths for high-speed clocks. The global clock networks can be accessed internally (CLKINT macro) or externally through CLKA and CLKB pins.

As FPGA applications become larger and more complicated, more high-drive signals are implemented within the FPGAs. In addition to one or two high-speed global clocks, there might be two or three more local clocks in need of low-skew paths. Furthermore, there are often reset or enable lines with high fanouts that could use dedicated circuitry to avoid deep buffer trees. These high-drive signals are ideal for the new quadrant clock buffers. Quadrant clocks can also be accessed internally or through external pins. Table 1 summarizes the 3200DX devices and their special features, including the quadrant clocks.

How to Use the Quadrant Clocks

The quadrant clock modules are accessed through library elements similar to those of traditional clock buffers in the ACT 2 and 3200DX families. Figure 2 shows the two new library elements available to capture the quadrant clocks, as well as the existing clock buffers used to capture global clocks. The quadrant clocks can be used for signals with high fanout. If the fanout on the signal driven by the quadrant clock exceeds the quadrant limits, two or more of them can be grouped together to cover the load. The grouping process can be done automatically or manually.

Table 1 • *3200DX Family*

	3265DX	32100DX	32140DX	32200DX	32300DX
Gates	6,503	9,240	14,210	20,140	30,735
Global Clocks	2	2	2	2	2
Quadrant Clocks	0	4	0	4	4
I/O MAX	126	152	176	202	250
Wide Decode Cells	20	20	24	24	28
JTAG	No	Yes	Yes	Yes	Yes
SRAM bits	0	2,048	0	2,560	3,072

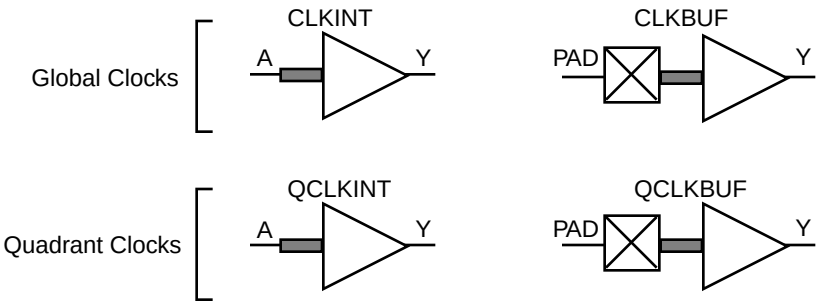

Figure 1 • *Global and Quadrant Clock Library Elements*