Axcelerator Development System

User's Guide

Windows®

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Introduction

The Axcelerator Development System is a platform for demonstrating and evaluating the unique capabilities of Actel's new Axcelerator family of FPGAs. The Axcelerator Development System provides you with a hardware platform for evaluating and exercising Axcelerator features such as PLLs, LVDS I/Os, PerPin FIFOs, Block RAMs, etc. The hardware platform also enables you to build systems using your own special requirements to test your FPGA design. This User's Guide is designed to help you take full advantage of the Axcelerator Development System's capabilities.

Document Organization

This guide provides detailed information and step-by-step instructions for the Axcelerator Development System.

The Axcelerator Development System User's Guide is divided into the following chapters:

Chapter 1 - Development System Description contains a detailed overview of the Axcelerator Development System.

Chapter 2 - System Operation describes software installation and Axcelerator Development System setup.

Chapter 3- Hardware Interfaces contains detailed information about the Axcelerator motherboard.

Appendix A - Representative HyperTerminal Connection Log provides the log file from a HyperTerminal Connection.

Appendix B- FPGA Pin Definition lists pin definition tables.

Appendix C- Product Support describes our support services.

Development System Content

The Axcelerator Development System includes the following:

- AX1000_FG896 based Axcelerator motherboard
- PowerQUICC II Processor Module
- LVDS loop-back board
- Optional LVDS backplane
- Power supply

- Axcelerator Development System CD ROM
- 9-pin RS-232 extension cable
- CAT5 standard and crossover Ethernet cables

CAUTION:

The Axcelerator Development System contains components that are sensitive to static electricity. You must only use the Axcelerator Development System in a static-safe environment.

The Axcelerator Development System is shipped with a programmed AX1000 FPGA that is used to demonstrate the Axcelerator FPGA capabilities. The programmed FPGA includes PowerQUICC II and DDR memory interfaces, LVDS, standard I/O, 10/100 Ethernet and Gigabit Ethernet loop-back interfaces, PLL-based clock generation, and Silicon Explorer II interface. The Axcelerator Development System is shipped with the programming file, not the netlist design file.

WARNING:

The Axcelerator Development System AX1000 FPGA is installed in a mechanically secured socket. When you install an AX1000 FPGA, you must line up the A1 ball with the A1 arrow designation on the board and use the appropriate torque screwdriver (specified by the socket manufacturer) or you may damage the system.

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System Description

You can use the Axcelerator Development System as a standalone demonstration platform or as a development platform to evaluate a custom Axcelerator-based design. A block diagram of the Axcelerator Development System is shown in Figure 1-1.

The Axcelerator motherboard includes a socketed Axcelerator FPGA with PowerQUICC II, DDR SDRAM, Hex 10/100 and Gigabit Ethernet, internal standard I/O loop-back, external LVDS loop-back, and Silicon Explorer II interfaces. The motherboard also includes power regulation, clock generation, power-up and push button reset, configuration jumpers/switches, LED indicators, and a user prototyping area.

The PowerQUICC II Processor Module is used as a control processor for controlling and monitoring the demonstration tests. The processor module includes the PowerQUICC II processor, Flash, SDRAM, a 10/100 Ethernet interface, two RS-232 interfaces, a COP port, and an ATM interface. The processor module controls the Axcelerator motherboard through an interface to the Axcelerator FPGA. The Axcelerator motherboard Hex 10/100 and Gigabit Ethernet interfaces are also controlled by the processor module through MDIO interfaces. The PowerQUICC II Processor Module connects to the Axcelerator motherboard via three PCI Mezzanine Card-type connectors.

The Axcelerator Development System application software runs on a host PC (connected to the development system via a 10/100 Ethernet link). The application software controls the demonstration tests through a graphical user interface.

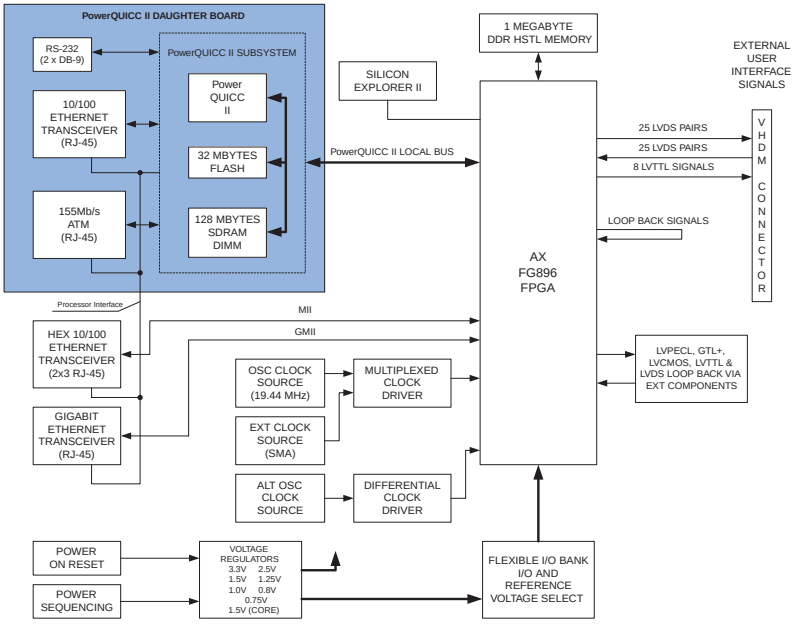

Figure 1-1. Axcelerator Development System Block Diagram

Axcelerator Motherboard

The Axcelerator motherboard is shipped with an AX1000 FPGA installed. The FPGA includes PowerQUICC II, DDR SDRAM, Hex 10/100 and Gigabit Ethernet, internal standard I/O loop-back, external LVDS loop-back, and Silicon Explorer II interfaces. The Axcelerator motherboard includes:

- PowerQUICC II Processor Module connectors
- One megabyte of DDR SDRAM (HSTL interface to FPGA)
- On-board standard I/O loop-back components for LVPECL, GTL+, LVCMOS and LVDS
- High-speed VHDM connector (external LVDS loop-back)
- Gigabit Ethernet Phy
- Hex 10/100 Base-T Ethernet Phy

- Silicon Explorer II connector

PowerQUICC II Processor Module Interface

The PowerQUICC II interface provides a communications link between the FPGA design and the PowerQUICC II control processor. The interface consists of the following:

- Synchronous 66 MHz 32-bit data bus
- 18-bit address bus
- 10 control signals

The interface uses the PowerQUICC II UPM. Several spare PowerQUICC II I/Os and interrupts are also provided for user expansion. The PowerQUICC II Processor Module is used as a control processor for controlling and monitoring the demonstration tests.

An additional interface to the PowerQUICC II is provided via the 802.3 MDIO interface bus. This is a two wire serial interface that configures the 10/100 Base-T and Gigabit Ethernet Phys.

DDR Memory

The DDR memory is implemented using a Micron MT57W2MH8CF with separate HSTL 1.5 volt I/O (SIO) double data rate (DDR) SDRAM. The DDR memory clock operates at 155.52 MHz (311.04 Mbits/second data rate).

The interface signals include the following:

- 19 Bit address
- 4 Bit synchronous data input
- 4 Bit synchronous data output
- Data load
- Data read/write
- Clocks

One megabyte of this memory is available on the Axcelerator Development System. The DDR memory demonstrates HSTL I/O compatibility and FPGA performance.

Standard I/O Loop-Back Components

The Axcelerator motherboard includes several standard I/O interface devices to demonstrate compatibility with the I/O standards. The I/O standards demonstrated are:

- LVDS (six pairs)
- LVPECL (2 pairs)
- GTL+ (two signals)
- LVCMOS (one signal)

The LVDS compatibility is demonstrated using a National DS90CP22. The LVPECL compatibility is demonstrated using On Semi's MC100EPT22 and MC100EPT23. The GTL+ compatibility is demonstrated using Philips' GTL2005 and GTLP2T152. The LVCMOS compatibility is demonstrated using two TI SN74AUC1G04 devices.

Bank 7 of the Axcelerator FPGA contains the GTL and LVCMOS devices and is by default configured to operate at 1.5 volts with a 1.0-volt Vref. The standard I/O loop-back interface operates at 97.2 MHz.

Bank 7 of the Axcelerator FPGA has jumper selection capabilities to allow the bank I/O voltages to be: 3.3, 2.5, 1.8, or 1.5 volts. The Vref for bank 7 is jumper selectable to allow for the following Vrefs: HSTL_I (0.75 volt), SSTL_II (1.25 volt) and GTL+ (1.0 volt). Jumper P3 selects the Vref and P4 selects the I/O voltage.

CAUTION:

Do not apply 3.3 volts to the SN74AUC1G04 LVCMOS devices. Remove these devices prior to configuring Bank 7 for 3.3 volts.

High-speed VHDM Connector

The Axcelerator motherboard provides a high-speed Teradyne VHDM connector for LVDS loop-back demonstration or user expansion. There are 25 LVDS output pairs from the FPGA to the connector, 25 LVDS input pairs from the connector to the FPGA, and 8 LVTTL signals between the connector and the FPGA. The standard FPGA shipped with the system, when coupled with the LVDS loop-back board (the system is shipped with the loop-back board installed), demonstrates the external loop-back of 311 Mbit/second LVDS signaling.

The optional LVDS backplane can also be used to connect two Axcelerator Development Systems together and demonstrate system data transfer (board-

to-board) using 311 Mbit/second LVDS signaling. The LVDS loop-back board and LVDS backplane utilize 25 LVDS loop-back pairs (it connects the 25 output pairs to the 25 input pairs of the FPGA) and 4 LVTTL loop-back signals.

The VHDM connector is a controlled impedance connector capable of low GHz performance. The Axcelerator motherboard VHDM connector pinout is provided in chapter 3 of this user's guide.

Gigabit Ethernet

The Gigabit Ethernet circuit is based on the LXT1000. The LXT1000 is connected to the Axcelerator FPGA via a standard 125 MHz GMII interface. The external interface to the LXT1000 is through a copper interface (RJ-45).

The default Ethernet address is sensed on power up through the address selection pins using LEDs. Upon power up, with reset active, the address selection pins are sensed as either a high or low to determine the Ethernet address. A sense of high or low is determined by LEDs connections- either to power or ground through a current limiting resistor.

After power up, the pins either source or sink current to provide the desired LED operation. The default Gigabit Ethernet PHY address, for the Axcelerator Development System, is configured on power up as address = 0. External dipswitches provide configuration control for the Gigabit Ethernet. The exact function of each switch setting is outlined in the "Switch Location/ Function" section. The LXT1000 is under software control via the MDIO interface.

CAUTION:

The Gigabit Ethernet Phy (U26- LXT 1000) dissipates 6 watts when active (S2-1 off and data is being transferred through J18), and can be extremely hot. The regulator (U23) supplying power to the LXT1000 can also be extremely hot when the Gigabit Phy is active. DO NOT TOUCH the U26 or U23 under these operating conditions.

Hex 10/100 Base-T Ethernet

The Hex 10/100 Ethernet circuit is based on the LXT9763. The LXT9763 is connected to the Axcelerator FPGA via six independent standard MII interfaces. The external interface to the LXT9763 is through six RJ-45 connectors (stacked 3 wide by 2 high).

The default operation is sensed on power up through the mode selection pins using LEDs. Upon power up, with reset active, the mode selection pins are sensed as either a high or low to determine the default operation. A sense of high or low is determined by the LEDs connections - either to power or ground through a current limiting resistor.

After power up, the pins will either source or sink current to provide the desired LED operation. The default operation of the Hex Ethernet, for the Axcelerator Development System, is 10/100 Auto-negotiation mode. The default Hex Ethernet PHY address, for the Axcelerator Development System, is hard wired to address = 2. The LXT9763 is under software control via the MDIO interface.

Silicon Explorer II

The Silicon Explorer II Interface consists of a standard JTAG interface and four probe pins. A standard Silicon Explorer 8x2 (0.1" center) header is used for all connections except PRC and PRD. An additional header, the 3x1 (0.1" center) header, is provided for PRC and PRD.

Clocking

The Axcelerator motherboard FPGA has two clock frequencies, 19.44 MHz and 66 MHz. Multiples of the 19.44 MHz, generated using the internal FPGA PLLs, are used for the DDR memory interface, the standard I/O loop-back, and LVDS loop-back. The PowerQUICC II interface uses 66 MHz. An SMA connector and spare oscillator slot are also available for user-defined clocks. (See Figure 1-2 below).

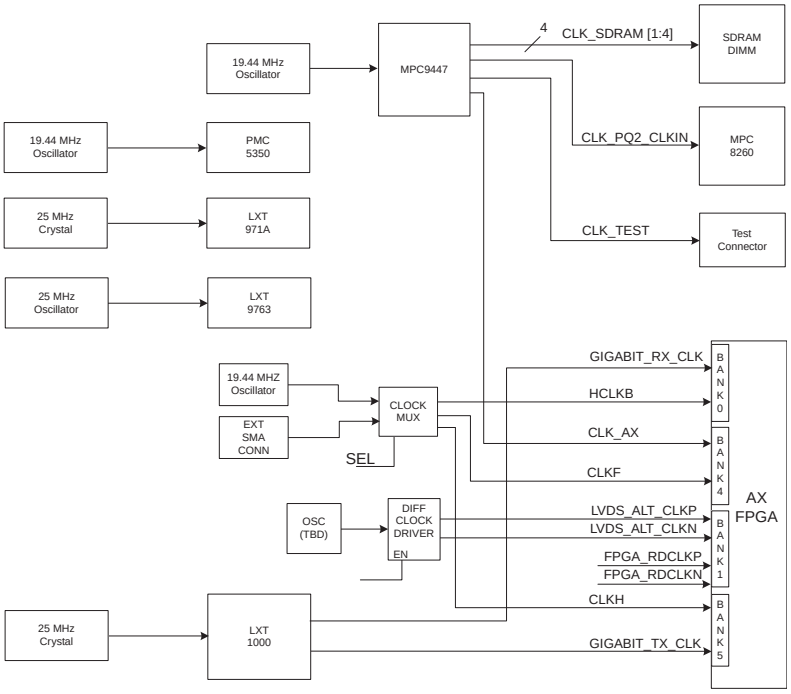

Figure 1-2. Axcelerator Development System Clock Diagram

There are several other independent clock sources on the system. These clocks are used for the Ethernet and ATM interfaces.

Reset

The Axcelerator motherboard has a push button reset (S1) that resets only motherboard devices. The PowerQUICC II Processor Module has a push button reset (S1) that resets both the PowerQUICC II Processor Module and the Axcelerator motherboard. See Figure 1-3 for the Axcelerator Development System reset distribution.

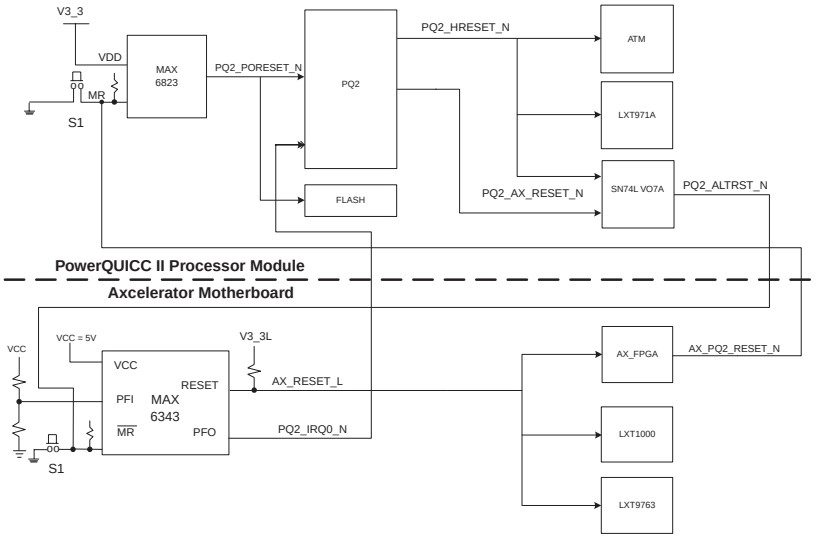

Figure 1-3. Axcelerator Development System Reset Distribution

Power Regulation

The Axcelerator Development System draws power from a single external 5 volt power brick. The 5 volt source supplies a 3.3 volt switching power regulator, a 3.3 volt linear regulator, a 2.5 volt linear regulator and the PowerQUICC II Processor Module ATM interface device. The 3.3 volt switcher is used to power a 1.5 volt linear regulator for the FPGA core, a 1.8 volt linear regulator, a 1.5 volt linear regulator, and the 0.75 volt HSTL termination voltage. The 3.3 volt switcher is also used as the main source of power for the PowerQUICC II Processor Module. See Figure 1-4 for the Axcelerator Development System power distribution.

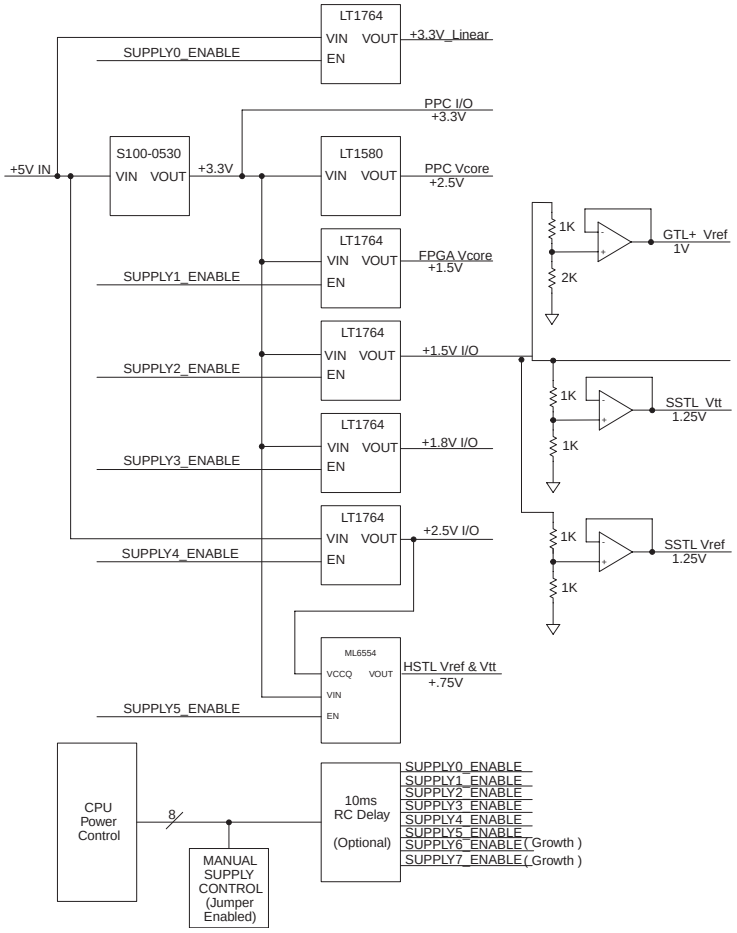

Figure 1-4. Axcelerator Development System Power Distribution

User Prototyping Area

The Axcelerator motherboard contains a user prototyping area with a 14 by 19 grid of holes (0.1 inch by 0.1 inch spacing). The holes can accept standard 0.025" square pins.

PowerQUICC II Daughter Board

The PowerQUICC II daughter board contains a complete PowerQUICC II processor subsystem including memory, voltage regulation, and control logic required for processor operation in addition to standard I/O interfaces. The software running on the PowerQUICC II configures the devices on the motherboard and provides the user interface for selecting and running tests. The key features of the PowerQUICC II daughter board are:

- Motorola PowerQUICC II processor operating at 200 MHz
- 128Mb SDRAM DIMM for program and data operation
- 32Mb Flash memory for code and constant storage
- 10/100 Ethernet interface utilizing an Intel LXT971A Phy
- Two serial ports
- Standard COP interface and Mictor connectors for software debug
- Mezzanine connectors used to connect with the motherboard
- 155Mb/S ATM interface, for future utilization, implemented using a PMC5350

Note: The Mezzanine connectors provide the required signals to interface with the motherboard components and the Axcelerator FPGA. The key interfaces provided by the daughter board connectors are the daughter board power, PowerQUICC II local bus, MDIO signals to provide the management interface for IEEE 802.3 devices, and general purpose I/O signals.

LVDS Loop-Back Board

The LVDS loop-back board is included with the standard Axcelerator Development System. The system is shipped with the loop-back board installed (it connects to the VHDM connector - J17). The loop-back board is used to demonstrate external loop-back of 311 Mbit/second LVDS signaling. The LVDS loop-back board utilizes 25 LVDS loop-back pairs (it connects the 25 output pairs to the 25 input pairs of the FPGA) and 4 LVTTL loop-back signals. Figure 1-5 shows a block diagram for the loop-back board connections.

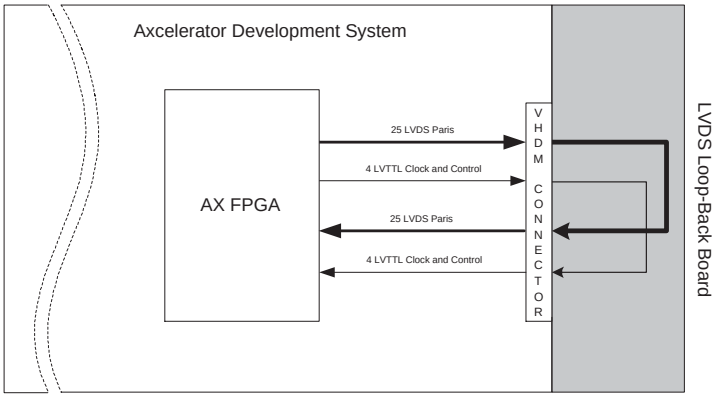

Figure 1-5. Axcelerator Development System Loop-Back Connections

LVDS Backplane Board

The LVDS backplane board is an optional Axcelerator Development System accessory. The LVDS backplane board can be used to connect two Axcelerator Development Systems together (J17 to J17) or an Axcelerator Development System and a user system. The LVDS backplane board is used to demonstrate system data transfer (board-to-board) using 311 Mbit/second LVDS signaling. The LVDS loop-back board utilizes 25 LVDS loop-back pairs (it connects the 25 output pairs of one board to 25 input pairs of a second board and vice-versa) and 4 LVTTL loop-back signals. See Figure 1-6 for the Axcelerator Development System backplane Connections.

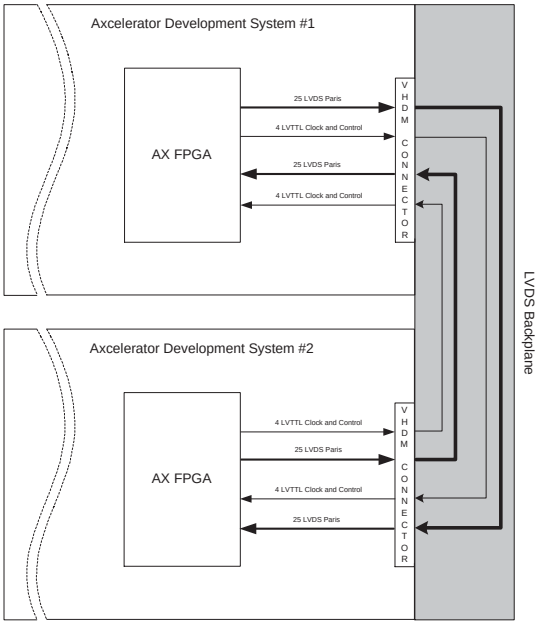

Figure 1-6. Axcelerator Development System Backplane Connections

Software

The Axcelerator Development System includes two software elements: software programmed into Flash on the PowerQUICC II Processor Module, and software installed on your host (PC). The software application uses a client/server architecture. The Windows-based client (host) application runs on a PC with a graphical user interface. The PowerQUICC II Processor Module software is a standalone boot application with an embedded server application running under the embedded Linux OS. The host and server applications communicate via a 10/100 Ethernet connection. The Axcelerator Development System is shipped with the PowerQUICC II Processor Module software pre-programmed into the on-board Flash.

Boot Software

The boot code resides in Flash on the PowerQUICC II Processor Module. The boot code is the initial code that executes on power-up or reset. The code performs basic PowerQUICC II Processor Module tests (quick SDRAM test), major component status, presence of motherboard, and reads the FPGA configuration registers. Code execution passes from boot to POST or from the operating system based on your input and/or switch settings.

POST Software

The POST code resides in Flash on the PowerQUICC II Processor Module. The POST code provides a menu driven diagnostic interface that operates via an RS-232 interface on the PowerQUICC II Processor Module.

Embedded Linux Operating System

The Axcelerator Development System uses an embedded Linux Operating System and device drivers to control and monitor the demonstration tests. The Linux Operating System code resides in Flash on the PowerQUICC II Processor Module. The Linux Operating System also includes a session logging interface (via an RS-232 interface on the PowerQUICC II Processor Module) that provides diagnostic and debug information. The session interface also enables you to set the Axcelerator Development System IP address during the Linux Operating System boot process. See "IP Address Configuration".

Application Server

The Axcelerator Development System application server is a standalone process that is controlled by the Linux Operating System. The server provides a command/response messaging interface for communications with the client software via Unix sockets. The server receives messages from the client software and dispatches commands/tests to the hardware via device drivers. The server is defined with a generic interface, which allows the addition of new user interface features without requiring Flash software updates.

Application Client

The Axcelerator Development System application client is a PC-based Windows application that is installed on the user's PC. The client communicates with server process via a 10/100 Base-T Ethernet interface. The client software provides the user with a graphical interface to configure the Axcelerator Development System and run pre-defined demonstration tests.

2

System Operation

This chapter describes system requirements, software installation, and Axcelerator Development System setup.

Platform Support

The Axcelerator Development System supports the following platforms:

- Windows 98
- Windows NT
- Windows 2000
- Windows XP

System Requirements

The Axcelerator Development System software requires the following:

- 300MHz Pentium or greater
- 32 MB RAM
- 5 MB available hard disk space (100 MB included support files and documentation)
- CD ROM drive

Software Installation

Using the Axcelerator Development System requires an available host PC for the application software.

To install the software:

1. **Insert the Axcelerator Development System CD ROM.**
2. **From the CD ROM, double click on the Setup.exe file.**
3. **Follow any installation procedures.**

Axcelerator Development System Setup

CAUTION:

The Axcelerator Development System contains components that are sensitive to static electricity. You must only use the Axcelerator Development System in a static-safe environment.

To setup the Axcelerator Development System:

1. **Remove the Axcelerator Development System using static safe procedures.**
2. **Make sure the Axcelerator motherboard power switch (S5) is turned off.**

CAUTION: Do not apply power to the system before installing the SDRAM.

3. **Install the SDRAM DIMM in the PowerQUICC II Processor Module DIMM socket.**
4. **Verify that the Axcelerator Development System switches and jumpers are correctly configured in their default settings.**

WARNING: The Axcelerator Development System AX1000 FPGA is installed in a mechanically secured socket. When installing an AX1000 FPGA, use the appropriate torque screwdriver, specified by the socket manufacturer, or you could damage the system.

Connecting to the System

The system can be used as a directly connect network resource.

To connect the system:

1. **Connect the Axcelerator Development System power supply to J19.**
2. **If you want to use the system as a directly connected resource, connect the crossover CAT5 Ethernet cable from the host PC to J8 on the PowerQUICC II Processor Module.**

3. **If you want to use the system as a network resource, connect the standard CAT5 Ethernet cable from the network to J8 on the PowerQUICC II Processor Module.**

4. **Connect the 9-pin RS-232 extension cable between the host PC COM port and J14 on the PowerQUICC II Processor Module.** During the first-time use of the Axcelerator Development System, you must have the RS-232 cable connected to the system. After you configure the system (i.e., the IP address has been set), the RS-232 cable is no longer required and the host PC RS-232 port can be used for Silicon Explorer.

   Proper communication between the Axcelerator Development System and the host PC requires that you configure the host PC properly.

   Note: You must assign a fixed IP address to the host PC. Using a PC configured to use a Dynamic Host Configuration Protocol (DHCP), or similar method of assigning a dynamic IP address upon connection, may prevent the host PC from properly communicating with the Axcelerator Development System.

Configuring the HyperTerminal

A HyperTerminal gathers user input and provides operational status information. A representative log file from a HyperTerminal connection, captured during start-up of the system, is provided in Appendix A. The required configuration for the HyperTerminal is shown below.

Note: There are several different types and versions of HyperTerminal; therefore, the method for configuring the terminal may be different from system to system.

To configure the HyperTerminal:

1. **From the host PC control panel or hardware device manager, Select Port (properties), Port Settings Advanced, and click Disable the Use FIFO buffer.**

2. **Start the HyperTerminal application.** From the *Start* menu, point to *Programs*, *Accessories*, *Communications*, and click *HyperTerminal*, as shown in Figure 2-1.

Figure 2-1. Starting the HyperTerminal Application

The HyperTerminal window displays, as shown in Figure 2-2.

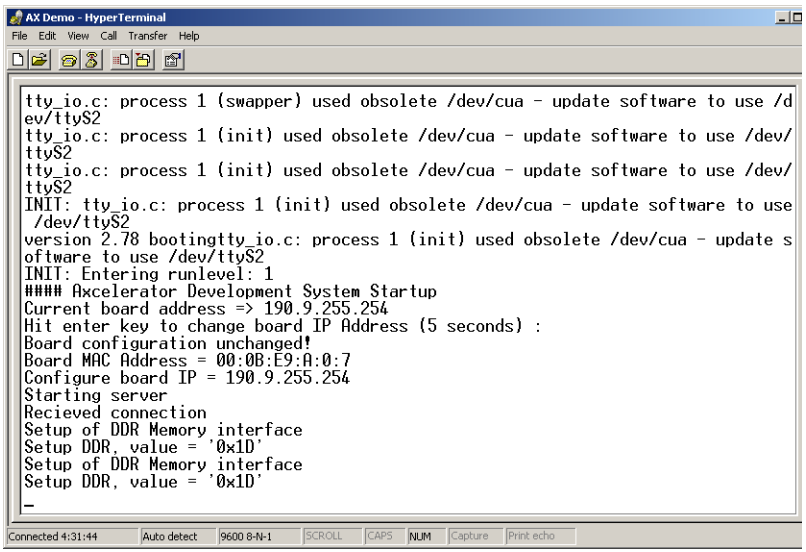

Figure 2-2. HyperTerminal Window

3. Set the connection to the proper COM port.

4. **Configure the terminal as follows: Bits per second - 9600, Data bits - 8, Parity - None, Stop bits - 1, Flow control - None.**

Note: Do not send line ends with line feeds and do not echo typed characters locally. The above settings are for configuring the board only. When you enter post, change these settings to Send line ends with line feeds and Echo typed characters locally.

System Start Up

To start the system, launch the application software on the host PC. (From the Start menu, select *Programs*, *Actel*, and click on *AX Demo Control*). See Figure 2-3.

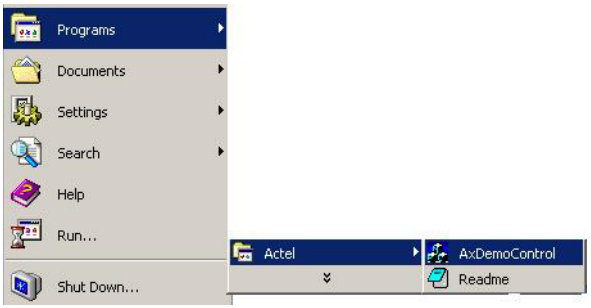

Figure 2-3. Starting the Axcelerator Development System Software

The Axcelerator Development System window displays. See Figure 2-4.

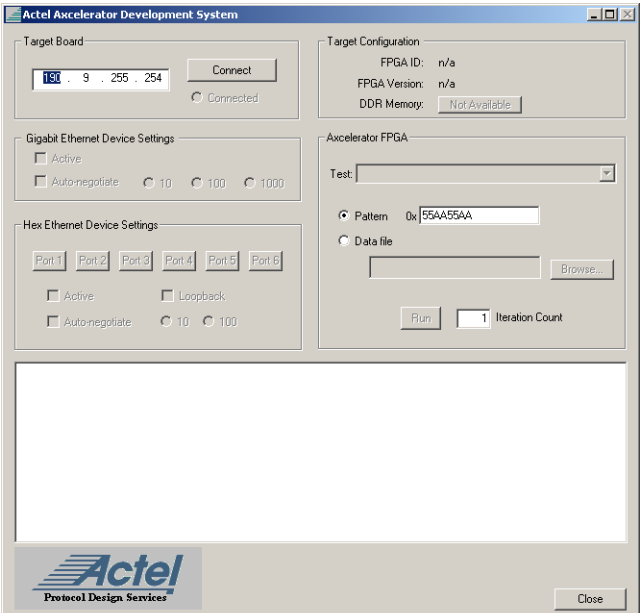

Figure 2-4. Axcelerator Development System Window

Note: The host PC HyperTerminal should have an active connection.

Power-On

Power on the Axcelerator Development System by turning on the power switch (S5). Once on, D34 on the motherboard illuminates. During power-up, the motherboard LED displays the following:

- The Hex 10/100 Ethernet LEDs (D16 - D33) flashes once unless the associated Ethernet RJ-45 (J1) jacks are connected to an active Ethernet network.
- The FPGA PLL lock indicators (D1 - D8) turn on.
- The Gigabit Ethernet LEDs (D9 - D14) are off, but D13 may randomly flash on from time-to-time.

See Table 2-1 for LED behavior when connected to an active network.

Table 2-1. Hex Ethernet LED Behavior

Port	100 Base-T Connection	Link Present	Activity
1	D16 On	D17 On	D18 On
2	D19 On	D20 On	D21 On
3	D22 On	D23 On	D24 On
4	D25 On	D26 On	D27 On
5	D28 On	D29 On	D30 On
6	D31 On	D32 On	D33 On

See Figure 2-5 for J1 port destinations.

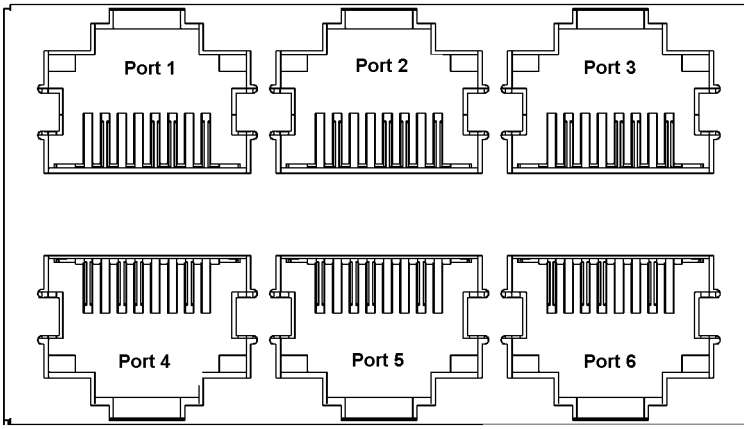

Figure 2-5. J1 Port Designations

During power-up, the Power QUICC II Processor Module LED displays the following:

- D1 - D8, on the PowerQUICC II Processor Module, blinks 5 times

(approximately 1/3 second on then 1/3 second off).

- D1 and D2 remain on.
- D3 is on if POST is entered.
- D4 is on once the operating system has booted.
- D9 flashes periodically if the Ethernet RJ-45 (J8) connector is connected to an active Ethernet network.
- The green LED on J8 is on if an Ethernet link is present on J8.
- The Yellow LED on J8 is on if a 100 Base-T Ethernet connection is present on J8.
- D10 is on unless a cable is plugged into J17.

Power-On Configuration

Power-on configuration requires an active HyperTerminal connection.

IP Address Configuration

You can modify the IP address of the Axcelerator Development System during the boot process. As the system is booting, the boot progress reports in the HyperTerminal window.

To modify the IP address during the boot process:

1. **When prompted, press the Enter key to change the board IP address.** You have approximately five seconds to press the Enter key to modify the IP address, if not, you skip the modifying process. See Figure 2-6.

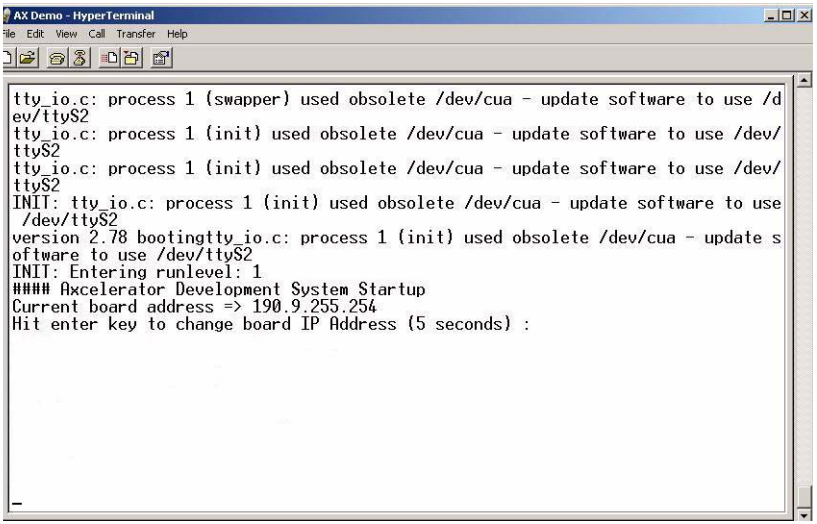

Figure 2-6. HyperTerminal Window for IP Address Modification

2. When prompted, enter the new IP address.

Note: The system is typically shipped with a default address of 10.20.81.170 or 10.20.81.171.

Diagnostic Interface

The RS-232 interface provides a diagnostic interface that is available when the HyperTerminal connection is active. During the boot process, the boot messages prompt you to: Hit any key to enter POST menu. The POST menu offers several options, as follows:

- Peek/Poke Menu
- Axcelerator FPGA Menu
- MDIO Device Menu
- Power and Reset Menu
- ATM Config Menu
- Axcelerator Board Configuration Information

- Boot Operating System

  Note: These menu options provide additional diagnostic and configuration/control functions. However, these functions are beyond the scope of this user's guide.

System Demonstrations

The following section describes how to run the default demonstration tests provided with the Axcelerator Development System application software.

To run the system demonstration tests:

1. **Connect to the system.** Set the IP address (in the Axcelerator Development System window Target Board block) to the IP address assigned to the Axcelerator Development System. See Figure 2-7.

Figure 2-7. Connecting to the System

2. **Click the Connect button.** The application should connect to the board within a few seconds. Once connected, you can run the demonstration tests. See Figure 2-7.

DDR Memory Interface

To run the DDR Memory interface demonstration:

1. **Click on the Available button in the Target Configuration section of the main Axcelerator Development System window.** See Figure 2-8.

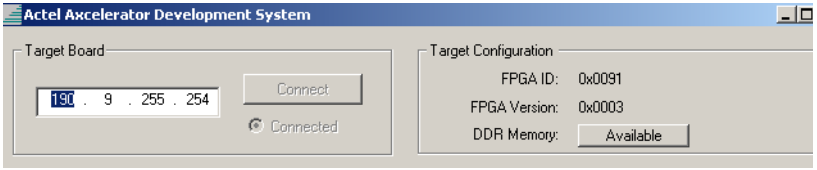

Figure 2-8. Running the DDR Memory Interface Demonstration

The DDR Memory window displays. See Figure 2-9.

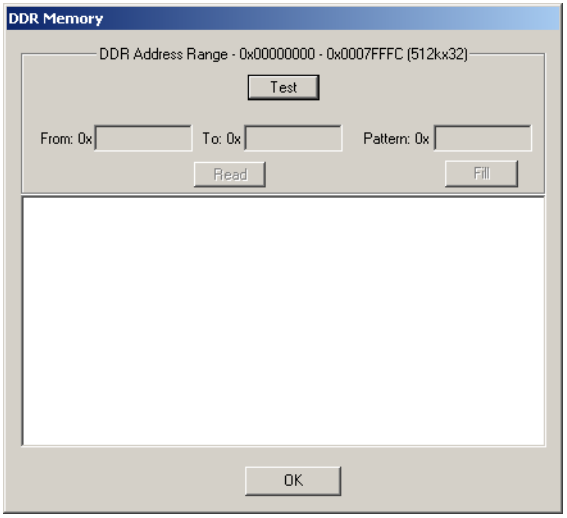

Figure 2-9. DDR Memory Window

2. Click the Test button.

The DDR Memory Test Passed window displays as shown in Figure 2-10.

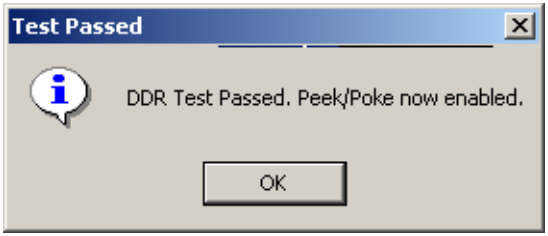

Figure 2-10. DDR Memory Test Passed Window

3. **Click OK.** The DDR interface calibrates and the other buttons are available to use. See Figure 2-11.

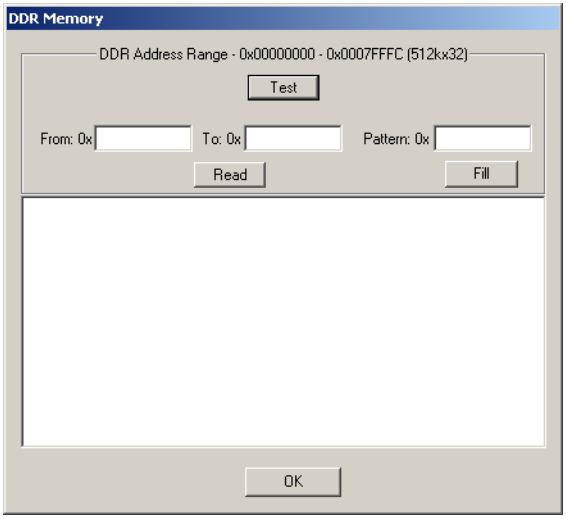

Figure 2-11. DDR Memory Active Window

You can use the DDR Memory window to read or fill memory. Use the "From" and "To" entries to complete the address range for the read or fill memory.

Note: The address range must be 32-bit aligned.

4. **If you click the Fill button, the specified pattern will write to the specified address range.**
5. **If you click the Read button, the data read from the specified address range dumps to the DDR Memory window.**

   A 32-bit (8 nibble) pattern must be specified for a fill operation. All values are entered in hexadecimal format.

   Note: The initial power-up tests use a data = address test format.

Internal Loop-back

To run the internal loop-back demonstration:

1. **From the Test selection bar in the Axcelerator Software window, select the On-board Standards Loop-Back Test.** See Figure 2-12.

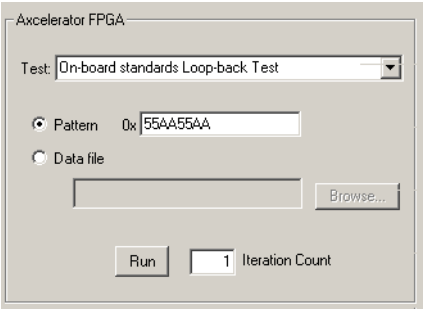

Figure 2-12. On-Board Standards Loop-Back Test

2. **If you use a fixed data pattern or ASCII text (data) file as the source test data, select the appropriate option the Axcelerator FPGA section.**

   Note: The pattern can be up to 16 nibbles of Hex data.

3. **If you want to select a data file, use the Browse button to find it.** The Iteration Count specifies the number of times the pattern or data file is transmitted (up to 99,999 times).
4. **Click Run to start the test.**

The status of the test is reported in the main application window as shown in Figure 2-13.

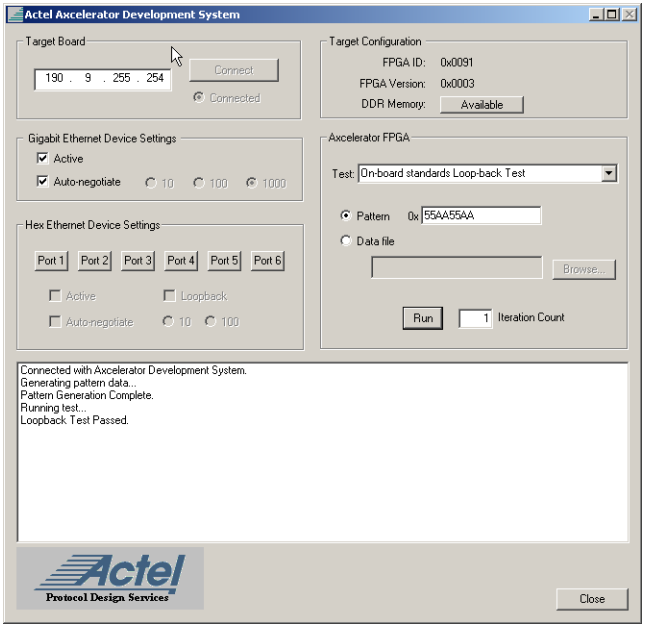

Figure 2-13. Test Status for Internal Loop-Back Demonstration

External Loop-Back

To run the external loop-back test:

1. **From the Test selection bar menu, select the External Loop-back Board/Backplane LVDS Loopback.** See Figure 2-14.

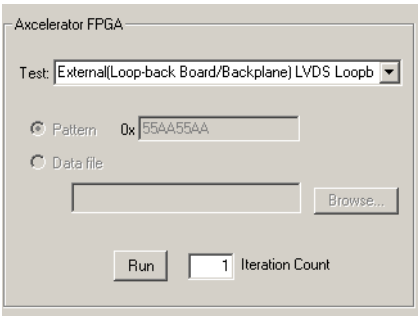

Figure 2-14. Running the External LoopBack Test

Note: You can use pseudo-random data or a fixed data pattern as the test data source.

The LVDS Board-Board Loopback Test window displays as shown in Figure 2-15.

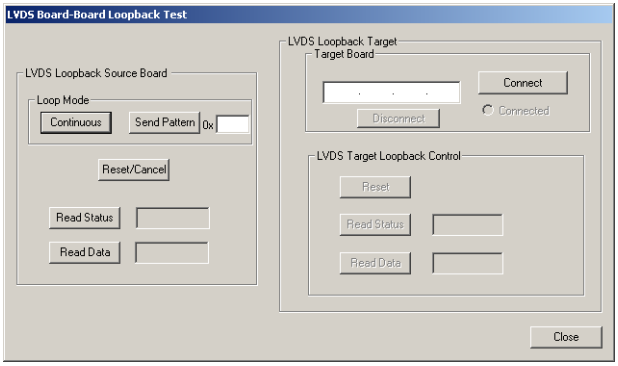

Figure 2-15. LVDS Board-Board Loopback Test Window

2. If you click the Continuous button in the LVDS Loopback Source Board portion of the LVDS Board-Board Loopback Test window, a Linear Feedback Shift Register (LFSR)

continuously generates pseudo-random data and transmits it to the VHDM connector.

3. **To terminate a continuous test, click the Reset/Cancel button.**
4. **Click the Send Pattern button.** The specified 16-bit pattern will be transmitted to the VHDM connector.

   The transmitted data is received by the FPGA.

5. **Click the Read Status button to determine the test status.**
6. **Click the Read Data button to read the received data.**

   A passing status is indicated by a Read Status of 0x0000FFFF. See Figure 2-16. A non-zero result in the first four nibbles or a zero in the last four nibbles indicates failure (e.g., 0x1000EFFF indicates a failure in bit 12).

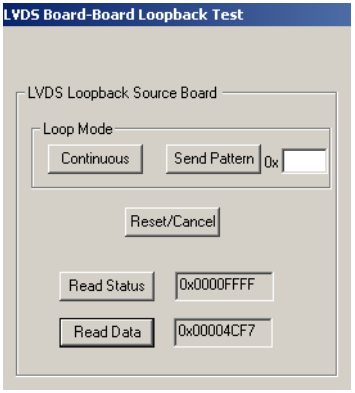

Figure 2-16. LVDS LoopBack Test Status

Note: The External Loop-Back Board (the Axcelerator Development System is shipped with this installed) must be installed for this test.

Backplane

The optionally available LVDS backplane board and a second Axcelerator Development System is required for this test. You must connect the two systems using the backplane prior to running this test. Use the backplane to

connect J17 (the VHDM connector) to one system and J17 on the other system.

To run the Backplane demonstration test:

1. **From the Test selection bar menu, select the External (Loop-back Board/Backplane) LVDS Loopback.** See Figure 2-17.

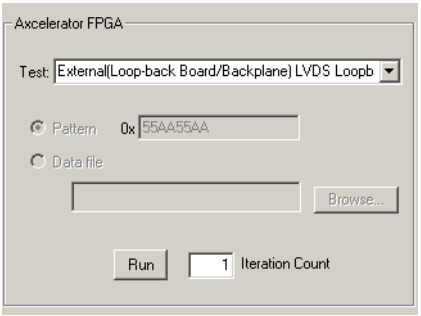

Figure 2-17. Running the Backplane Demonstration Test

2. **Click Run.** The LVDS Board-Board Loopback Test window displays as shown in Figure 2-18.

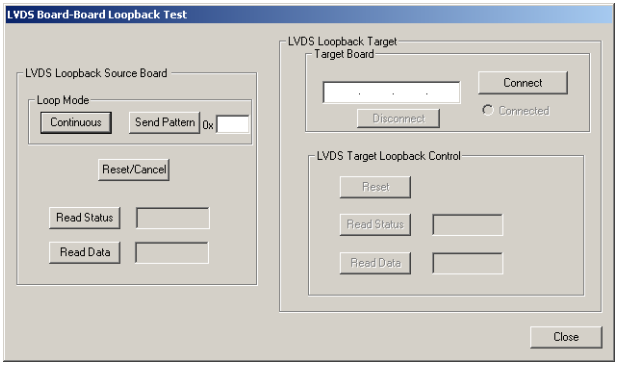

Figure 2-18. LVDS Board-Board Loopback Test Window

3. **Connect the target board (a second Axcelerator Development System).** Specify the IP address of the target bard in the LVDS Loopback Target block of the LVDS Board-Board Loopback Test window and click *Connect*. See Figure 2-19.

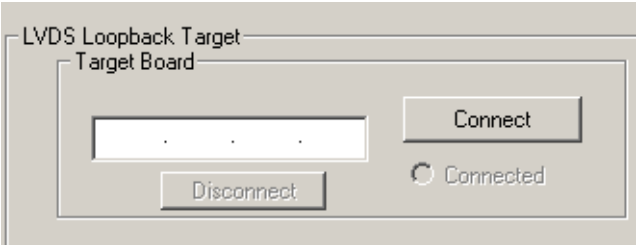

Figure 2-19. LVDS Loopback Target Box

Note: The IP address of the two boards must be different and unique to the network they are on.

You can use pseudo-random data or a fixed data pattern as the test data source.

4. **If you click the Continuous button in the LVDS Loopback Source Board portion of the LVDS Board-Board Loopback Test window, a Linear Feedback Shift Register (LFSR) continuously generates pseudo-random data and transmits it to the VHDM connector.** See Figure 2-16.
5. **To terminate a continuous test, click the Reset/Cancel button.** See Figure 2-16.
6. **Click the Send Pattern button.** The specified 16-bit pattern will be transmitted to the VHDM connector.

   The transmitted data is received by the FPGA.
7. **Click the on the Read Status button to determine the test status.**
8. **Click the Read Data button to read the received data.**

A passing status is indicated by a Read Status of 0x0000FFFF. A non-zero result in the first four nibbles or a zero in the last four nibbles indicates failure (e.g., 0x1000EFFF indicates a failure in bit 12).

Note: The External Loop-Back Board (the Axcelerator Development System is shipped with this installed) must be installed for this test.

Gigabit Ethernet Loop-back

To run the Gigabit Ethernet Loop-back test:

1. **Connect a Gigabit Ethernet source to J18 (on the motherboard).**
2. **Turn S2-1 (on the motherboard) off.** The Gigabit Ethernet data transmitted to the Axcelerator Development Board automatically loops back to J18.

CAUTION:

The Gigabit Ethernet Phy (U26- LXT1000) dissipates 6 watts when active (S2-1 off and data is being transferred through J18), and can be extremely hot. The regulator (U23) supplying power to the LXT1000 can also be extremely hot when the Gigabit Phy is active. DO NOT TOUCH the U26 or U23 under these operating conditions.

10/100 Ethernet Loop-back

To run the 10/100 Ethernet Loop-back demonstration test:

1. **Click the Port 2 button in the Hex Ethernet Device Settings block of the main Axcelerator Development System window.** See Figure 2-20.

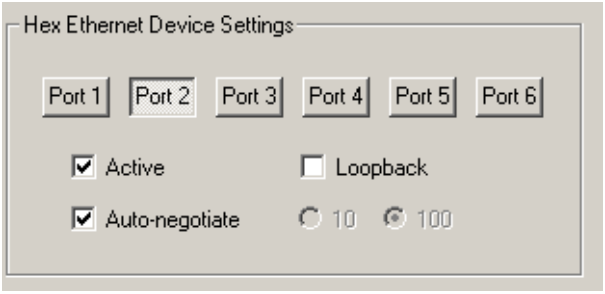

Figure 2-20. Hex Ethernet Device Settings

2. **Put Port 2 in loop-back by clicking on the loop-back check box for this port.** The port is set for Loopback mode. Leave other Port 2 settings in their default state (Auto-negotiate and Active). See Figure 2-21.

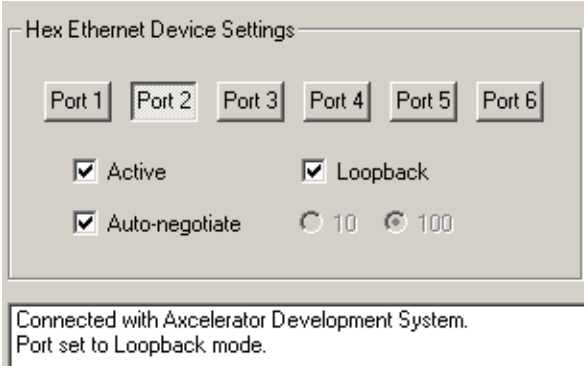

Figure 2-21. Port Set to LoopBack Mode Window

3. **Repeat the previous step for Ports 3, 4, and 5.**
4. **Insert one end of a crossover Ethernet patch cable (provided) into the upper-left port (Port 1) of the Hex Ethernet connector on the motherboard, and insert the other end into a network wall jack or Ethernet hub.**

5. **Insert one end of a straight-through Ethernet patch cable into the lower right port (Port 6) of the Hex Ethernet connector on the motherboard and, insert the other end into the Ethernet card of a PC.**

   Note: A web browser can be used on the PC to download a web page or ping can be used to verify connectivity between the PC and the network wall jack.

High-Speed Clock Output

A 311.04 MHz output clock from the FPGA is connected to the SMA connector J20 on the motherboard. This clock is generated from the 19.44 MHz input clock (from U12) using a PLL with a multiply by 16.

Note: This is a 50 ohm output.

Silicon Explorer II Interface

The Axcelerator FPGA Silicon Explorer II interface is connected to a standard Silicon Explorer 16-pin header and two additional single pin header connections. The connections are specified in Table 2-2.

Note: J16 is the connector adjacent to J20.

Table 2-2. Silicon Explorer Connections

Silicon Explorer Signal	Header Connection
PRB	J16-1
GND	J16-2
PRA	J16-3
GND	J16-4
VCC	J16-5
GND	J16-6
RSVD	J16-7
RSVD	J16-8
TMS	J16-9
MODE	J16-10
SDO	J16-11
RSVD	J16-12
DCLK	J16-13
RSVD	J16-14
SDI	J16-15
RSVD	J16-16
PRC	J2-1
PRD	J2-2

3

Hardware Interfaces

This chapter describes hardware interfaces for the Axcelerator Development Board System.

Axcelerator Motherboard

This section describes locations and functions of the motherboard.

Switch Location/ Function

The Axcelerator Development System motherboard switches are described in Table 3-1 and their locations are shown in Figure 3-1.

Table 3-1. Axcelerator Development System Motherboard Switch Definitions

Switch	Description	Switch On	Switch Off	Default Setting
S1	Reset	Reset system	Normal Operation	Off
S2(1)	Gigabit Ethernet Power Down Selector	Gigabit Ethernet disabled	Gigabit Ethernet enabled	On
S2(2)	Gigabit Ethernet Speed 2	Advertise 1000 Base-T during Auto-negotiation	Do not advertise 1000 Base-T during Auto negotiation	On
S2(3)	Gigabit Ethernet Speed 1	Advertise 100 Base-T during Auto-negotiation	Do not advertise 100 Base-T during Auto negotiation	On
S2(4)	Gigabit Ethernet Speed 0	Advertise 10 Base-T during Auto-negotiation	Do not advertise 10 Base-T during Auto negotiation	On
S3(1)	Gigabit Ethernet Auto-negotiation enable	Enabled	Disabled	On
S3(2)	Gigabit Ethernet Smart Speed enable	Enabled	Disabled	On
S3(3)	Gigabit Ethernet Pause mode	Enabled	Disabled	On

Switch	Description	Switch On	Switch Off	Default Setting
S3(4)	Giabit Ethernet Master/Slave configuration	Master	Slave	Off
S4(1)	Unused			
S4(2)	Gigabit Ethernet Auto-negotiate Isolation feature	Enabled	Disabled	On
S4(3)	Gigabit Ethernet 10 Mb/s link select	Serial Mode	MII mode	Off
S4(4)	Gigabit Ethernet TBI/GMII MAC configuration	TBI configuration	GMII configuration	Off
S5	Axcelerator Development System power switch	System powered	System off	Off

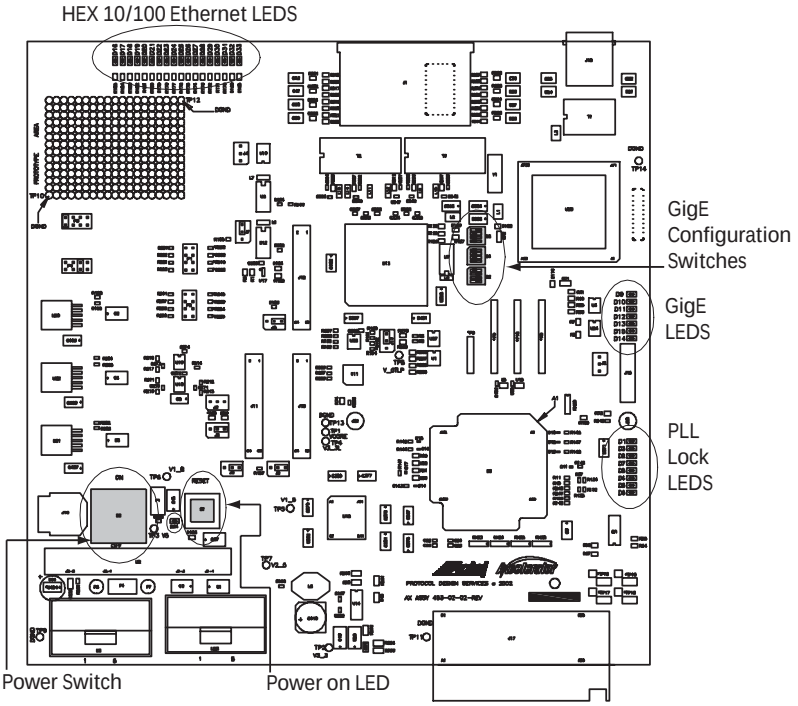

Figure 3-1. Axcelerator Development System Motherboard Switch and LED Locations

Configuration Jumpers Location/ Function

The Axcelerator Development System motherboard jumpers are described in Table 3-2, and their locations are shown in Figure 3-2.

Table 3-2. Axcelerator Development System Motherboard Jumper Definitions

Jumper Reference	Jumper Function	Default Location Pin-to-Pin
J3	JTAG TRST	Open
J4	Alternate JTAG from PQ2 interface	Open
J5	FPGA low power pin	Open
J6	FPGA Vpump control pin	2 to 3
J7	19.44 MHz Global Clock Enable	2 to 3
J8	Global Clock buffer mux selector	2 to 3
J9	DLL enable for DDR Memory	2 to 3
J13	Differential Clock buffer enable	2 to 3
P3	Bank 7 Voltage selector	1 to 8
P4	Bank & Voltage reference selector	3 to 6

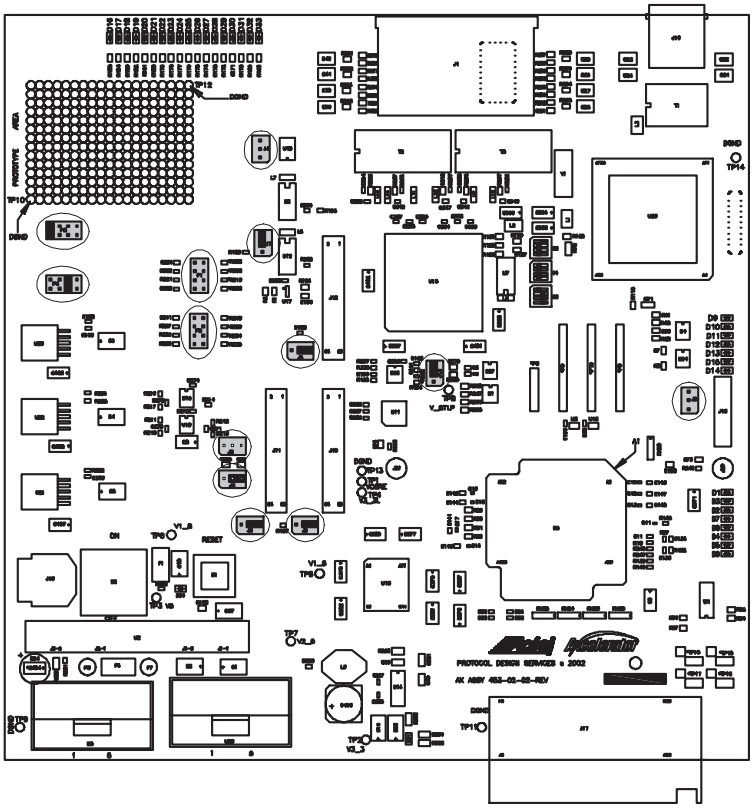

Figure 3-2. Axcelerator Development System Motherboard Jumper Locations

LEDs Location/ Function

This section describes the location and function of the LEDs.

PLL (General Purpose)

The Axcelerator Development System motherboard PLL (general purpose) LEDs are described in Table 3-3, and their locations are shown in Figure 3-1.

Table 3-3. Axcelerator Development System Motherboard PLL LED Definitions

LED	Definition for Active LED
D1	PLL H has lock
D2	PLL F has lock
D3	PLL G has lock
D4	PLL C has lock
D5	PLL B has lock
D6	PLL A has lock
D7	PLL E has lock
D8	PLL D has lock

Gigabit Ethernet

The Axcelerator Development System motherboard Gigabit Ethernet LEDs are described in Table 3-4, and their locations are shown in Figure 3-1.

Table 3-4. Axcelerator Development System Motherboard PLL LED Definitions

LED	Definition for Active LED
D9	Gigabit link established
D10	100 Mbps link established
D11	Collision activity
D12	Duplex state
D13	Receive activity
D14	Transmit activity
D15	Any speed link activity

Hex 10/100 Ehternet

The Axcelerator Development System motherboard Hex Ethernet LEDs are described in Table 3-5, and their locations are shown in Figure 3-1.

Table 3-5. Axcelerator Development System Motherboard Hex Ethernet LEDs

LED	Definition for Active LED
D16	Port 1 100 Base-T link present
D17	Port 1 Link
D18	Port 1 Activity
D19	Port 2 100 Base-T link present
D20	Port 2 Link
D21	Port 2 Activity
D22	Port 3 100 Base-T link present
D23	Port 3 Link
D24	Port 3 Activity
D25	Port 4 100 Base-T link present
D26	Port 4 Link
D27	Port 4 Activity
D28	Port 5 100 Base-T link present
D29	Port 5 Link
D30	Port 5 Activity
D31	Port 6 100 Base-T link present
D32	Port 6 Link
D33	Port 6 Activity

Test Points Location/Function

The Axcelerator Development System motherboard test points are described in Table 3-6, and shown in Figure 3-3.

Table 3-6. Axcelerator Development System Motherboard Test Point Definitions

Test Point	Definition
TP1	VCORE- 1.5 volt FPGA power supply
TP2	V3_3-3.3 volt switcher power supply
TP3	V5-5 volt input power
TP4	V3_3L-3.3 volt linear power supply
TP5	V1_5-1.5 volt linear power supply
TP6	V1_8-1.8 volt linear power supply
TP7	V2_5-2.5 volt linear power supply
TP8	V_GTLP-1.0 voltage source
TP9-TP14	Ground

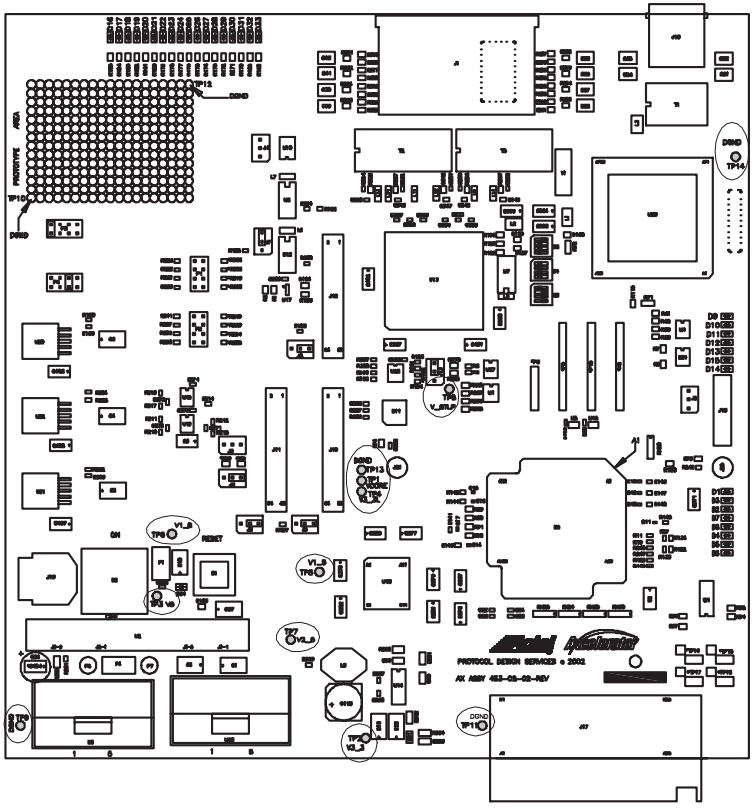

Figure 3-3. Axcelerator Development System Motherboard Test Point Locations

External VHDM-HSD Connector

The Axcelerator Development System motherboard VHDM connections are defined in Table 3-7.

Table 3-7. Axcelerator Development System Motherboard VHMD Connections

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
F21	IO51NB1F4	SPI 4.2 Receive Data[15]	FPGA_RDATN15	J17 pin H16
E21	IO51PB1F4	SPI 4.2 Receive Data[15]	FPGA_RDATP15	J17 pin G16
D24	IO54NB1F5	SOI 4.2 Receive Data [14]	FPGA_RDATN14	J17 pin H15
D23	IO54PB1F5	SPI 4.2 Receive Data[14]	FPGA_RDATP14	J17 pin G15
C24	IO49NB1F3	SPI 4.2 Receive Data[13]	FPGA_RDATN13	J17 pin H14
C23	IO49PB1F4	SPI 4.2 Receive Data[13]	FPGA_RDATP13	J17 pin G14
F24	IO58NB1F4	SPI 4.2 Receive Data[12]	FPGA_RDATN12	J17 pin H13
E24	IO58PB1F5	SPI 4.2 Receive Data[12]	FPGA_RDATP12	J17 pin G13
F25	IO62NB1F5	SPI 4.2 Receive Data[11]	FPGA_RDATN11	J17 pin H12
E25	IO62PB1F5	SPI 4.2 Receive Data[11]	FPGA_RDATP11	J17 pin G12
A17	IO34NB1F3	SPI 4.2 Receive Data[10]	FPGA_RDATN10	J17 pin H11
B17	IO34PB1F3	SPI 4.2 Receive Data[10]	FPGA_RDATP10	J17 pin G11
D18	IO35NB1F3	SPI 4.2 Receive Data[9]	FPGA_RDATN9	J17 pin H10
C18	IO35PB1F3	SPI 4.2 Receive Data[9]	FPGA_RDATP9	J17 pin G10
B19	IO37NB1F3	SPI 4.2 Receive Data[8]	FPGA_RDATN8	J17 pin H9
A19	IO37PB1F3	SPI 4.2 Receive Data[8]	FPGA_RDATP8	J17 pin G9
B20	IO39NB1F3	SPI 4.2 Receive Data[7]	FPGA_RDATN7	J17 pin H8
A20	IO39PB1F3	SPI 4.2 Receive Data[7]	FPGA_RDATP7	J17 pin G8
A22	IO43NB1F4	SPI 4.2 Receive Data[6]	FPGA_RDATN6	J17 pin H7
A21	IO43PB1F4	SPI 4.2 Receive Data[6]	FPGA_RDATP6	J17 pin G7
D22	IO46NB1F4	SPI 4.2 Receive Data[5]	FPGA_RDATN5	J17 pin H6

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
C22	IO46PB1F4	SPI 4.2 Receive Data[5]	FPGA_RDATP5	J17 pin G6
B25	IO53NB1F4	SPI 4.2 Receive Data[4]	FPGA_RDATN4	J17 pin H5
B24	IO53PB1F4	SPI 4.2 Receive Data[4]	FPGA_RDATP4	J17 pin G5
A25	IO47NB1F4	SPI 4.2 Receive Data[3]	FPGA_RDATN3	J17 pin H4
A24	IO47PB1F4	SPI 4.2 Receive Data[3]	FPGA_RDATP3	J17 pin G4
D25	IO57NB1F5	SPI 4.2 Receive Data[2]	FPGA_RDATN2	J17 pin H3
C25	IO57PB1F5	SPI 4.2 Receive Data[2]	FPGA_RDATP2	J17 pin G3
D26	IO59NB1F5	SPI 4.2 Receive Data[1]	FPGA_RDATN1	J17 pin H2
C26	IO59PB1F5	SPI 4.2 Receive Data[1]	FPGA_RDATP1	J17 pin G2
B27	IO61NB1F5	SPI 4.2 Receive Data[0]	FPGA_RDATN0	J17 pin H1
A27	IO61PB1F5	SPI 4.2 Receive Data[0]	FPGA_RDATP0	J17 pin G1
D21	IO45NB1F4	SPI 4.2 Receive Control	FPGA_RDCTLN	J17 pin H17
D20	IO45PB1F4	SPI 4.2 Receive Control	FPGA_RDCTLP	J17 pin G17
D9	IO13PB0F1	SPI 4.2 Receive FIFO Status [1]	FPGA_RSTAT1	J17 pin D2
F11	IO14NB0F1	SPI 4.2 Receive FIFO Status [0]	FPGA_RSTAT0	J17 pin E2
G11	IO14PB0F1	SPI 4.2 Receive Status Clock	FPGA_RSCLK	J17 pin D3
J26	IO70NB2F6	SPI 4.2 Transmit Data [15]	FPGA_TDATN15	J17 pin B16
J25	IO70PB2F6	SPI 4.2 Transmit Data [15]	FPGA_TDATP15	J17 pin A16
K27	IO77NB2F7	SPI 4.2 Transmit Data [14]	FPGA_TDATN14	J17 pin B15
J27	IO77PB2F7	SPI 4.2 Transmit Data [14]	FPGA_TDATP14	J17 pin A15
M27	IO78NB2F7	SPI 4.2 Transmit Data [13]	FPGA_TDATN13	J17 pin B14
L27	IO78PB2F7	SPI 4.2 Transmit Data [13]	FPGA_TDATP13	J17 pin A14

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
M28	IO81NB2F7	SPI 4.2 Transmit Data [12]	FPGA_TDATN12	J17 pin B13
L28	IO81PB2F7	SPI 4.2 Transmit Data [12]	FPGA_TDATP12	J17 pin A13
N26	IO82NB2F7	SPI 4.2 Transmit Data [11]	FPGA_TDATN11	J17 pin B12
M26	IO82PB2F7	SPI 4.2 Transmit Data [11]	FPGA_TDATP11	J17 pin A12
P28	IO89NB2F8	SPI 4.2 Transmit Data [10]	FPGA_TDATN10	J17 pin B11
P27	IO89PB2F8	SPI 4.2 Transmit Data [10]	FPGA_TDATP10	J17 pin A11
R26	IO91NB2F8	SPI 4.2 Transmit Data [9]	FPGA_TDATN9	J17 pin B10
P26	IO91PB2F8	SPI 4.2 Transmit Data [9]	FPGA_TDATP9	J17 pin A10
F27	IO69NB2F6	SPI 4.2 Transmit Data [8]	FPGA_TDATN8	J17 pin B9
E27	IO69PB2F6	SPI 4.2 Transmit Data [8]	FPGA_TDATP8	J17 pin A9
G28	IO73NB2F6	SPI 4.2 Transmit Data [7]	FPGA_TDATN7	J17 pin B8
F28	IO73PB2F6	SPI 4.2 Transmit Data [7]	FPGA_TDATP7	J17 pin A8
H27	IO71NB2F6	SPI 4.2 Transmit Data [6]	FPGA_TDATN6	J17 pin B7
G27	IO71PB2F6	SPI 4.2 Transmit Data [6]	FPGA_TDATP6	J17 pin A7
J28	IO72NB2F6	SPI 4.2 Transmit Data [5]	FPGA_TDATN5	J17 pin B6
H28	IO72PB2F6	SPI 4.2 Transmit Data [5]	FPGA_TDATP5	J17 pin A6
K30	IO79NB2F6	SPI 4.2 Transmit Data [4]	FPGA_TDATN4	J17 pin B5
K29	IO79PB2F7	SPI 4.2 Transmit Data [4]	FPGA_TDATP4	J17 pin A5
M29	IO85NB2F7	SPI 4.2 Transmit Data [3]	FPGA_TDATN3	J17 pin B4
L29	IO85PB2F8	SPI 4.2 Transmit Data [3]	FPGA_TDATP3	J17 pin A4
N28	IO86NB2F8	SPI 4.2 Transmit Data [2]	FPGA_TDATN2	J17 pin B3
N27	IO86PB2F8	SPI 4.2 Transmit Data [2]	FPGA_TDATP2	J17 pin A3

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
P29	IO87NB2F8	SPI 4.2 Transmit Data [1]	FPGA_TDATN1	J17 pin B2
P30	IO87PB2F8	SPI 4.2 Transmit Data [1]	FPGA_TDATP1	J17 pin A2
R29	IO93NB2F8	SPI 4.2 Transmit Data [0]	FPGA_TDATN0	J17 pin B1
R30	IO93PB2F8	SPI 4.2 Transmit Data [0]	FPGA_TDATP0	J17 pin A1
H26	IO66NB2F6	SPI 4.2 Transmit Control	FPGA_TDCTLN	J17 pin B17
H25	IO66PB2F6	SPI 4.2 Transmit Control	FPGA_TDCTLP	J17 pin A17
E10	IO12NB0F1	SPI 4.2 Transmit FIFO Status [1]	FPGA_TSTAT1	J17 pin D24
F10	IO12PB0F1	SPI 4.2 Transmit FIFO Status [0]	FPGA_TSTAT0	J17 pin E24
D10	IO13NB1F3	SPI 4.2 Transmit Clock	FPGA_TSCLK	J17 pin D23

PowerQUICC II Processor Module

This section describes LED locations and functions for the PowerQUICC II Processor Module.

Switch Location/Function

The Axcelerator Development System PowerQUICC II Processor Module switches are described in Table 3-8, and their locations are shown in Figure 3-4.

Note: Do not change these switches. They are for software configuration only.

Table 3-8. PowerQUICC II Processor Module Switch Definitions

Switch	Description	Switch On	Switch Off	Default Setting
S1	Reset	Reset System	Normal Operation	Off
S2(1)	Future use	N/A	N/A	Off
S2(2)	Future use	N/A	N/A	Off
S2(3)	Future use	N/A	N/A	Off
S2(4)	Configuration	Factory-defined	Standard	Off

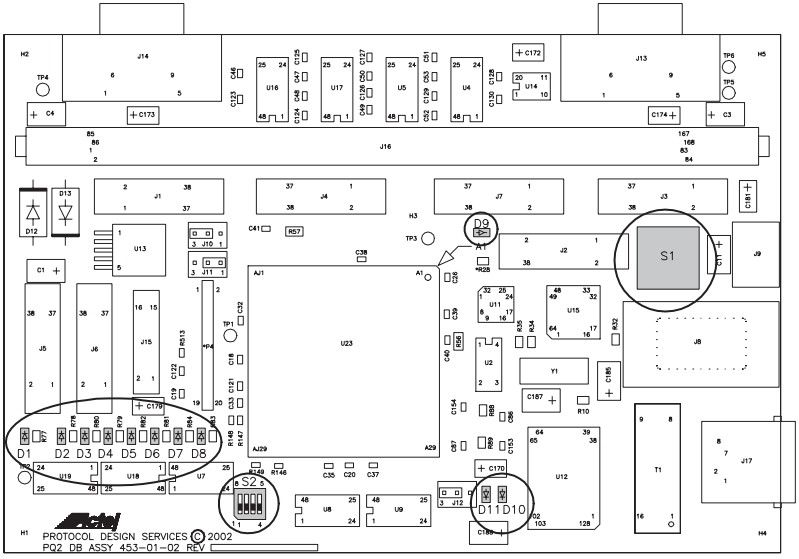

Figure 3-4. PowerQUICC II Processor Module Switch and LED Locations

Configuration Jumpers Location/Function

The Axcelerator Development System PowerQUICC II Processor Module jumpers are described in Table 3-9, and their locations are shown in Figure 3-5.

Table 3-9. PowerQUICC II Processor Module Jumper Definitions

Jumper Reference	Jumper Function	Default Location Pin-to-Pin
J10	PowerQUICC II Flash configuration (programmed or blank)	2 to 3
J11	Enable/disable PowerQUICC II control of AX FPGA power sequencing	1 to 2
J12	PowerQUICC II local bus enable to AX FPGA	2 to 3

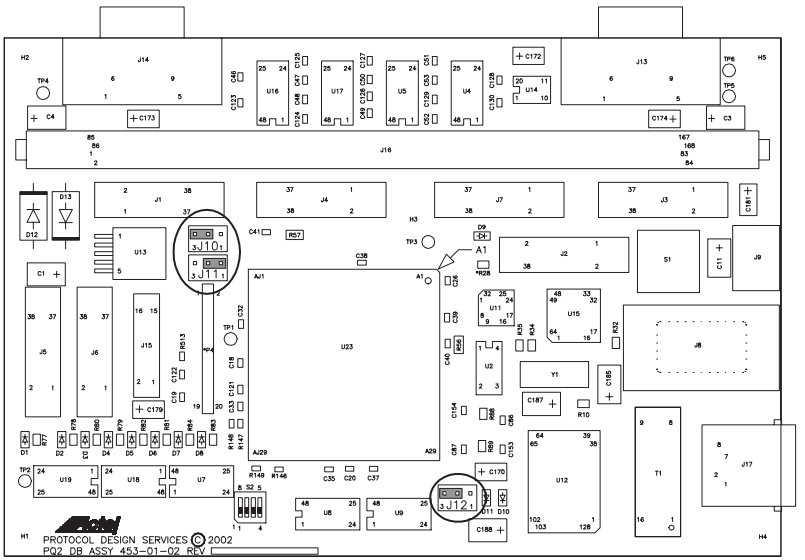

Figure 3-5. PowerQUICC II Processor Module Jumper Locations

LEDs Location/Function

The Axcelerator Development System PowerQUICC II Processor Module general purpose LEDs are described in Table 3-10 and their locations are shown in Figure 3-4.

Table 3-10. PowerQUICC II Processor Module General Purpose LED Definitions

LED	Definition for Active LED
D1	Power
D2	Processor configuration complete
D3	Entered POST
D4	Server ready
D5	Future use
D6	Future use
D7	Future use
D8	Future use
D9	10/100 Ethernet activity
D10	ATM Transmit
D11	ATM receive

Test Points Location/ Function

The Axcelerator Development System PowerQUICC II Processor Module test points are described in Table 3-11, and their locations are shown in Figure 3-6.

Table 3-11. PowerQUICC II Processor Module Test Points

Test Point	Definition
TP1	VCORE_PPC- 2.5 volt from linear regulator
TP2	VCC- 5 volt input power
TP3	V3_3-3.3 volt input power
TP4	Ground
TP5	Ground
TP6	Chassis Ground

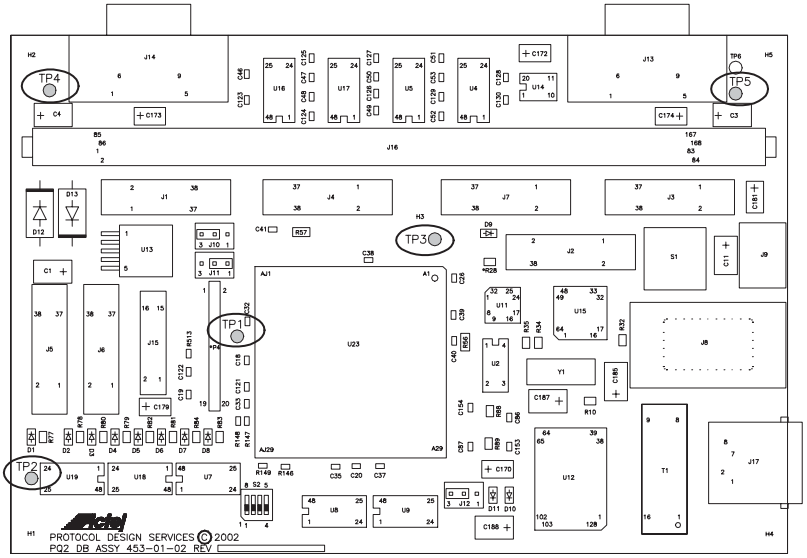

Figure 3-6. PowerQUICC II Processor Module Test Point Locations

Loop-back Board

The Axcelerator Development System Loop-back Board connections are defined in Table 3-12.

Table 3-12. Loop-Back Board Connections.

J1 .B1 to J1 .H1	J1 .B19 to J1 .H19
J1 .A1 to J1 .G1	J1 .A19 to J1 .G19
J1 .B2 to J1 .H2	J1 .B20 to J1 .H20
J1 .A2 to J1 .G2	J1 .A20 to J1 .G20
J1 .B3 to J1 .H3	J1 .B21 to J1 .H21
J1 .A3 to J1 .G3	J1 .A21 to J1 .G21
J1 .B4 to J1 .H4	J1 .B22 to J1 .H22
J1 .A4 to J1 .G4	J1 .A22 to J1 .G22
J1 .B5 to J1 .H5	J1 .B23 to J1 .H23
J1 .A5 to J1 .G5	J1 .A23 to J1 .G23
J1 .B6 to J1 .H6	J1 .B24 to J1 .H24
J1 .A6 to J1 .G6	J1 .A24 to J1 .G24
J1 .B7 to J1 .H7	J1 .B25 to J1 .H25
J1 .A7 to J1 .G7	J1 .A25 to J1 .G25
J1 .B8 to J1 .H8	J1 .E2 to J1 .E24
J1 .A8 to J1 .G8	J1 .D2 to J1 .D24
J1 .B9 to J1 .H9	J1 .E3 to J1 .E23
J1 .A9 to J1 .G9	J1 .D3 to J1 .D23
J1 .B10 to J1 .H10	J1 .E4 to J1 .E22
J1 .A10 to J1 .G10	J1 .D4 to J1 .D22
J1 .B11 to J1 .H11	J1 .E5 to J1 .E21

J1 .A11 to J1 .G11	J1 .D5 to J1 .D21
J1 .B12 to J1 .H12	J1 .E6 to J1 .E20
J1 .A12 to J1 .G12	J1 .D6 to J1 .D20
J1 .B13 to J1 .H13	J1 .E7 to J1 .E19
J1 .A13 to J1 .G13	J1 .D7 to J1 .D19
J1 .B14 to J1 .H14	J1 .E8 to J1 .E18
J1 .A14 to J1 .G14	J1 .D8 to J1 .D18
J1 .B15 to J1 .H15	J1 .E9 to J1 .E17
J1 .A15 to J1 .G15	J1 .D9 to J1 .D17
J1 .B16 to J1 .H16	J1 .E10 to J1 .E1
J1 .A16 to J1 .G16	J1 .D10 to J1 .D16
J1 .B17 to J1 .H17	J1 .E11 to J1 .E15
J1 .A17 to J1 .G17	J1 .D11 to J1 .D15
J1 .B18 to J1 .H18	J1 .E12 to J1 .E14
J1 .A18 to J1 .G18	J1 .D12 to J1 .D14

Backplane

The Axcelerator Development System Backplane connections are defined in Table 3-13.

Table 3-13. Backplane Connections

J13 pin H1 to J14 pin B1	J13 pin B7 to J14 pin H7	J13 pin E19 to J14 pin E7
J13 pin G1 to J14 pin A1	J13 pin A7 to J14 pin G7	J13 pin D19 to J14 pin D7
J13 pin H2 to J14 pin B2	J13 pin B8 to J14 pin H8	J13 pin E18 to J14 pin E8
J13 pin G2 to J14 pin A2	J13 pin A8 to J14 pin G8	J13 pin D18 to J14 pin D8
J13 pin H3 to J14 pin B3	J13 pin B9 to J14 pin H9	J13 pin E17 to J14 pin E9

J13 pin G3 to J14 pin A3	J13 pin A9 to J14 pin G9	J13 pin D17 to J14 pin D9
J13 pin H4 to J14 pin B4	J13 pin B10 to J14 pin H10	J13 pin E16 to J14 pin E10
J13 pin G4 to J14 pin A4	J13 pin A10 to J14 pin G10	J13 pin D16 to J14 pin D10
J13 pin H5 to J14 pin B5	J13 pin B11 to J14 pin H11	J13 pin E15 to J14 pin E11
J13 pin G5 to J14 pin A5	J13 pin A11 to J14 pin G11	J13 pin D15 to J14 pin D11
J13 pin H6 to J14 pin B6	J13 pin B12 to J14 pin H12	J13 pin E14 to J14 pin E12
J13 pin G6 to J14 pin A6	J13 pin A12 to J14 pin G12	J13 pin D14 to J14 pin D12
J13 pin H7 to J14 pin B7	J13 pin B13 to J14 pin H13	J13 pin B19 to J14 pin H19
J13 pin G7 to J14 pin A7	J13 pin A13 to J14 pin G13	J13 pin A19 to J14 pin G19
J13 pin H8 to J14 pin B8	J13 pin B14 to J14 pin H14	J13 pin B20 to J14 pin H20
J13 pin G8 to J14 pin A8	J13 pin A14 to J14 pin G14	J13 pin A20 to J14 pin G20
J13 pin H9 to J14 pin B9	J13 pin B15 to J14 pin H15	J13 pin B21 to J14 pin H21
J13 pin G9 to J14 pin A9	J13 pin A15 to J14 pin G15	J13 pin A21 to J14 pin G21
J13 pin H10 to J14 pin B10	J13 pin B16 to J14 pin H16	J13 pin B22 to J14 pin H22
J13 pin G10 to J14 pin A10	J13 pin A16 to J14 pin G16	J13 pin A22 to J14 pin G22
J13 pin H11 to J14 pin B11	J13 pin B17 to J14 pin H17	J13 pin B23 to J14 pin H23
J13 pin G11 to J14 pin A11	J13 pin A17 to J14 pin G17	J13 pin A23 to J14 pin G23
J13 pin H12 to J14 pin B12	J13 pin B18 to J14 pin H18	J13 pin B24 to J14 pin H24
J13 pin G12 to J14 pin A12	J13 pin A18 to J14 pin G18	J13 pin A24 to J14 pin G24
J13 pin H13 to J14 pin B13	J13 pin H19 to J14 pin B19	J13 pin B25 to J14 pin H25
J13 pin G13 to J14 pin A13	J13 pin G19 to J14 pin A19	J13 pin A25 to J14 pin G25
J13 pin H14 to J14 pin B14	J13 pin H20 to J14 pin B20	J13 pin E2 to J14 pin E24
J13 pin G14 to J14 pin A14	J13 pin G20 to J14 pin A20	J13 pin D2 to J14 pin D24
J13 pin H15 to J14 pin B15	J13 pin H21 to J14 pin B21	J13 pin E3 to J14 pin E23

J13 pin G15 to J14 pin A15	J13 pin G21 to J14 pin A21	J13 pin D3 to J14 pin D23
J13 pin H16 to J14 pin B16	J13 pin H22 to J14 pin B22	J13 pin E4 to J14 pin E22
J13 pin G16 to J14 pin A16	J13 pin G22 to J14 pin A22	J13 pin D4 to J14 pin D22
J13 pin H17 to J14 pin B17	J13 pin H23 to J14 pin B23	J13 pin E5 to J14 pin E21
J13 pin G17 to J14 pin A17	J13 pin G23 to J14 pin A23	J13 pin D5 to J14 pin D21
J13 pin H18 to J14 pin B18	J13 pin H24 to J14 pin B24	J13 pin E6 to J14 pin E20
J13 pin G18 to J14 pin A18	J13 pin G24 to J14 pin A24	J13 pin D6 to J14 pin D20
J13 pin B1 to J14 pin H1	J13 pin H25 to J14 pin B25	J13 pin E7 to J14 pin E19
J13 pin A1 to J14 pin G1	J13 pin G25 to J14 pin A25	J13 pin D7 to J14 pin D19
J13 pin B2 to J14 pin H2	J13 pin E24 to J14 pin E2	J13 pin E8 to J14 pin E18
J13 pin A2 to J14 pin G2	J13 pin D24 to J14 pin D2	J13 pin D8 to J14 pin D18
J13 pin B3 to J14 pin H3	J13 pin E23 to J14 pin E3	J13 pin E9 to J14 pin E17
J13 pin A3 to J14 pin G3	J13 pin D23 to J14 pin D3	J13 pin D9 to J14 pin D17
J13 pin B4 to J14 pin H4	J13 pin E22 to J14 pin E4	J13 pin E10 to J14 pin E16
J13 pin A4 to J14 pin G4	J13 pin D22 to J14 pin D4	J13 pin D10 to J14 pin D16
J13 pin B5 to J14 pin H5	J13 pin E21 to J14 pin E5	J13 pin E11 to J14 pin E15
J13 pin A5 to J14 pin G5	J13 pin D21 to J14 pin D5	J13 pin D11 to J14 pin D15
J13 pin B6 to J14 pin H6	J13 pin E20 to J14 pin E6	J13 pin E12 to J14 pin E14
J13 pin A6 to J14 pin G6	J13 pin D20 to J14 pin D6	J13 pin D12 to J14 pin D14

A

Representative HyperTerminal Connection Log

This appendix shows the representative HyperTerminal connection log.

Checking communications with Ethernet PHY...PASSED

Checking local bus connection with PMC5350 ATM Device...PASSED

Running SDRAM Address line test...PASSED

Running SDRAM Data line test...PASSED

Hit any key to enter POST menu.....

Loading OS from Flash...

Šooting OS...

loaded at: 00400000 00956298

board data at: 00000000 0000002C

relocated to: 00953130 0095315C

zimage at: 00405820 00472EB7

initrd at: 00473000 00952F11

avail ram: 00957000 08000000

Linux/PPC load: console=ttyS2,9600 root=/dev/ramdisk

Uncompressing Linux...done.

Now booting the kernel

Memory BAT mapping: BAT2=128Mb, BAT3=0Mb, residual: 0Mb

Linux version 2.4.18 (Actel Design Services @ENG-NJ1) (gcc version 2.95.3 20010

315 (release)) #369 Thu Dec 19 11:56:58 2002

On node 0 totalpages: 32768

zone(0): 32768 pages.

zone(1): 0 pages.

zone(2): 0 pages.

Kernel command line: console=ttyS2,9600 root=/dev/ramdisk

Warning: real time clock seems stuck!

Calibrating delay loop... 133.12 BogoMIPS

Memory: 122600k available (916k kernel code, 328k data, 44k init, 0k highmem)

Dentry-cache hash table entries: 16384 (order: 5, 131072 bytes)

Inode-cache hash table entries: 8192 (order: 4, 65536 bytes)

Mount-cache hash table entries: 2048 (order: 2, 16384 bytes)

Buffer-cache hash table entries: 8192 (order: 3, 32768 bytes)

Page-cache hash table entries: 32768 (order: 5, 131072 bytes)

POSIX conformance testing by UNIFIX

Linux NET4.0 for Linux 2.4

Based upon Swansea University Computer Society NET3.039

Initializing RT netlink socket

Starting kswapd

CPM UART driver version 0.01

ttyS00 at 0x0000 is a SMC

ttyS01 at 0x0040 is a SMC

ttyS02 at 0x, ttyS03 at 0x8100 is a SCC

ttyS04 at 0x8200 is a SCC

Actel daughterboard driver initialized

Axcelerator LED driver initialized

CS4 remap address = '0xC9000000

CS5 remap address = '0xC9011000'

CS6 remap address = '0xC9022000

CS7 remap address = '0xC9033000

Actel Axcelerator FPGA, Version '0x30091', Features '0x1B0B'

Axcelerator FPGA driver initialized

Axcelerator Hex Ethernet driver initialized

Axcelerator Gigabit driver initialized

Axcelerator Power driver initialized

block: 128 slots per queue, batch=32

RAMDISK driver initialized: 16 RAM disks of 16384K size 1024 blocksize

eth0: FCC ENET Version 0.2, 00:0b:e9:0a:00:0f

PPP generic driver version 2.4.1

PPP Deflate Compression module registered

NET4: Linux TCP/IP 1.0 for NET4.0

IP Protocols: ICMP, UDP, TCP

IP: routing cache hash table of 1024 buckets, 8Kbytes

TCP: Hash tables configured (established 8192 bind 8192)

NET4: Unix domain sockets 1.0/SMP for Linux NET4.0.

RAMDISK: Compressed image found at block 0

Freeing initrd memory: 4991k freed

EXT2-fs warning: mounting unchecked fs, running e2fsck is recommended

VFS: Mounted root (ext2 filesystem).

Freeing unused kernel memory: 44k init

tty_io.c: process 1 (swapper) used obsolete /dev/cua - update software to use /d

ev/ttyS2

tty_io.c: process 1 (init) used obsolete /dev/cua - update software to use /dev/ttyS2

tty_io.c: process 1 (init) used obsolete /dev/cua - update software to use /dev/

ttyS2

INIT: tty_io.c: process 1 (init) used obsolete /dev/cua - update software to use /dev/ttyS2

version 2.78 bootingtty_io.c: process 1 (init) used obsolete /dev/cua - update s oftware to use /dev/ttyS2

INIT: Entering runlevel: 1

Axcelerator Development System Startup

Current board address => 10.20.81.170

Hit enter key to change board IP Address (5 seconds) :

Enter new board address(. to ignore): (x.x.x.x) ->10.20.81.170

Board MAC Address = 00:0B:E9:A:0:F

Configure board IP = 10.20.81.170

Starting server

B

FPGA Pin Definition

This appendix lists the FPGA pin definitions.

GIGABIT TX AND CONTROL SIGNALS

Table B-1 lists FPGA pin definitions for Gigabit TX and Control Signals.

Table B-1. Gigabit TX and Control Signal Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level*
D6	IO00NB0F0	GbE Transmit Data [7]	GIBT_TXD_7_TERM	port_out_reg0_i(0)	OUTBUF LVTTL	V3_3L	Low
E6	IO00PB0F0	GbE Transmit Data [6]	GIBT_TXD_6_TERM	port_out_reg0_i(1)	OUTBUF LVTTL	V3_3L	Low
A5	IO01NB0F0	GbE Transmit Data [5]	GIBT_TXD_5_TERM	port_out_reg0_i(2)	OUTBUF LVTTL	V3_3L	Low
B5	IO01PB0F0	GbE Transmit Data [4]	GIBT_TXD_4_TERM	port_out_reg0_i(3)	OUTBUF LVTTL	V3_3L	Low
G9	IO02NB0F0	GbE Transmit Data [3]	GIBT_TXD_3_TERM	port_out_reg0_i(4)	OUTBUF LVTTL	V3_3L	Low
G8	IO02PB0F0	GbE Transmit Data [2]	GIBT_TXD_2_TERM	port_out_reg0_i(5)	OUTBUF LVTTL	V3_3L	Low

Table B-1. Gigabit TX and Control Signal Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level*
F8	IO03NB0F0	GbE Transmit Data [1]	GIBT_TXD_1_TERM	port_out_reg0_i(6)	OUTBUF LVTTL	V3_3L	Low
F7	IO03PB0F0	GbE Transmit Data [0]	GIBT_TXD_0_TERM	port_out_reg0_i(7)	OUTBUF LVTTL	V3_3L	Low
D7	IO04NB0F0	GbE Transmit Enable	GIBT_TX_EN_TERM	port_out_reg0_i(8)	OUTBUF LVTTL	V3_3L	Low
C7	IO05NB0F0	GbE Transmit Coding Error	GIBT_TX_ER_TERM	port_out_reg0_i(10)	OUTBUF LVTTL	V3_3L	Low
C8	IO11PB0F0	GbE Autonegotiation Restart	LXT1000_AN_RSTRT	port_out_reg0_i(11)	OUTBUF LVTTL	V3_3L	Low

Note: The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B- 2 lists FPGA pin definitions for Gigabit RX and Control Signals.

Table B-2. Gigabit RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip -tion	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level*
C6	IO05PB0 F0	GbE Receive Data [7]	GIGABIT_ RXD_7	port_in_reg0 _i(0)	INBUF LVTTL	V3_3L	Input Only
H9	IO06NB0 F0	GbE Receive Data [6]	GIGABIT_ RXD_6	port_in_reg0 _i(1)	INBUF LVTTL	V3_3L	Input Only
H8	IO06PB0 F0	GbE Receive Data [5]	GIGABIT_ RXD_5	port_in_reg0 _i(2)	INBUF LVTTL	V3_3L	Input Only
D8	IO07NB0 F0	GbE Receive Data [4]	GIGABIT_ RXD_4	port_in_reg0 _i(3)	INBUF LVTTL	V3_3L	Input Only
E8	IO07PB0 F0	GbE Receive Data [3]	GIGABIT_ RXD_3	port_in_reg0 _i(4)	INBUF LVTTL	V3_3L	Input Only
E9	IO08NB0 F0	GbE Receive Data [2]	GIGABIT_ RXD_2	port_in_reg0 _i(5)	INBUF LVTTL	V3_3L	Input Only
F9	IO08PB0 F0	GbE Receive Data [1]	GIGABIT_ RXD_1	port_in_reg0 _i(6)	INBUF LVTTL	V3_3L	Input Only
A7	IO09NB0 F0	GbE Receive Data [0]	GIGABIT_ RXD_0	port_in_reg0 _i(7)	INBUF LVTTL	V3_3L	Input Only

Table B-2. Gigabit RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip -tion	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level*
B7	IO09PB0 F0	GbE Receive Data Valid	GIGABIT_ RXD_DV	port_in_reg0 _i(8)	INBUF LVTTL	V3_3L	Input Only
H10	IO10NB0 F0	GbE Receive Error	GIGABIT_ RXD_ER	port_in_reg0 _i(9)	INBUF LVTTL	V3_3L	Input Only
G10	IO10PB0 F0	GbE Col- lision	GIGABIT_ COL	port_in_reg0 _i(10)	INBUF LVTTL	V3_3L	Input Only
C9	IO11NB0 F0	GbE Car- rier Sense	GIGABIT_ CRS	port_in_reg0 _i(11)	INBUF LVTTL	V3_3L	Input Only

Note: The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-3 lists FPGA pin definitions for SPI-4.2 RX and Control Signals.

Table B-3. SPI -4.2 RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O RingNet Name	External Connector	FPGA Buffer Type	Power Domain	Note
F21	IO51N B1F4	SPI 4.2 Receive Data[15]	FPGA_ RDATN15	port_in_ reg1_i(15)	J17 pin H16	INBUF _LVDS	V2_5	1
E21	IO51P B1F4	SPI 4.2 Receive Data[15]	FPGA_ RDATP15	port_in_ reg1_i(15)	J17 pin G16	INBUF _LVDS	V2_5	
D24	IO54N B1F5	SPI 4.2 Receive Data[14]	FPGA_ RDATN14	port_in_ reg1_i(14)	J17 pin H15	INBUF _LVDS	V2_5	1
D23	IO54P B1F5	SPI 4.2 Receive Data[14]	FPGA_ RDATP14	port_in_re g1_i(14)	J17 pin G15	INBUF _LVDS	V2_5	
C24	IO49N B1F3	SPI 4.2 Receive Data[13]	FPGA_ RDATN13	port_in_ reg1_i(13)	J17 pin H14	INBUF _LVDS	V2_5	1
C23	IO49P B1F4	SPI 4.2 Receive Data[13]	FPGA_ RDATP13	port_in_ reg1_i(13)	J17 pin G14	INBUF _LVDS	V2_5	
F24	IO58N B1F4	SPI 4.2 Receive Data[12]	FPGA_ RDATN12	port_in_ reg1_i(12)	J17 pin H13	INBUF _LVDS	V2_5	1
E24	IO58P B1F5	SPI 4.2 Receive Data[12]	FPGA_ RDATP12	port_in_ reg1_i(12)	J17 pin G13	INBUF _LVDS	V2_5	

Table B-3. SPI -4.2 RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O RingNet Name	External Connector	FPGA Buffer Type	Power Domain	Note
F25	IO62N B1F5	SPI 4.2 Receive Data[11]	FPGA_ RDATN11	port_in_ reg1_i(11)	J17 pin H12	INBUF _LVDS	V2_5	1
E25	IO62P B1F5	SPI 4.2 Receive Data[11]	FPGA_ RDATP11	port_in_ reg1_i(11)	J17 pin G12	INBUF _LVDS	V2_5	
A17	IO34N B1F3	SPI 4.2 Receive Data[10]	FPGA_ RDATN10	port_in_ reg1_i(10)	J17 pin H11	INBUF _LVDS	V2_5	1
B17	IO34P B1F3	SPI 4.2 Receive Data[10]	FPGA_ RDATP10	port_in_ reg1_i(10)	J17 pin G11	INBUF _LVDS	V2_5	
D18	IO35N B1F3	SPI 4.2 Receive Data[9]	FPGA_ RDATN9	port_in_ reg1_i(9)	J17 pin H10	INBUF _LVDS	V2_5	1
C18	IO35P B1F3	SPI 4.2 Receive Data[9]	FPGA_ RDATP9	port_in_ reg1_i(9)	J17 pin G10	INBUF _LVDS	V2_5	
B19	IO37N B1F3	SPI 4.2 Receive Data[8]	FPGA_ RDATN8	port_in_ reg1_i(8)	J17 pin H9	INBUF _LVDS	V2_5	1
A19	IO37P B1F3	SPI 4.2 Receive Data[8]	FPGA_ RDATP8	port_in_ reg1_i(8)	J17 pin G9	INBUF _LVDS	V2_5	
B20	IO39N B1F3	SPI 4.2 Receive Data[7]	FPGA_ RDATN7	port_in_ reg1_i(7)	J17 pin H8	INBUF _LVDS	V2_5	1

Table B-3. SPI -4.2 RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O RingNet Name	External Connector	FPGA Buffer Type	Power Domain	Note
A20	IO39P B1F3	SPI 4.2 Receive Data[7]	FPGA_ RDATP7	port_in_ reg1_i(7)	J17 pin G8	INBUF _LVDS	V2_5	
A22	IO43N B1F4	SPI 4.2 Receive Data[6]	FPGA_ RDATN6	port_in_ reg1_i(6)	J17 pin H7	INBUF _LVDS	V2_5	1
A21	IO43P B1F4	SPI 4.2 Receive Data[6]	FPGA_ RDATP6	port_in_ reg1_i(6)	J17 pin G7	INBUF _LVDS	V2_5	
D22	IO46N B1F4	SPI 4.2 Receive Data[5]	FPGA_ RDATN5	port_in_ reg1_i(5)	J17 pin H6	INBUF _LVDS	V2_5	1
C22	IO46P B1F4	SPI 4.2 Receive Data[5]	FPGA_ RDATP5	port_in_ reg1_i(5)	J17 pin G6	INBUF _LVDS	V2_5	
B25	IO53N B1F4	SPI 4.2 Receive Data[4]	FPGA_ RDATN4	port_in_ reg1_i(4)	J17 pin H5	INBUF _LVDS	V2_5	1
B24	IO53P B1F4	SPI 4.2 Receive Data[4]	FPGA_ RDATP4	port_in_ reg1_i(4)	J17 pin G5	INBUF _LVDS	V2_5	
A25	IO47N B1F4	SPI 4.2 Receive Data[3]	FPGA_ RDATN3	port_in_ reg1_i(3)	J17 pin H4	INBUF _LVDS	V2_5	1
A24	IO47P B1F4	SPI 4.2 Receive Data[3]	FPGA_ RDATP3	port_in_ reg1_i(3)	J17 pin G4	INBUF _LVDS	V2_5	

Table B-3. SPI -4.2 RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O RingNet Name	External Connector	FPGA Buffer Type	Power Domain	Note
D25	IO57N B1F5	SPI 4.2 Receive Data[2]	FPGA_ RDATN2	port_in_ reg1_i(2)	J17 pin H3	INBUF _LVDS	V2_5	1
C25	IO57P B1F5	SPI 4.2 Receive Data[2]	FPGA_ RDATP2	port_in_ reg1_i(2)	J17 pin G3	INBUF _LVDS	V2_5	
D26	IO59N B1F5	SPI 4.2 Receive Data[1]	FPGA_ RDATN1	port_in_ reg1_i(1)	J17 pin H2	INBUF _LVDS	V2_5	1
C26	IO59P B1F5	SPI 4.2 Receive Data[1]	FPGA_ RDATP1	port_in_ reg1_i(1)	J17 pin G2	INBUF _LVDS	V2_5	
B27	IO61N B1F5	SPI 4.2 Receive Data[0]	FPGA_ RDATN0	port_in_ reg1_i(0)	J17 pin H1	INBUF _LVDS	V2_5	1
A27	IO61P B1F5	SPI 4.2 Receive Data[0]	FPGA_ RDATP0	port_in_ reg1_i(0)	J17 pin G1	INBUF _LVDS	V2_5	
D21	IO45N B1F4	SPI 4.2 Receive Control	FPGA_ RDCTLN	port_in_ reg1_i(16)	J17 pin H17	INBUF _LVDS	V2_5	1
D20	IO45P B1F4	SPI 4.2 Receive Control	FPGA_ RDCTLP	port_in_ reg1_i(16)	J17 pin G17	INBUF _LVDS	V2_5	

Table B-3. SPI -4.2 RX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O RingNet Name	External Connector	FPGA Buffer Type	Power Domain	Note
D9	IO13P B0F1	SPI 4.2 Receive FIFO Status [1]	FPGA_ RSTAT1	port_out_ reg0_i(12)	J17 pin D2	OUT-BUF LVTTL	V3_3L	
F11	IO14N B0F1	SPI 4.2 Receive FIFO Status [0]	FPGA_ RSTAT0	port_out_ reg0_i(13)	J17 pin E2	OUT-BUF LVTTL	V3_3L	
G11	IO14P B0F1	SPI 4.2 Receive Status Clock	FPGA_ RSCLK	port_out_ reg0_i(14)	J17 pin D3	OUT-BUF LVTTL	V3_3L	

The logic default level is not required for SPI-4.2 RX and Control Signals.

Note: (1) This signal has been setup with on-board termination for an input LVDS signal. This signal will have indeterminate behavior if it is used as anything other than an LVDS input.

Table B-4 lists FPGA pin definitions for SPI-4.2 -TX and Control Signals.

Table B-4. SPI-4.2-TX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Note
J26	IO70NB 2F6	SPI 4.2 Transmit Data[15]	FPGA_TDATN15	port_out_reg2_i(15)	J17 pin B16	OUTBUF_LVDS	V2_5	2
J25	IO70PB 2F6	SPI 4.2 Transmit Data[15]	FPGA_TDATP15	port_out_reg2_i(15)	J17 pin A16	OUTBUF_LVDS	V2_5	
K27	IO77NB 2F7	SPI 4.2 Transmit Data[14]	FPGA_TDATN14	port_out_reg2_i(14)	J17 pin B15	OUTBUF_LVDS	V2_5	2
J27	IO77PB 2F7	SPI 4.2 Transmit Data[14]	FPGA_TDATP14	port_out_reg2_i(14)	J17 pin A15	OUTBUF_LVDS	V2_5	
M27	IO78NB 2F7	SPI 4.2 Transmit Data[13]	FPGA_TDATN13	port_out_reg2_i(13)	J17 pin B14	OUTBUF_LVDS	V2_5	2
L27	IO78PB 2F7	SPI 4.2 Transmit Data[13]	FPGA_TDATP13	port_out_reg2_i(13)	J17 pin A14	OUTBUF_LVDS	V2_5	
M28	IO81NB 2F7	SPI 4.2 Transmit Data[12]	FPGA_TDATN12	port_out_reg2_i(12)	J17 pin B13	OUTBUF_LVDS	V2_5	2
L28	IO81PB 2F7	SPI 4.2 Transmit Data[12]	FPGA_TDATP12	port_out_reg2_i(12)	J17 pin A13	OUTBUF_LVDS	V2_5	

Table B-4. SPI-4.2-TX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Note
N26	IO82NB 2F7	SPI 4.2 Transmit Data[11]	FPGA_TDATN11	port_out_reg2_i(11)	J17 pin B12	OUTBUF_LVDS	V2_5	2
M26	IO82PB 2F7	SPI 4.2 Transmit Data[11]	FPGA_TDATP11	port_out_reg2_i(11)	J17 pin A12	OUTBUF_LVDS	V2_5	
P28	IO89NB 2F8	SPI 4.2 Transmit Data[10]	FPGA_TDATN10	port_out_reg2_i(10)	J17 pin B11	OUTBUF_LVDS	V2_5	2
P27	IO89PB 2F8	SPI 4.2 Transmit Data[10]	FPGA_TDATP10	port_out_reg2_i(10)	J17 pin A11	OUTBUF_LVDS	V2_5	
R26	IO91NB 2F8	SPI 4.2 Transmit Data[9]	FPGA_TDATN9	port_out_reg2_i(9)	J17 pin B10	OUTBUF_LVDS	V2_5	2
P26	IO91PB 2F8	SPI 4.2 Transmit Data[9]	FPGA_TDATP9	port_out_reg2_i(9)	J17 pin A10	OUTBUF_LVDS	V2_5	
F27	IO69NB 2F6	SPI 4.2 Transmit Data[8]	FPGA_TDATN8	port_out_reg2_i(8)	J17 pin B9	OUTBUF_LVDS	V2_5	2
E27	IO69PB 2F6	SPI 4.2 Transmit Data[8]	FPGA_TDATP8	port_out_reg2_i(8)	J17 pin A9	OUTBUF_LVDS	V2_5	
G28	IO73NB 2F6	SPI 4.2 Transmit Data[7]	FPGA_TDATN7	port_out_reg2_i(7)	J17 pin B8	OUTBUF_LVDS	V2_5	2

Table B-4. SPI-4.2-TX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Note
F28	IO73PB 2F6	SPI 4.2 Transmit Data[7]	FPGA_TDATP7	port_out_reg2_i(7)	J17 pin A8	OUTBUF_LVDS	V2_5	
H27	IO71NB 2F6	SPI 4.2 Transmit Data[6]	FPGA_TDATN6	port_out_reg2_i(6)	J17 pin B7	OUTBUF_LVDS	V2_5	2
G27	IO71PB 2F6	SPI 4.2 Transmit Data[6]	FPGA_TDATP6	port_out_reg2_i(6)	J17 pin A7	OUTBUF_LVDS	V2_5	
J28	IO72NB 2F6	SPI 4.2 Transmit Data[5]	FPGA_TDATN5	port_out_reg2_i(5)	J17 pin B6	OUTBUF_LVDS	V2_5	2
H28	IO72PB 2F6	SPI 4.2 Transmit Data[5]	FPGA_TDATP5	port_out_reg2_i(5)	J17 pin A6	OUTBUF_LVDS	V2_5	
K30	IO79NB 2F6	SPI 4.2 Transmit Data[4]	FPGA_TDATN4	port_out_reg2_i(4)	J17 pin B5	OUTBUF_LVDS	V2_5	2
K29	IO79PB 2F7	SPI 4.2 Transmit Data[4]	FPGA_TDATP4	port_out_reg2_i(4)	J17 pin A5	OUTBUF_LVDS	V2_5	
M29	IO85NB 2F7	SPI 4.2 Transmit Data[3]	FPGA_TDATN3	port_out_reg2_i(3)	J17 pin B4	OUTBUF_LVDS	V2_5	2
L29	IO85PB 2F8	SPI 4.2 Transmit Data[3]	FPGA_TDATP3	port_out_reg2_i(3)	J17 pin A4	OUTBUF_LVDS	V2_5	

Table B-4. SPI-4.2-TX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Note
N28	IO86NB2F8	SPI 4.2 Transmit Data[2]	FPGA_TDATN2	port_out_reg2_i(2)	J17 pin B3	OUTBUF_LVDS	V2_5	2
N27	IO86PB2F8	SPI 4.2 Transmit Data[2]	FPGA_TDATP2	port_out_reg2_i(2)	J17 pin A3	OUTBUF_LVDS	V2_5	
P29	IO87NB2F8	SPI 4.2 Transmit Data[1]	FPGA_TDATN1	port_out_reg2_i(1)	J17 pin B2	OUTBUF_LVDS	V2_5	2
P30	IO87PB2F8	SPI 4.2 Transmit Data[1]	FPGA_TDATP1	port_out_reg2_i(1)	J17 pin A2	OUTBUF_LVDS	V2_5	
R29	IO93NB2F8	SPI 4.2 Transmit Data[0]	FPGA_TDATN0	port_out_reg2_i(0)	J17 pin B1	OUTBUF_LVDS	V2_5	2
R30	IO93PB2F8	SPI 4.2 Transmit Data[0]	FPGA_TDATP0	port_out_reg2_i(0)	J17 pin A1	OUTBUF_LVDS	V2_5	
H26	IO66NB2F6	SPI 4.2 Transmit Control	FPGA_TDCTLN	port_out_reg2_i(16)	J17 pin B17	OUTBUF_LVDS	V2_5	2
H25	IO66PB2F6	SPI 4.2 Transmit Control	FPGA_TDCTLP	port_out_reg2_i(16)	J17 pin A17	OUTBUF_LVDS	V2_5	

Table B-4. SPI-4.2-TX and Control Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Note
E10	IO12NB 0F1	SPI 4.2 Transmit FIFO Status [1]	FPGA_TSTAT1	port_in_reg0_i(12)	J17 pin D24	INBUF LVTTL	V3_3L	
F10	IO12PB 0F1	SPI 4.2 Transmit FIFO Status [0]	FPGA_TSTAT0	port_in_reg0_i(13)	J17 pin E24	INBUF LVTTL	V3_3L	
D10	IO13NB 1F3	SPI 4.2 Transmit Clock	FPGA_TSCLK	port_in_reg0_i(14)	J17 pin D23	INBUF LVTTL	V3_3L	

The logic default level is not required for SPI-4.2 RX and Control Signals.

Note: (2) This signal has been setup with on-board termination for an output LVDS signal. This signal will have indeterminate behavior if it is used as anything other than an LVDS output.

Table B-5 lists FPGA pin definitions for Clocks.

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level *	Note
C14	IO30NB0F2/ HCLKAN	10 kohm Pulldown	HCLKAN (PULLDOWN)	nc	OPEN	V3_3L		
D14	IO30PB0F2/ HCLKAP	GbE Receive Clock	GIBT_RXD_CLK	port_in_hclock01_i	HCLKBUF LVTTL	V3_3L		
E15	IO31NB0F2/ HCLKBN	10 kohm Pulldown	HCLKBN(PULLDOWN)	nc	OPEN	V3_3L		
D15	IO31PB0F2/ HCLKBP	Global Clock Source 1	HCLKB (GLOBAL CLOCK 1)	port_in_hclock02_i	HCLKBUF LVTTL	V3_3L	Input Only	
E17	IO32NB1F3/ HCLKCN	SPI 4.2 Receive Data Clock	FPGA_RDCLKN	port_in_hclock11_i	HCLKBUF_LVDS	V2_5		
E16	IO32PB1F3/ HCLKCP	SPI 4.2 Receive Data Clock	FPGA_RDCLKP	port_in_hclock11_i	HCLKBUF_LVDS	V2_5		
C17	IO33NB1F3/ HCLKDN	Alternate LVDS Clock source	LVDS_ALT_CLKN_T	port_in_hclock12_i	HCLKBUF_LVDS	V2_5		

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip -tion	Schem- atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Do- main	Required Default Logic Level *	Note
D17	IO33PB1F 3/ HCLKDP	Alternate LVDS Clock source	LVDS_AL T_CLKP_ T	port_in _hclock 12_i	HCLKB UF_LV DS	V2_5		
AG18	IO159NB 4F14/ CLKEN	10 kohm Pulldown	CLKEN(P ULL- DOWN)	nc	OPEN	V3_3L		
AH18	IO159PB4 F14/ CLKEP	Power- QUICC II Clock	CLK_AX	port_in _rclock 41_i	CLK- BUF LVTTL	V3_3L	Input Only	
AG16	IO160NB 4F14/ CLKFN	10 kohm Pulldown	CLKFN(P ULL- DOWN)	nc	OPEN	V3_3L		
AG17	IO160PB4 F14/ CLKFP	Global Clock Source 2	CLKF(GL OBAL CLOCK 2)	port_in _rclock 42_i	CLK- BUF LVTTL	V3_3L	Input Only	
AG14	IO161NB 5F15/ CLKGN	10 kohm Pulldown	CLKHN(P ULL- DOWN)	nc	OPEN	V3_3L		
AG15	IO161PB5 F15/ CLKGP	GbE Transmit Clock	GIBT_TX _CLK	port_in _rclock 51_i	CLK- BUF LVTTL	V3_3L	Input Only	
AG13	IO162NB 5F15/ CLKHN	10 kohm Pulldown	CLKHN(P ULL- DOWN)	nc	OPEN	V3_3L		

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip -tion	Schem- atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Do- main	Required Default Logic Level *	Note
AH13	IO162PB5 F15/ CLKHP	Global Clock Source 3	CLKH(GL OBAL CLOCK 3)	port_in _rclock 52_i	CLK- BUF LVTTL	V3_3L	Input Only	
E7	IO04PB0F 0	GbE Gigabit Transmit Clock	GIBT_GT X_CLK_T ERM	port_ou t_reg0_i (9)	OUT- BUF LVTTL	V3_3L	Low	
G26	IO67NB2 F6	SPI 4.2 Transmit Data Clock	FPGA_TD CLKN	port_ou t_reg2_i (17)	OUTB UF_LV DS	V2_5		2
G25	IO67PB2F 6	SPI 4.2 Transmit Data Clock	FPGA_TD CLKP	port_ou t_reg2_i (17)	OUTB UF_LV DS	V2_5		
AD25	IO126NB 3F11	DDR Memory Output Stage Clock	FPGA_DD R_KN	port_ou t_reg3_i (26)	OUTB UF_HS TL_I	V1_5	Low	
AC25	IO126PB3 F11	DDR Memory Output Stage Clock	FPGA_DD R_K	port_ou t_reg3_i (27)	OUTB UF_HS TL_I	V1_5	High	

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip-tion	Schem-atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Do-main	Required Default Logic Level *	Note
AE26	IO127NB 3F11	DDR Memory Output Clock	FPGA_DD R_CN	port_ou t_reg3_i (28)	OUTB UF_HS TL_I	V1_5	Low	
AD26	IO127PB3 F11	DDR Memory Output Clock	FPGA_DD R_C	port_ou t_reg3_i (29)	OUTB UF_HS TL_I	V1_5	High	
AC24	IO128NB 3F11	DDR Memory Synch. Echo Clock	FPGA_DD R_CQN	port_in _reg3_i (4)	INBUF _HSTL _I	V1_5	Input Only	
AB24	IO128PB EF11	DDR Memory Synch. Echo Clock	FPGA_DD R_CQ	port_in _reg3_i (5)	INBUF _HSTL _I	V1_5	Input Only	
T2	IO224PB6 F20	PLL Test Output @ SMA	NON-AME(PLL _TEST_O UTPUT)	port_ou t_reg6_i (14)	OUT-BUF LVTTL	V3_3L		
AC11	IO181NB 5F17	Hex Fast Ethernet Transmit Clock Port [0]	HEX_TX_ CLK0_TE RM	port_in _reg5_i (15)	INBUF LVTTL	V3_3L	Input Only	

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip-tion	Schem-atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Do-main	Required Default Logic Level *	Note
AD11	IO181PB5F17	Hex Fast Ethernet Transmit Clock Port [1]	HEX_TX_CLK1_TERM	port_in_reg5_i(16)	INBUF LVTTL	V3_3L	Input Only	
AK6	IO182NB5F17	Hex Fast Ethernet Transmit Clock Port [2]	HEX_TX_CLK2_TERM	port_in_reg5_i(17)	INBUF LVTTL	V3_3L	Input Only	
AK7	IO182PB5F17	Hex Fast Ethernet Transmit Clock Port [3]	HEX_TX_CLK3_TERM	port_in_reg5_i(18)	INBUF LVTTL	V3_3L	Input Only	
AF8	IO183NB5F17	Hex Fast Ethernet Transmit Clock Port [4]	HEX_TX_CLK4_TERM	port_in_reg5_i(19)	INBUF LVTTL	V3_3L	Input Only	
AG8	IO183PB5F17	Hex Fast Ethernet Transmit Clock Port [5]	HEX_TX_CLK5_TERM	port_in_reg5_i(20)	INBUF LVTTL	V3_3L	Input Only	

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level *	Note
W3	IO214NB6F20	Hex Fast Ethernet Receive Clock Port [0]	HEX_RX_CLK0_TERM	port_in_reg6_i (42)	INBUF LVTTL	V3_3L	Input Only	
W4	IO214PB6F20	Hex Fast Ethernet Receive Clock Port [1]	HEX_RX_CLK1_TERM	port_in_reg6_i (43)	INBUF LVTTL	V3_3L	Input Only	
U8	IO215NB6F20	Hex Fast Ethernet Receive Clock Port [2]	HEX_RX_CLK2_TERM	port_in_reg6_i (44)	INBUF LVTTL	V3_3L	Input Only	
U9	IO215PB6F20	Hex Fast Ethernet Receive Clock Port [3]	HEX_RX_CLK3_TERM	port_in_reg6_i (45)	INBUF LVTTL	V3_3L	Input Only	
W1	IO216NB6F20	Hex Fast Ethernet Receive Clock Port [4]	HEX_RX_CLK4_TERM	port_in_reg6_i (46)	INBUF LVTTL	V3_3L	Input Only	

Table B-5. Clocks Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Descrip-tion	Schem-atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Do-main	Required Default Logic Level *	Note
W2	IO216PB6 F20	Hex Fast Ethernet Receive Clock Port [5]	HEX_RX_ CLK5_TE RM	port_in _reg6_i (47)	INBUF LVTTL	V3_3L	Input Only	

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Note: (2) This signal has been setup with on-board termination for an output LVDS signal. This signal will have indeterminate behavior if it is used as anything other than an LVDS output.

Table B-6 lists FPGA pin definitions for Reset.

Table B-6. FPGA Reset Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA BUFFER TYPE	Power Domain	Required Default Logic Level
AJ18	IO158PB4 F14	Board Level Power-On Reset	AX_RESET_L_1	port_in_fpga_reset_i	INBUF LVTLL	V3_3L	Input Only
AC21	IO137PB4 F12	Reset from FPGA to Power-QUICC II	AX_PQ2_RESET_N	port_out_reg4_i (32)	OUTBUF LVTTL	V3_3L	

Note: The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-7 lists FPGA pin definitions for DDR Memory.

Table B-7. FPGA Pin Definitions for DDR Memory

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
T29	IO96NB3F9	DDR Memory Synchronous Address [0]	FPGA_DDR_A0	port_out_reg3_i(0)	OUTBUF_HSTL_I	V1_5	Low
T30	IO96PB3F9	DDR Memory Synchronous Address [1]	FPGA_DDR_A1	port_out_reg3_i(1)	OUTBUF_HSTL_I	V1_5	Low
U29	IO97NB3F9	DDR Memory Synchronous Address [2]	FPGA_DDR_A2	port_out_reg3_i(2)	OUTBUF_HSTL_I	V1_5	Low
U30	IO97PB3F9	DDR Memory Synchronous Address [3]	FPGA_DDR_A3	port_out_reg3_i(3)	OUTBUF_HSTL_I	V1_5	Low
U24	IO100NB3F9	DDR Memory Synchronous Address [4]	FPGA_DDR_A4	port_out_reg3_i(4)	OUTBUF_HSTL_I	V1_5	Low
Y28	IO105NB3F9	DDR Memory Synchronous Address [5]	FPGA_DDR_A5	port_out_reg3_i(5)	OUTBUF_HSTL_I	V1_5	Low

Table B-7. FPGA Pin Definitions for DDR Memory

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
W28	IO105 PB3F9	DDR Memory Synchronous Address [6]	FPGA_DDR_A6	port_out_reg3_i(6)	OUTBUF_HSTL_I	V1_5	Low
W24	IO108 NB3F10	DDR Memory Synchronous Address [7]	FPGA_DDR_A7	port_out_reg3_i(7)	OUTBUF_HSTL_I	V1_5	Low
Y27	IO109 NB3F10	DDR Memory Synchronous Address [8]	FPGA_DDR_A8	port_out_reg3_i(8)	OUTBUF_HSTL_I	V1_5	Low
Y26	IO115 PB3F10	DDR Memory Synchronous Address [9]	FPGA_DDR_A9	port_out_reg3_i(9)	OUTBUF_HSTL_I	V1_5	Low
AE29	IO117 NB3F10	DDR Memory Synchronous Address [10]	FPGA_DDR_A10	port_out_reg3_i(10)	OUTBUF_HSTL_I	V1_5	Low
AE28	IO118 NB3F11	DDR Memory Synchronous Address [11]	FPGA_DDR_A11	port_out_reg3_i(11)	OUTBUF_HSTL_I	V1_5	Low
AD28	IO118 PB3F11	DDR Memory Synchronous Address [12]	FPGA_DDR_A12	port_out_reg3_i(12)	OUTBUF_HSTL_I	V1_5	Low

Table B-7. FPGA Pin Definitions for DDR Memory

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
AD27	IO119 NB3F11	DDR Memory Synchronous Address [13]	FPGA_DDR_A13	port_out_reg3_i(13)	OUTBUF_HSTL_I	V1_5	Low
AC27	IO119 PB3F11	DDR Memory Synchronous Address [14]	FPGA_DDR_A14	port_out_reg3_i(14)	OUTBUF_HSTL_I	V1_5	Low
AA24	IO120 NB3F11	DDR Memory Synchronous Address [15]	FPGA_DDR_A15	port_out_reg3_i(15)	OUTBUF_HSTL_I	V1_5	Low
Y24	IO120 PB3F11	DDR Memory Synchronous Address [16]	FPGA_DDR_A16	port_out_reg3_i(16)	OUTBUF_HSTL_I	V1_5	Low
AB25	IO121 NB3F11	DDR Memory Synchronous Address [17]	FPGA_DDR_A17	port_out_reg3_i(17)	OUTBUF_HSTL_I	V1_5	Low
AA25	IO121 PB3F11	DDR Memory Synchronous Address [18]	FPGA_DDR_A18	port_out_reg3_i(18)	OUTBUF_HSTL_I	V1_5	Low
U28	IO101 PB3F9	DDR Memory Synchronous Data Input [0]	FPGA_DDR_D0	port_out_reg3_i(19)	OUTBUF_HSTL_I	V1_5	Low

Table B-7. FPGA Pin Definitions for DDR Memory

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
U22	IO102 PB3F9	DDR Memory Synchronous Data Input [1]	FPGA_DDR_D1	port_out_reg3_i(20)	OUTBUF_HSTL_I	V1_5	Low
U27	IO103 PB3F9	DDR Memory Synchronous Data Input [2]	FPGA_DDR_D2	port_out_reg3_i(21)	OUTBUF_HSTL_I	V1_5	Low
V29	IO104 PB3F9	DDR Memory Synchronous Data Input [3]	FPGA_DDR_D3	port_out_reg3_i(22)	OUTBUF_HSTL_I	V1_5	Low
V22	IO110 PB3F10	DDR Memory Synchronous Data Output [0]	FPGA_DDR_Q0	port_in_reg3_i(0)	INBUF_HSTL_I	V1_5	Input Only
Y29	IO111 PB3F10	DDR Memory Synchronous Data Output [1]	FPGA_DDR_Q1	port_in_reg3_i(1)	INBUF_HSTL_I	V1_5	Input Only
W25	IO112 PB3F10	DDR Memory Synchronous Data Output [2]	FPGA_DDR_Q2	port_in_reg3_i(2)	INBUF_HSTL_I	V1_5	Input Only
AA27	IO113 PB3F10	DDR Memory Synchronous Data Output [3]	FPGA_DDR_Q3	port_in_reg3_i(3)	INBUF_HSTL_I	V1_5	Input Only

Table B-7. FPGA Pin Definitions for DDR Memory

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
Y23	IO114NB3F10	DDR Memory Synchronous Load	FPGA_DDR_LD_N	port_out_reg3_i(23)	OUTBUF_HSTL_I	V1_5	High
W23	IO114PB3F10	DDR Memory Synchronous Read/Write	FPGA_DDR_RW_N	port_out_reg3_i(24)	OUTBUF_HSTL_I	V1_5	High
AA26	IO115NB3F10	DDR Memory Synchronous Byte Writes	FPGA_DDR_NWON	port_out_reg3_i(25)	OUTBUF_HSTL_I	V1_5	High

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-8 lists FPGA pin definitions for PowerQUICC II interface.

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
T6	IO223PB6F20	PowerQUICC II module presence detect	PQ2_PRESENT_N	port_in_reg6_i (54)	INBUF_LVTTL	V3_3L	Input Only	3
AD23	IO129NB4F12	PowerQUICC II Local Bus Address [31]	PQ2_BLA31	port_in_reg4_i (53)	INBUF LVTTL	V3_3L	Input Only	3
AC23	IO129PB4F12	PowerQUICC II Local Bus Address [30]	PQ2_BLA30	port_in_reg4_i (52)	INBUF LVTTL	V3_3L	Input Only	3
AK26	IO130NB4F12	PowerQUICC II Local Bus Address [29]	PQ2_BLA29	port_in_reg4_i (51)	INBUF LVTTL	V3_3L	Input Only	3
AK27	IO130PB4F12	PowerQUICC II Local Bus Address [28]	PQ2_BLA28	port_in_reg4_i (50)	INBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AF24	IO131NB4F12	PowerQUICC II Local Bus Address [27]	PQ2_BLA27	port_in_reg4_i (49)	INBUF LVTTL	V3_3L	Input Only	3
AF25	IO131PB4F12	PowerQUICC II Local Bus Address [26]	PQ2_BLA26	port_in_reg4_i (48)	INBUF LVTTL	V3_3L	Input Only	3
AG25	IO132NB4F12	PowerQUICC II Local Bus Address [25]	PQ2_BLA25	port_in_reg4_i (47)	INBUF LVTTL	V3_3L	Input Only	3
AG26	IO132PB4F12	PowerQUICC II Local Bus Address [24]	PQ2_BLA24	port_in_reg4_i (46)	INBUF LVTTL	V3_3L	Input Only	3
AD22	IO133NB4F12	PowerQUICC II Local Bus Address [23]	PQ2_BLA23	port_in_reg4_i (45)	INBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AC22	IO133PB4F12	PowerQUICC II Local Bus Address [22]	PQ2_BLA22	port_in_reg4_i (44)	INBUF LVTTL	V3_3L	Input Only	3
AE23	IO134NB4F12	PowerQUICC II Local Bus Address [21]	PQ2_BLA21	port_in_reg4_i (43)	INBUF LVTTL	V3_3L	Input Only	3
AE24	IO134PB4F12	PowerQUICC II Local Bus Address [20]	PQ2_BLA20	port_in_reg4_i (42)	INBUF LVTTL	V3_3L	Input Only	3
AH24	IO135NB4F12	PowerQUICC II Local Bus Address [19]	PQ2_BLA19	port_in_reg4_i (41)	INBUF LVTTL	V3_3L	Input Only	3
AH25	IO135PB4F12	PowerQUICC II Local Bus Address [18]	PQ2_BLA18	port_in_reg4_i (40)	INBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AJ25	IO136NB4F12	PowerQUICC II Local Bus Address [17]	PQ2_BLA17	port_in_reg4_i(39)	INBUFLVTTL	V3_3L	Input Only	3
AJ26	IO136PB4F12	PowerQUICC II Local Bus Address [16]	PQ2_BLA16	port_in_reg4_i(38)	INBUFLVTTL	V3_3L	Input Only	3
AD21	IO137NB4F12	PowerQUICC II Local Bus Address [15]	PQ2_BLA15	port_in_reg4_i(37)	INBUFLVTTL	V3_3L	Input Only	3
AK24	IO138NB4F12	PowerQUICC II Local Bus Write Enable [3]	PQ2_BLWE3_N	port_in_reg4_i(36)	INBUFLVTTL	V3_3L	Input Only	3
AK25	IO138PB4F12	PowerQUICC II Local Bus Write Enable [2]	PQ2_BLWE2_N	port_in_reg4_i(35)	INBUFLVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AE21	IO139NB4F13	PowerQUICC II Local Bus Write Enable [1]	PQ2_BLWE1_N	port_in_reg4_i(34)	INBUFLVTTL	V3_3L	Input Only	3
AE22	IO139PB4F13	PowerQUICC II Local Bus Write Enable [0]	PQ2_BLWE0_N	port_in_reg4_i(33)	INBUFLVTTL	V3_3L	Input Only	3
AG23	IO140NB4F13	PowerQUICC II Local Bus Write	PQ2_BLWR_N	port_in_reg4_i(32)	INBUFLVTTL	V3_3L	Input Only	3
AG24	IO140PB4F13	PowerQUICC II Local Bus Data [31]	PQ2_BLD31	port_out_reg4_i(0), port_out_enable4_i(3), port_in_reg4_i(0)	BIBUFLVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AF22	IO141NB4F13	PowerQUICC II Local Bus Data [30]	PQ2_BLD30	port_out_reg4_i(1), port_out_enable4_i(3), port_in_reg4_i(1)	BIBUF LVTTL	V3_3L	Input Only	3
AF23	IO141PB4F13	PowerQUICC II Local Bus Data [29]	PQ2_BLD29	port_out_reg4_i(2), port_out_enable4_i (3), port_in_reg4_i(2)	BIBUF LVTTL	V3_3L	Input Only	3
AJ23	IO142NB4F13	PowerQUICC II Local Bus Data [28]	PQ2_BLD28	port_out_reg4_i(3), port_out_enable4_i (3), port_in_reg4_i(3)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AJ24	IO142PB4F13	PowerQUICC II Local Bus Data [27]	PQ2_BLD27	port_out_reg4_i(4), port_out_enable4_i (3), port_in_reg4_i(4)	BIBUF LVTTL	V3_3L	Input Only	3
AD19	IO143NB4F13	PowerQUICC II Local Bus Data [26]	PQ2_BLD26	port_out_reg4_i(5), port_out_enable4_i (3), port_in_reg4_i(5)	BIBUF LVTTL	V3_3L	Input Only	3
AD20	IO143PB4F13	PowerQUICC II Local Bus Data [25]	PQ2_BLD25	port_out_reg4_i(6), port_out_enable4_i (3), port_in_reg4_i(6)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AG21	IO144NB4F13	PowerQUICC II Local Bus Data [24]	PQ2_BLD24	port_out_reg4_i(7), port_out_enable4_i (3), port_in_reg4_i(7)	BIBUF LVTTL	V3_3L	Input Only	3
AG22	IO144PB4F13	PowerQUICC II Local Bus Data [23]	PQ2_BLD23	port_out_reg4_i(8), port_out_enable4_i (2), port_in_reg4_i(8)	BIBUF LVTTL	V3_3L	Input Only	3
AE19	IO145NB4F13	PowerQUICC II Local Bus Data [22]	PQ2_BLD22	port_out_reg4_i(9), port_out_enable4_i (2), port_in_reg4_i(9)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AE20	IO145PB4F13	PowerQUICC II Local Bus Data [21]	PQ2_BLD21	port_out_reg4_i (10), port_out_enable4_i (2), port_in_reg4_i (10)	BIBUF LVTTL	V3_3L	Input Only	3
AF20	IO146NB4F13	PowerQUICC II Local Bus Data [20]	PQ2_BLD20	port_out_reg4_i (11), port_out_enable4_i (2), port_in_reg4_i (11)	BIBUF LVTTL	V3_3L	Input Only	3
AF21	IO146PB4F13	PowerQUICC II Local Bus Data [19]	PQ2_BLD19	port_out_reg4_i (12), port_out_enable4_i (2), port_in_reg4_i (12)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AC19	IO147NB4F13	PowerQUICC II Local Bus Data [18]	PQ2_BLD18	port_out_reg4_i (13), port_out_enable4_i (2), port_in_reg4_i (13)	BIBUF LVTTL	V3_3L	Input Only	3
AC20	IO147PB4F13	PowerQUICC II Local Bus Data [17]	PQ2_BLD17	port_out_reg4_i (14), port_out_enable4_i (2), port_in_reg4_i (14)	BIBUF LVTTL	V3_3L	Input Only	3
AH22	IO148NB4F13	PowerQUICC II Local Bus Data [16]	PQ2_BLD16	port_out_reg4_i (15), port_out_enable4_i (2), port_in_reg4_i (15)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AH23	IO148PB4F13	PowerQUICC II Local Bus Data [15]	PQ2_BLD15	port_out_reg4_i (16), port_out_enable4_i (1), port_in_reg4_i (16)	BIBUF LVTTL	V3_3L	Input Only	3
AC18	IO149NB4F13	PowerQUICC II Local Bus Data [14]	PQ2_BLD14	port_out_reg4_i (17), port_out_enable4_i (1), port_in_reg4_i (17)	BIBUF LVTTL	V3_3L	Input Only	3
AB18	IO149PB4F13	PowerQUICC II Local Bus Data [13]	PQ2_BLD13	port_out_reg4_i (18), port_out_enable4_i (1), port_in_reg4_i (18)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AK21	IO150NB4F13	PowerQUICC II Local Bus Data [12]	PQ2_BLD12	port_out_reg4_i(19), port_out_enable4_i (1), port_in_reg4_i(19)	BIBUF LVTTL	V3_3L	Input Only	3
AJ21	IO150PB4F13	PowerQUICC II Local Bus Data [11]	PQ2_BLD11	port_out_reg4_i(20), port_out_enable4_i (1), port_in_reg4_i(20)	BIBUF LVTTL	V3_3L	Input Only	3
AE18	IO151NB4F13	PowerQUICC II Local Bus Data [10]	PQ2_BLD10	port_out_reg4_i(21), port_out_enable4_i (1), port_in_reg4_i(21)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AD18	IO151PB4F13	Power-QUICC II Local Bus Data [9]	PQ2_BLD9	port_out_reg4_i (22), port_out_enable4_i (1), port_in_reg4_i (22)	BIBUF LVTTL	V3_3L	Input Only	3
AJ20	IO152NB4F14	Power-QUICC II Local Bus Data [8]	PQ2_BLD8	port_out_reg4_i (23), port_out_enable4_i (1), port_in_reg4_i (23)	BIBUF LVTTL	V3_3L	Input Only	3
AK20	IO152PB4F14	Power-QUICC II Local Bus Data [7]	PQ2_BLD7	port_out_reg4_i (24), port_out_enable4_i (0), port_in_reg4_i (24)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AG19	IO153 NB4F14	Power-QUICC II Local Bus Data [6]	PQ2_BL D6	port_out_reg4_i (25), port_out_enable4_i (0), port_in_reg4_i (25)	BIBUF LVTTL	V3_3L	Input Only	3
AG20	IO153P B4F14	Power-QUICC II Local Bus Data [5]	PQ2_BL D5	port_out_reg4_i (26), port_out_enable4_i (0), port_in_reg4_i (26)	BIBUF LVTTL	V3_3L	Input Only	3
AH19	IO154 NB4F14	Power-QUICC II Local Bus Data [4]	PQ2_BL D4	port_out_reg4_i (27), port_out_enable4_i (0), port_in_reg4_i (27)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AH20	IO154PB4F14	PowerQUICC II Local Bus Data [3]	PQ2_BLD3	port_out_reg4_i (28), port_out_enable4_i (0), port_in_reg4_i (28)	BIBUF LVTTL	V3_3L	Input Only	3
AC17	IO155NB4F14	PowerQUICC II Local Bus Data [2]	PQ2_BLD2	port_out_reg4_i (29), port_out_enable4_i (0), port_in_reg4_i (29)	BIBUF LVTTL	V3_3L	Input Only	3
AB17	IO155PB4F14	PowerQUICC II Local Bus Data [1]	PQ2_BLD1	port_out_reg4_i (30), port_out_enable4_i (0), port_in_reg4_i (30)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AK19	IO156 NB4F14	Power-QUICC II Local Bus Data [0]	PQ2_BLD0	port_out_reg4_i (31), port_out_enable4_i (0), port_in_reg4_i (31)	BIBUF LVTTL	V3_3L	Input Only	3
AJ19	IO156PB4F14	Power-QUICC II Chip Select[7]	PQ2_BCS7_N	port_in_reg4_i (57)	INBUF LVTTL	V3_3L	Input Only	3
AE17	IO157 NB4F14	Power-QUICC II Chip Select[6]	PQ2_BCS6_N	port_in_reg4_i (56)	INBUF LVTTL	V3_3L	Input Only	3
AD17	IO157PB4F14	Power-QUICC II Chip Select[5]	PQ2_BCS5_N	port_in_reg4_i (55)	INBUF LVTTL	V3_3L	Input Only	3
AJ17	IO158 NB4F14	Power-QUICC II Chip Select[4]	PQ2_BCS4_N	port_in_reg4_i (54)	INBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AE7	IO187NB5F17	PowerQUICC II General Purpose I/O Port[0]	PQ2_BLGPL0	port_out_reg5_i(6)	INBUFLVTTL	V3_3L	Input Only	3
AE8	IO187PB5F17	PowerQUICC II General Purpose I/O Port[1]	PQ2_BLGPL1	port_out_reg5_i(7)	INBUFLVTTL	V3_3L	Input Only	3
AF6	IO188NB5F17	PowerQUICC II General Purpose I/O Port[2]	PQ2_BLGPL2	port_out_reg5_i(8)	INBUFLVTTL	V3_3L	Input Only	3
AF7	IO188PB5F17	PowerQUICC II General Purpose I/O Port[3]	PQ2_BLGPL3	port_out_reg5_i(9)	INBUFLVTTL	V3_3L	Input Only	3
AD8	IO189NB5F17	PowerQUICC II General Purpose I/O Port[4]	PQ2_BLGPL4	port_out_reg5_i(10)	INBUFLVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AD9	IO189PB5F17	PowerQUICC II General Purpose I/O Port[5]	PQ2_BLGPL5	port_out_reg5_i(11)	INBUFLVTTL	V3_3L	Input Only	3
AH6	IO190NB5F17	PowerQUICC II Interrupt Request[5]	PQ2_IRQ5_N	port_out_reg5_i(42)	OUTBUFLVTTL	V3_3L		
AG6	IO190PB5F17	PowerQUICC II Interrupt Request[6]	PQ2_IRQ6_N	port_out_reg5_i(43)	OUTBUFLVTTL	V3_3L		
AG5	IO191NB5F17	PowerQUICC II Interrupt Request[7]	PQ2_IRQ7_N	port_out_reg5_i(44)	OUTBUFLVTTL	V3_3L		
AH5	IO191PB5F17	FPGA TO PowerQUICC II Spare Connection	FPGA_PQ2_SPARE0_T	port_out_reg5_i(45), port_out_enable5_i (0), port_in_reg5_i(12)	BIBUFLVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AC8	IO192NB5F17	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE1_T	port_out_reg5_i (46), port_out_enable5_i (1), port_in_reg5_i (13)	BIBUF LVTTL	V3_3L	Input Only	3
AC9	IO192PB5F17	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE2_T	port_out_reg5_i (47), port_out_enable5_i (2), port_in_reg5_i (14)	BIBUF LVTTL	V3_3L	Input Only	3
U7	IO217NB6F20	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE3_T	port_out_reg6_i (0), port_out_enable6_i (0), port_in_reg6_i (48)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
U6	IO217PB6F20	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE4_T	port_out_reg6_i (1), port_out_enable6_i (1), port_in_reg6_i (49)	BIBUF LVTTL	V3_3L	Input Only	3
U4	IO218NB6F20	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE5_T	port_out_reg6_i (2), port_out_enable6_i (2), port_in_reg6_i (50)	BIBUF LVTTL	V3_3L	Input Only	3
V4	IO218PB6F20	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE6_T	port_out_reg6_i (3), port_out_enable6_i (3), port_in_reg6_i (51)	BIBUF LVTTL	V3_3L	Input Only	3

Table B-8. PowerQUICC II Interface Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
T5	IO219 NB6F2 0	FPGA TO Power-QUICC II Spare Connection	FPGA_PQ2_SPARE7_T	port_out_reg6_i (4), port_out_enable6_i (4), port_in_reg6_i (52)	BIBUF LVTTL	V3_3L	Input Only	3

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Note: (3) This signal must be used as an input only, unless the PowerQUICC II Processor Module is not attached to the Axcelerator Motherboard.

Table B-9 lists FPGA pin definitions for Hex Ethernet TX, RX, and Control.

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AE14	IO163NB 5F15	Hex Fast Ethernet Transmit Port [0], Data [0]	HEX_TX D0_0	port_out_ reg5_i(0)	OUT-BUF LVTTL	V3_3L	Low
AD14	IO163PB5 F15	Hex Fast Ethernet Transmit Port [0], Data [1]	HEX_TX D0_1	port_out_ reg5_i(1)	OUT-BUF LVTTL	V3_3L	Low
AJ12	IO164NB 5F15	Hex Fast Ethernet Transmit Port [0], Data [2]	HEX_TX D0_2	port_out_ reg5_i(2)	OUT-BUF LVTTL	V3_3L	Low
AJ13	IO164PB5 F15	Hex Fast Ethernet Transmit Port [0], Data [3]	HEX_TX D0_3	port_out_ reg5_i(3)	OUT-BUF LVTTL	V3_3L	Low
AB14	IO165NB 5F15	Hex Fast Ethernet Transmit Port [1], Data [0]	HEX_TX D1_0	port_out_ reg5_i(4)	OUT-BUF LVTTL	V3_3L	Low
AC15	IO165PB5 F15	Hex Fast Ethernet Transmit Port [1], Data [1]	HEX_TX D1_1	port_out_ reg5_i(5)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AK11	IO166NB 5F15	Hex Fast Ethernet Transmit Port [1], Data [2]	HEX_TX D1_2	port_out_ reg5_i(6)	OUT-BUF LVTTL	V3_3L	Low
AK12	IO166PB5 F15	Hex Fast Ethernet Transmit Port [1], Data [3]	HEX_TX D1_3	port_out_ reg5_i(7)	OUT-BUF LVTTL	V3_3L	Low
AB13	IO167NB 5F15	Hex Fast Ethernet Transmit Port [2], Data [0]	HEX_TX D2_0	port_out_ reg5_i(8)	OUT-BUF LVTTL	V3_3L	Low
AC14	IO167PB5 F15	Hex Fast Ethernet Transmit Port [2], Data [1]	HEX_TX D2_1	port_out_ reg5_i(9)	OUT-BUF LVTTL	V3_3L	Low
AH11	IO168NB 5F15	Hex Fast Ethernet Transmit Port [2], Data [2]	HEX_TX D2_2	port_out_ reg5_i(10)	OUT-BUF LVTTL	V3_3L	Low
AH12	IO168PB5 F15	Hex Fast Ethernet Transmit Port [2], Data [3]	HEX_TX D2_3	port_out_ reg5_i(11)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AD13	IO169NB 5F15	Hex Fast Ethernet Transmit Port [3], Data [0]	HEX_TX D3_0	port_out_ reg5_i(12)	OUT-BUF LVTTL	V3_3L	Low
AC13	IO169PB5 F15	Hex Fast Ethernet Transmit Port [3], Data [1]	HEX_TX D3_1	port_out_ reg5_i(13)	OUT-BUF LVTTL	V3_3L	Low
AJ10	IO170NB 5F15	Hex Fast Ethernet Transmit Port [3], Data [2]	HEX_TX D3_2	port_out_ reg5_i(14)	OUT-BUF LVTTL	V3_3L	Low
AJ11	IO170PB5 F15	Hex Fast Ethernet Transmit Port [3], Data [3]	HEX_TX D3_3	port_out_ reg5_i(15)	OUT-BUF LVTTL	V3_3L	Low
AG11	IO171NB 5F16	Hex Fast Ethernet Transmit Port [4], Data [0]	HEX_TX D4_0	port_out_ reg5_i(16)	OUT-BUF LVTTL	V3_3L	Low
AG12	IO171PB5 F16	Hex Fast Ethernet Transmit Port [4], Data [1]	HEX_TX D4_1	port_out_ reg5_i(17)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AK9	IO172NB 5F16	Hex Fast Ethernet Transmit Port [4], Data [2]	HEX_TX D4_2	port_out_ reg5_i(18)	OUT-BUF LVTTL	V3_3L	Low
AK10	IO172PB5 F16	Hex Fast Ethernet Transmit Port [4], Data [3]	HEX_TX D4_3	port_out_ reg5_i(19)	OUT-BUF LVTTL	V3_3L	Low
AE12	IO173NB 5F16	Hex Fast Ethernet Transmit Port [5], Data [0]	HEX_TX D5_0	port_out_ reg5_i(20)	OUT-BUF LVTTL	V3_3L	Low
AE13	IO173PB5 F16	Hex Fast Ethernet Transmit Port [5], Data [1]	HEX_TX D5_1	port_out_ reg5_i(21)	OUT-BUF LVTTL	V3_3L	Low
AG9	IO174NB 5F16	Hex Fast Ethernet Transmit Port [5], Data [2]	HEX_TX D5_2	port_out_ reg5_i(22)	OUT-BUF LVTTL	V3_3L	Low
AG10	IO174PB5 F16	Hex Fast Ethernet Transmit Port [5], Data [3]	HEX_TX D5_3	port_out_ reg5_i(23)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AE11	IO175NB 5F16	Hex Fast Ethernet Transmit Enable Port [0]	HEX_TX_ EN0	port_out_ reg5_i(24)	OUT-BUF LVTTL	V3_3L	Low
AF11	IO175PB5 F16	Hex Fast Ethernet Transmit Enable Port [1]	HEX_TX_ EN1	port_out_ reg5_i(25)	OUT-BUF LVTTL	V3_3L	Low
AH8	IO176NB 5F16	Hex Fast Ethernet Transmit Enable Port [2]	HEX_TX_ EN2	port_out_ reg5_i(26)	OUT-BUF LVTTL	V3_3L	Low
AH9	IO176PB5 F16	Hex Fast Ethernet Transmit Enable Port [3]	HEX_TX_ EN3	port_out_ reg5_i(27)	OUT-BUF LVTTL	V3_3L	Low
AC12	IO177NB 5F16	Hex Fast Ethernet Transmit Enable Port [4]	HEX_TX_ EN4	port_out_ reg5_i(28)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AD12	IO177PB5 F16	Hex Fast Ethernet Transmit Enable Port [5]	HEX_TX_ EN5	port_out_ reg5_i(29)	OUT-BUF LVTTL	V3_3L	Low
AJ7	IO178NB 5F16	Hex Fast Ethernet Transmit Coding Error Port [0]	HEX_TX_ ER0	port_out_ reg5_i(30)	OUT-BUF LVTTL	V3_3L	Low
AJ8	IO178PB5 F16	Hex Fast Ethernet Transmit Coding Error Port [1]	HEX_TX_ ER1	port_out_ reg5_i(31)	OUT-BUF LVTTL	V3_3L	Low
AF9	IO179NB 5F16	Hex Fast Ethernet Transmit Coding Error Port [2]	HEX_TX_ ER2	port_out_ reg5_i(32)	OUT-BUF LVTTL	V3_3L	Low
AF10	IO179PB5 F16	Hex Fast Ethernet Transmit Coding Error Port [3]	HEX_TX_ ER3	port_out_ reg5_i(33)	OUT-BUF LVTTL	V3_3L	Low

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AE9	IO180NB 5F16	Hex Fast Ethernet Transmit Coding Error Port [4]	HEX_TX_ ER4	port_out_ reg5_i(34)	OUT-BUF LVTTL	V3_3L	Low
AE10	IO180PB5 F16	Hex Fast Ethernet Transmit Coding Error Port [5]	HEX_TX_ ER5	port_out_ reg5_i(35)	OUT-BUF LVTTL	V3_3L	Low
AB7	IO193NB 6F18	Hex Fast Ethernet Receive Port [0], Data [0]	HEX_RX D0_0	port_in_reg 6_i(0)	INBUF LVTTL	V3_3L	Input Only
AC7	IO193PB6 F18	Hex Fast Ethernet Receive Port [0], Data [1]	HEX_RX D0_1	port_in_reg 6_i(1)	INBUF LVTTL	V3_3L	Input Only
AD5	IO194NB 6F18	Hex Fast Ethernet Receive Port [0], Data [2]	HEX_RX D0_2	port_in_reg 6_i(2)	INBUF LVTTL	V3_3L	Input Only
AE5	IO194PB6 F18	Hex Fast Ethernet Receive Port [0], Data [3]	HEX_RX D0_3	port_in_reg 6_i(3)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AB6	IO195NB 6F18	Hex Fast Ethernet Receive Port [1], Data [0]	HEX_RX D1_0	port_in_reg 6_i(4)	INBUF LVTTL	V3_3L	Input Only
AC6	IO195PB6 F18	Hex Fast Ethernet Receive Port [1], Data [1]	HEX_RX D1_1	port_in_reg 6_i(5)	INBUF LVTTL	V3_3L	Input Only
AE4	IO196NB 6F18	Hex Fast Ethernet Receive Port [1], Data [2]	HEX_RX D1_2	port_in_reg 6_i(6)	INBUF LVTTL	V3_3L	Input Only
AF4	IO196PB6 F18	Hex Fast Ethernet Receive Port [1], Data [3]	HEX_RX D1_3	port_in_reg 6_i(7)	INBUF LVTTL	V3_3L	Input Only
AA8	IO197NB 6F18	Hex Fast Ethernet Receive Port [2], Data [0]	HEX_RX D2_0	port_in_reg 6_i(8)	INBUF LVTTL	V3_3L	Input Only
AB8	IO197PB6 F18	Hex Fast Ethernet Receive Port [2], Data [1]	HEX_RX D2_1	port_in_reg 6_i(9)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AF3	IO198NB 6F18	Hex Fast Ethernet Receive Port [2], Data [2]	HEX_RX D2_2	port_in_reg 6_i(10)	INBUF LVTTL	V3_3L	Input Only
AG3	IO198PB6 F18	Hex Fast Ethernet Receive Port [2], Data [3]	HEX_RX D2_3	port_in_reg 6_i(11)	INBUF LVTTL	V3_3L	Input Only
AC4	IO199NB 6F18	Hex Fast Ethernet Receive Port [3], Data [0]	HEX_RX D3_0	port_in_reg 6_i(12)	INBUF LVTTL	V3_3L	Input Only
AD4	IO199PB6 F18	Hex Fast Ethernet Receive Port [3], Data [1]	HEX_RX D3_1	port_in_reg 6_i(13)	INBUF LVTTL	V3_3L	Input Only
AB5	IO200NB 6F18	Hex Fast Ethernet Receive Port [3], Data [2]	HEX_RX D3_2	port_in_reg 6_i(14)	INBUF LVTTL	V3_3L	Input Only
AC5	IO200PB6 F18	Hex Fast Ethernet Receive Port [3], Data [3]	HEX_RX D3_3	port_in_reg 6_i(15)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
Y7	IO201NB 6F18	Hex Fast Ethernet Receive Port [4], Data [0]	HEX_RX D4_0	port_in_reg 6_i(16)	INBUF LVTTL	V3_3L	Input Only
AA7	IO201PB6 F18	Hex Fast Ethernet Receive Port [4], Data [1]	HEX_RX D4_1	port_in_reg 6_i(17)	INBUF LVTTL	V3_3L	Input Only
AD3	IO202NB 6F18	Hex Fast Ethernet Receive Port [4], Data [2]	HEX_RX D4_2	port_in_reg 6_i(18)	INBUF LVTTL	V3_3L	Input Only
AE3	IO202PB6 F18	Hex Fast Ethernet Receive Port [4], Data [3]	HEX_RX D4_3	port_in_reg 6_i(19)	INBUF LVTTL	V3_3L	Input Only
Y6	IO203NB 6F19	Hex Fast Ethernet Receive Port [5], Data [0]	HEX_RX D5_0	port_in_reg 6_i(20)	INBUF LVTTL	V3_3L	Input Only
AA6	IO203PB6 F19	Hex Fast Ethernet Receive Port [5], Data [1]	HEX_RX D5_1	port_in_reg 6_i(21)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
Y5	IO204NB6F19	Hex Fast Ethernet Receive Port [5], Data [2]	HEX_RXD5_2	port_in_reg6_i(22)	INBUF LVTTL	V3_3L	Input Only
AA5	IO204PB6F19	Hex Fast Ethernet Receive Port [5], Data [3]	HEX_RXD5_3	port_in_reg6_i(23)	INBUF LVTTL	V3_3L	Input Only
W8	IO205NB6F19	Hex Fast Ethernet Carrier Sense Port [0]	HEX_CRS0	port_in_reg6_i(24)	INBUF LVTTL	V3_3L	Input Only
Y8	IO205PB6F19	Hex Fast Ethernet Carrier Sense Port [1]	HEX_CRS1	port_in_reg6_i(25)	INBUF LVTTL	V3_3L	Input Only
AA4	IO206NB6F19	Hex Fast Ethernet Carrier Sense Port [2]	HEX_CRS2	port_in_reg6_i(26)	INBUF LVTTL	V3_3L	Input Only
AB4	IO206PB6F19	Hex Fast Ethernet Carrier Sense Port [3]	HEX_CRS3	port_in_reg6_i(27)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
W6	IO207NB6F19	Hex Fast Ethernet Carrier Sense Port [4]	HEX_CRS4	port_in_reg6_i(28)	INBUF LVTTL	V3_3L	Input Only
W7	IO207PB6F19	Hex Fast Ethernet Carrier Sense Port [5]	HEX_CRS5	port_in_reg6_i(29)	INBUF LVTTL	V3_3L	Input Only
AB3	IO208NB6F19	Hex Fast Ethernet Collision Port [0]	HEX_COL0	port_in_reg6_i(30)	INBUF LVTTL	V3_3L	Input Only
AC3	IO208PB6F19	Hex Fast Ethernet Collision Port [1]	HEX_COL1	port_in_reg6_i(31)	INBUF LVTTL	V3_3L	Input Only
V8	IO209NB6F19	Hex Fast Ethernet Collision Port [2]	HEX_COL2	port_in_reg6_i(32)	INBUF LVTTL	V3_3L	Input Only
V9	IO209PB6F19	Hex Fast Ethernet Collision Port [3]	HEX_COL3	port_in_reg6_i(33)	INBUF LVTTL	V3_3L	Input Only
AA2	IO210NB6F19	Hex Fast Ethernet Collision Port [4]	HEX_COL4	port_in_reg6_i(34)	INBUF LVTTL	V3_3L	Input Only
AA1	IO210PB6F19	Hex Fast Ethernet Collision Port [5]	HEX_COL5	port_in_reg6_i(35)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
V5	IO211NB 6F19	Hex Fast Ethernet Receive Error Port [0]	HEX_RX_ ER0	port_in_reg 6_i(36)	INBUF LVTTL	V3_3L	Input Only
W5	IO211PB6 F19	Hex Fast Ethernet Receive Error Port [1]	HEX_RX_ ER1	port_in_reg 6_i(37)	INBUF LVTTL	V3_3L	Input Only
Y3	IO212NB 6F19	Hex Fast Ethernet Receive Error Port [2]	HEX_RX_ ER2	port_in_reg 6_i(38)	INBUF LVTTL	V3_3L	Input Only
Y4	IO212PB6 F19	Hex Fast Ethernet Receive Error Port [3]	HEX_RX_ ER3	port_in_reg 6_i(39)	INBUF LVTTL	V3_3L	Input Only
V7	IO213NB 6F19	Hex Fast Ethernet Receive Error Port [4]	HEX_RX_ ER4	port_in_reg 6_i(40)	INBUF LVTTL	V3_3L	Input Only
V6	IO213PB6 F19	Hex Fast Ethernet Receive Error Port [5]	HEX_RX_ ER5	port_in_reg 6_i(41)	INBUF LVTTL	V3_3L	Input Only

Table B-9. Hex Ethernet TX, RX, and Control Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
AG7	IO184NB 5F17	Hex Fast Ethernet Receive Data Valid Port [0]	HEX_RX_ DV0	port_in_reg 5_i(0)	INBUF LVTTL	V3_3L	Input Only
AH7	IO184PB5 F17	Hex Fast Ethernet Receive Data Valid Port [1]	HEX_RX_ DV1	port_in_reg 5_i(1)	INBUF LVTTL	V3_3L	Input Only
AC10	IO185NB 5F17	Hex Fast Ethernet Receive Data Valid Port [2]	HEX_RX_ DV2	port_in_reg 5_i(2)	INBUF LVTTL	V3_3L	Input Only
AD10	IO185PB5 F17	Hex Fast Ethernet Receive Data Valid Port [3]	HEX_RX_ DV3	port_in_reg 5_i(3)	INBUF LVTTL	V3_3L	Input Only
AJ5	IO186NB 5F17	Hex Fast Ethernet Receive Data Valid Port [4]	HEX_RX_ DV4	port_in_reg 5_i(4)	INBUF LVTTL	V3_3L	Input Only
AJ6	IO186PB5 F17	Hex Fast Ethernet Receive Data Valid Port [5]	HEX_RX_ DV5	port_in_reg 5_i(5)	INBUF LVTTL	V3_3L	Input Only

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally

shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-10 lists the FPGA pin definitions for LVDS Loopback.

Table B-10. LVDS Loopback Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
F22	IO52NB1F4	LVDS Signal from External Chip, Data[0]	FPGA_LVDS_CIR_IN_N0	port_in_reg1_i(17)	INBUF_LVDS	V2_5	LVDS input pair only
E22	IO52PB1F4	LVDS Signal from External Chip, Data[0]	FPGA_LVDS_CIR_IN_P0	port_in_reg1_i(17)	INBUF_LVDS	V2_5	LVDS input pair only
F23	IO55NB1F5	LVDS Signal from External Chip, Data[1]	FPGA_LVDS_CIR_IN_N1	port_in_reg1_i(18)	INBUF_LVDS	V2_5	LVDS input pair only
E23	IO55PB1F5	LVDS Signal from External Chip, Data[1]	FPGA_LVDS_CIR_IN_P1	port_in_reg1_i(18)	INBUF_LVDS	V2_5	LVDS input pair only
L23	IO74NB2F7	LVDS Signal to External Chip, Data[0]	FPGA_LVDS_CIR_OUT_N0	port_out_reg2_i(18)	OUTBUF_LVDS	V2_5	Low

Table B-10. LVDS Loopback Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
L24	IO74PB2F7	LVDS Signal from External Chip, Data[0]	FPGA_LVDS_CIR_OUT_P0	port_out_reg2_i(18)	OUTBUF_LVDS	V2_5	High
K25	IO68NB2F6	LVDS Signal to External Chip, Data[1]	FPGA_LVDS_CIR_OUT_N1	port_out_reg2_i(19)	OUTBUF_LVDS	V2_5	Low
K24	IO68PB2F6	LVDS Signal to External Chip, Data[1]	FPGA_LVDS_CIR_OUT_P1	port_out_reg2_i(19)	OUTBUF_LVDS	V2_5	High
H17	IO36NB1F3	LVDS Signal Loopback Input, Data[0]	FPGA_LVDS_LOOP0_N_T	port_in_reg1_i(19)	INBUF_LVDS	V2_5	LVDS input pair only
J17	IO36PB1F3	LVDS Signal Loopback Input, Data[0]	FPGA_LVDS_LOOP0_P_T	port_in_reg1_i(19)	INBUF_LVDS	V2_5	LVDS input pair only
H18	IO38NB1F3	LVDS Signal Loopback Input, Data[1]	FPGA_LVDS_LOOP1_N_T	port_in_reg1_i(20)	INBUF_LVDS	V2_5	LVDS input pair only

Table B-10. LVDS Loopback Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
J18	IO38PB1F3	LVDS Signal Loopback Input, Data[1]	FPGA_LVDS_LOOP1_P_T	port_in_reg1_i(20)	INBUF_LVDS	V2_5	LVDS input pair only
H19	IO48NB1F4	LVDS Signal Loopback Input, Data[2]	FPGA_LVDS_LOOP2_N_T	port_in_reg1_i(21)	INBUF_LVDS	V2_5	LVDS input pair only
G19	IO48PB1F4	LVDS Signal Loopback Input, Data[2]	FPGA_LVDS_LOOP2_P_T	port_in_reg1_i(21)	INBUF_LVDS	V2_5	LVDS input pair only
G20	IO50NB1F4	LVDS Signal Loopback Input, Data[3]	FPGA_LVDS_LOOP3_N_T	port_in_reg1_i(22)	INBUF_LVDS	V2_5	LVDS input pair only
H20	IO50PB1F4	LVDS Signal Loopback Input, Data[3]	FPGA_LVDS_LOOP3_P_T	port_in_reg1_i(22)	INBUF_LVDS	V2_5	LVDS input pair only
R22	IO94NB2F8	LVDS Signal Loopback Output, Data[0]	FPGA_LVDS_LOOP0_N	port_out_reg2_i(20)	OUTBUF_LVDS	V2_5	Low

Table B-10. LVDS Loopback Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
R23	IO94PB2F8	LVDS Signal Loopback Output, Data[0]	FPGA_LVDS_LOOP0_P	port_out_reg2_i(20)	OUTBUF_LVDS	V2_5	High
P22	IO90NB2F8	LVDS Signal Loopback Output, Data[1]	FPGA_LVDS_LOOP1_N	port_out_reg2_i(21)	OUTBUF_LVDS	V2_5	Low
P23	IO90PB2F8	LVDS Signal Loopback Output, Data[1]	FPGA_LVDS_LOOP1_P	port_out_reg2_i(21)	OUTBUF_LVDS	V2_5	High
N22	IO84NB2F7	LVDS Signal Loopback Output, Data[2]	FPGA_LVDS_LOOP2_N	port_out_reg2_i(22)	OUTBUF_LVDS	V2_5	Low
N23	IO84PB2F7	LVDS Signal Loopback Output, Data[2]	FPGA_LVDS_LOOP2_P	port_out_reg2_i(22)	OUTBUF_LVDS	V2_5	High
M23	IO80NB2F7	LVDS Signal Loopback Output, Data[3]	FPGA_LVDS_LOOP3_N	port_out_reg2_i(23)	OUTBUF_LVDS	V2_5	Low

Table B-10. LVDS Loopback Pin Definitions

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIPTION	SCHEMATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFER TYPE	POWER DOMAIN	REQUIRED DEFAULT LOGIC LEVEL *
M24	IO80PB2F7	LVDS Signal Loopback Output, Data[3]	FPGA_LVDS_LOOP3_P	port_out_reg2_i(23)	OUTBUF_LVDS	V2_5	High

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-11 lists the FPGA pin definitions for the GTL+ Loopback.

Table B-11. FPGA Pin Definitions for GTL + Loopback

FPGA PIN No.	FPGA PIN NAME	SIGNAL DESCRIP-TION	SCHEM-ATIC NET NAME	FPGA I/O RING NET NAME	FPGA BUFFE R TYPE	POWER DO-MAIN	RE-QUIRED DEFAULT LOGIC LEVEL *
K4	IO242N B7F22	GTL Signal to External Chip, Data[0]	FPGA_ GTL_D0_ IN	port_out_ reg7_i(21)	OUTBUF _GTLP25	Selectable	Low
L4	IO242P B7F22	GTL Signal to External Chip, Data[1]	FPGA_ GTL_D1_ IN	port_out_ reg7_i(22)	OUTBUF _GTLP25	Selectable	Low
H7	IO257N B7F23	GTL Signal from Exter-nal Chip, Data[0]	FPGA_ GTL_D0_ OUT	port_in_ reg7_i(11)	INBUF_ GTLP25	Selectable	Input Only
J7	IO257P B7F23	GTL Signal from Exter-nal Chip, Data[1]	FPGA_ GTL_D1_ OUT	port_in_ reg7_i(12)	INBUF_ GTLP25	Selectable	Input Only

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-12 lists the FPGA pin definitions for the LVPECL LOOPBACK.

Table B-12. LVPECL LoopBack Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schem-atic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Required Default Logic Level
A10	IO15N B0F1	LVPECL Signal to External Chip Data[0]	FPGA_LVPECL_D0N_IN	port_out_reg0_i (15)	OUTBUF_LVPECL	Low
A9	IO15PB 0F1	LVPECL Signal to External Chip Data[0]	FPGA_LVPECL_D0P_IN	port_out_reg0_i (15)	OUTBUF_LVPECL	High
H12	IO16N B0F1	LVPECL Signal to External Chip Data[1]	FPGA_LVPECL_D1N_IN	port_out_reg0_i (16)	OUTBUF_LVPECL	Low
H11	IO16PB 0F1	LVPECL Signal to External Chip Data[1]	FPGA_LVPECL_D1P_IN	port_out_reg0_i (16)	OUTBUF_LVPECL	High
H14	IO28N B0F2	LVPECL Signal from External Chip Data[0]	FPGA_LVPECL_D0N_OUT_T	port_in_reg0_i (35)	INBUF_LVPECL	LVPECL input pair only
J14	IO28PB 0F2	LVPECL Signal from External Chip Data[0]	FPGA_LVPECL_D0P_OUT_T	port_in_reg0_i (35)	INBUF_LVPECL	LVPECL input pair only
B15	IO29N B0F2	LVPECL Signal from External Chip Data[1]	FPGA_LVPECL_D1N_OUT_T	port_in_reg0_i (36)	INBUF_LVPECL	LVPECL input pair only

Table B-12. LVPECL LoopBack Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Required Default Logic Level
A15	IO29PB 0F2	LVPECL Signal from External Chip Data[1]	FPGA_LVPECL_D1P_OUT_T	port_in_reg0_i (36)	INBUF_ LVPECL	LVPECL input pair only

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-13 lists the pin definitions for the LVCMOS Loopback.

Table B-13. LVCMOS LoopBack Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Required Default Logic Level
R7	IO225NB7F21	LVCMOS Signal to External Chip, Data[0]	FPGA_LVCMOS_D0	port_out_reg7_i(0)	OUTBUF_LVCMOS25	Selectable	Low
N9	IO237PB7F22	LVCMOS Signal from External Chip, Data[0]	LVCMOS_FPGA_D0	port_in_reg6_i(53)	INBUF_LVCMOS25	Selectable	

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Table B-14 lists the FPGA pin definitions for Misc. Signals.

Table B-14. Misc. Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	FPGA Buffer Type	Power Domain	Note
U5	IO219PB6F20	PLL Block A Lock Indicator	PLL_A_LOCK_N	port_out_reg6_i(5)	OUTBUF LVTTL	V3_3L	4
U3	IO220NB6F20	PLL Block B Lock Indicator	PLL_B_LOCK_N	port_out_reg6_i(6)	OUTBUF LVTTL	V3_3L	4
V3	IO220PB6F20	PLL Block C Lock Indicator	PLL_C_LOCK_N	port_out_reg6_i(7)	OUTBUF LVTTL	V3_3L	4
T8	IO221NB6F20	PLL Block D Lock Indicator	PLL_D_LOCK_N	port_out_reg6_i(8)	OUTBUF LVTTL	V3_3L	4
T9	IO221PB6F20	PLL Block E Lock Indicator	PLL_E_LOCK_N	port_out_reg6_i(9)	OUTBUF LVTTL	V3_3L	4
U2	IO222NB6F20	PLL Block F Lock Indicator	PLL_F_LOCK_N	port_out_reg6_i(10)	OUTBUF LVTTL	V3_3L	4
V2	IO222PB6F20	PLL Block G Lock Indicator	PLL_G_LOCK_N	port_out_reg6_i(11)	OUTBUF LVTTL	V3_3L	4
T7	IO223NB6F20	PLL Block H Lock Indicator	PLL_H_LOCK_N	port_out_reg6_i(12)	OUTBUF LVTTL	V3_3	4

Note: (4) This signal drives an individual LED (a logic 0 turns on the LED).

Table B-15 lists the FPGA pin definitions for JTAG Signals.

Table B-15. JTAG Signals Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
G15	PRA	Silicon Explorer Probe A	AX_PRA_T	J16 pin 3
D16	PRB	Silicon Explorer Probe B	AX_PRB_T	J16 pin 1
AB16	PRC	Silicon Explorer Probe C	AX_PRC_T	J2 pin 1
AF16	PRD	Silicon Explorer Probe D	AX_PRD_T	J2 pin 2
G7	TCK	JTAG TCK	AX_TCK	J16 pin 13
D5	TDI	JTAG TDI	AX_TDI	J16 pin 15
J8	TDO	JTAG TDO	AX_TDO_T	J16 pin 11
F6	TMS	JTAG TMS	AX_TMS	J16 pin 9
C4	TRST	JTAG TRST	AX_TRST_N	J3 pin 1

Table B-16 lists FPGA pin definitions for Special Functions.

Table B-16. Special Functions Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	External Connector
E4	GND/LP144	Low Power Mode Select	GND/LP	J5 pin 2
G24	VPUMP	VPUMP Select	VPUMP	J6 pin

Table B-17 lists FPGA pin definitions for Spares..

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
B11	IO17 NB0 F1	Test Header P8 pin 1	P8_1	port_out_reg0_i(17), port_out_enable0_iv(0), port_in_reg0_i(15)	P8 pin 1	BIBUF LVTTL	V3_3L		5
B10	IO17 PB0 F1	Test Header P8 pin 2	P8_2	port_out_reg0_i(18), port_out_enable0_i(1), port_in_reg0_i(16)	P8 pin 2	BIBUF LVTTL	V3_3L		5

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
D11	IO18_NB0F1	Test Header P8 pin 3	P8_3	port_out_reg0_i(19), port_out_enable0_i(2), port_in_reg0_i(17)	P8 pin 3	BIBUF LVTTL	V3_3L		5
E11	IO18_PB0F1	Test Header P8 pin 4	P8_4	port_out_reg0_i(20), port_out_enable0_i(3), port_in_reg0_i(18)	P8 pin 4	BIBUF LVTTL	V3_3L		5
C12	IO19_NB0F1	Test Header P8 pin 5	P8_5	port_out_reg0_i(21), port_out_enable0_i(4), port_in_reg0_i(19)	P8 pin 5	BIBUF LVTTL	V3_3L		5
C11	IO19_PB0F1	Test Header P8 pin 6	P8_6	port_out_reg0_i(22), port_out_enable0_i(5), port_in_reg0_i(20)	P8 pin 6	BIBUF LVTTL	V3_3L		5

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
F12	IO20 NB0 F1	Test Header P8 pin 7	P8_7	port_out_reg0_i(23), port_out_enable0_i(6), port_in_reg0_i(21)	P8 pin 7	BIBUF LVTTL	V3_3L		5
G12	IO20 PB0 F1	Test Header P8 pin 8	P8_8	port_out_reg0_i(24), port_out_enable0_i(7), port_in_reg0_i(22)	P8 pin 8	BIBUF LVTTL	V3_3L		5
D12	IO21 NB0 F1	Test Header P8 pin 9	P8_9	port_out_reg0_i(25), port_out_enable0_i(8), port_in_reg0_i(23)	P8 pin 9	BIBUF LVTTL	V3_3L		5
E12	IO21 PB0 F1	Test Header P8 pin 10	P8_10	port_out_reg0_i(26), port_out_enable0_i(9), port_in_reg0_i(24)	P8 pin 10	BIBUF LVTTL	V3_3L		5

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
H13	IO22NB0F2	Test Header P8 pin 11	P8_11	port_out_reg0_i(27), port_out_enable0_i(10), port_in_reg0_i(25)	P8 pin 11	BIBUF LVTTL	V3_3L		5
J13	IO22PB0F2	Test Header P8 pin 12	P8_12	port_out_reg0_i(28), port_out_enable0_i(11), port_in_reg0_i(26)	P8 pin 12	BIBUF LVTTL	V3_3L		5
A12	IO23NB0F2	Test Header P8 pin 13	P8_13	port_out_reg0_i(29), port_out_enable0_i(12), port_in_reg0_i(27)	P8 pin 13	BIBUF LVTTL	V3_3L		5
A11	IO23PB0F2	Test Header P8 pin 14	P8_14	port_out_reg0_i(30), port_out_enable0_i(13), port_in_reg0_i(28)	P8 pin 14	BIBUF LVTTL	V3_3L		5

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
F13	IO24 NB0 F2	Test Header P8 pin 15	P8_15	port_out_reg0_i(31), port_out_enable0_i(14), port_in_reg0_i(29)	P8 pin 15	BIBUF LVTTL	V3_3L		5
G13	IO24 PB0 F2	Test Header P8 pin 16	P8_16	port_out_reg0_i(32), port_out_enable0_i(15), port_in_reg0_i(30)	P8 pin 16	BIBUF LVTTL	V3_3L		5
B13	IO25 NB0 F2	Test Header P8 pin 17	P8_17	port_out_reg0_i(33), port_out_enable0_i(16), port_in_reg0_i(31)	P8 pin 17	BIBUF LVTTL	V3_3L		5
B12	IO25 PB0 F2	Test Header P8 pin 18	P8_18	port_out_reg0_i(34), port_out_enable0_i(17), port_in_reg0_i(32)	P8 pin 18	BIBUF LVTTL	V3_3L		5

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
E14	IO26 NB0 F2	Test Header P8 pin 19	P8_19	port_out_reg0_i(35), port_out_enable0_i(18), port_in_reg0_i(33)	P8 pin 19	BIBUF LVTTL	V3_3L		5
E13	IO26 PB0 F2	Test Header P8 pin 20	P8_20	port_out_reg0_i(36), port_out_enable0_i(19), port_in_reg0_i(34)	P8 pin 20	BIBUF LVTTL	V3_3L		5
B14	IO27 NB0 F2	Spare Single-Ended Connection to VHDM Connector	SE_SPARE_0 (VHDM)	port_out_reg0_i(37), port_out_enable0_i(20), port_in_reg0_i(37)	J17 pin E3	BIBUF LVTTL	V3_3L		
A14	IO27 PB0 F2	Spare Single-Ended Connection to VHDM Connector	SE_SPARE_1 (VHDM)	port_out_reg0_i(38), port_out_enable0_i(20), port_in_reg0_i(38)	J17 pin E23	BIBUF LVTTL	V3_3L		

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
F20	IO44 NB1 F4	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ N7	port_in_ reg1_i(26)	J17 pin H19	INBUF_ LVDS	V2_5	LVDS input pair only	1
F19	IO44 PB1 F4	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ P7	port_in_ reg1_i(26)	J17 pin G19	INBUF_ LVDS	V2_5	LVDS input pair only	
C20	IO40 NB1 F3	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ N8	port_in_ reg1_i(23)	J17 pin H20	INBUF_ LVDS	V2_5	LVDS input pair only	1

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
C19	IO40 PB1 F3	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ P8	port_in_ reg1_i(23)	J17 pin G20	INBUF_ LVDS	V2_5		
E20	IO41 NB1 F4	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ N9	port_in_ reg1_i(24)	J17 pin H21	INBUF_ LVDS	V2_5	LVDS input pair only	1
E19	IO41 PB1 F4	Spare LVDS Terminated Connection from VHDM Connector	FPGA_ LVDS_ SPARE_ P9	port_in_ reg1_i(24)	J17 pin G21	INBUF_ LVDS	V2_5	LVDS input pair only	

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
F18	IO42 NB1 F4	Spare LVDS Termi-nated Connec-tion from VHDM Connector	FPGA_ LVDS_ SPARE_ N10	port_in_ reg1_i(25)	J17 pin H22	INBUF_ LVDS	V2_5	LVDS input pair only	1
G1 8	IO42 PB1 F4	Spare LVDS Termi-nated Connec-tion from VHDM Connector	FPGA_ LVDS_ SPARE_ P10	port_in_ reg1_i(25)	J17 pin G22	INBUF_ LVDS	V2_5		
H2 3	IO63 NB1 F5	Spare LVDS Termi-nated Connec-tion from VHDM Connector	FPGA_LV DS_SPAR E_N11	port_in_ reg1_i(29)	J17 pin H23	INBUF_ LVDS	V2_5	LVDS input pair only	1

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
H22	IO63PB1F5	Spare LVDS Terminated Connection from VHDM Connector	FPGA_LVDS_SPARE_P11	port_in_reg1_i(29)	J17 pin G23	INBUF_LVDS	V2_5		
G23	IO60NB1F5	Spare LVDS Terminated Connection from VHDM Connector	FPGA_LVDS_SPARE_N12	port_in_reg1_i(28)	J17 pin H24	INBUF_LVDS	V2_5	LVDS input pair only	1
G22	IO60PB1F5	Spare LVDS Terminated Connection from VHDM Connector	FPGA_LVDS_SPARE_P12	port_in_reg1_i(28)	J17 pin G24	INBUF_LVDS	V2_5		

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
H21	IO56NB1F5	Spare LVDS Terminated Connection from VHDM Connector	FPGA_LVDS_SPARE_N13	port_in_reg1_i(27)	J17 pin H25	INBUF_LVDS	V2_5	LVDS input pair only	1
G21	IO56PB1F5	Spare LVDS Terminated Connection from VHDM Connector	FPGA_LVDS_SPARE_P13	port_in_reg1_i(27)	J17 pin G25	INBUF_LVDS	V2_5		
R24	IO92NB2F8	Spare LVDS Terminated Connection to VHDM Connector	FPGA_LVDS_SPARE_N0_T	port_out_reg2_i(30)	J17 pin B19	OUTBUF_LVDS	V2_5	LVDS output pair only	2

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
R25	IO92 PB2 F8	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ P0_T	port_out_ reg2_i(30)	J17 pin A19	OUTBUF _LVDS	V2_5		
P25	IO88 NB2 F8	Spare LVDS Terminated Connection to VHDM Connector	FPGA_LV DS_SPAR E_N1_T	port_out_ reg2_i(29)	J17 pin B20	OUTBUF _LVDS	V2_5	LVDS output pair only	2
P24	IO88 PB2 F8	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ S PARE_ P1_T	port_out_ reg2_i(29)	J17 pin A20	OUTBUF _LVDS	V2_5		

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
N25	IO83_NB2_F7	Spare LVDS Terminated Connection to VHDM Connector	FPGA_LVDS_SPARE_N2_T	port_out_reg2_i(28)	J17 pin B21	OUTBUF_LVDS	V2_5	LVDS output pair only	2
N24	IO83_PB2_F7	Spare LVDS Terminated Connection to VHDM Connector	FPGA_LVDS_SPARE_P2_T	port_out_reg2_i(28)	J17 pin A21	OUTBUF_LVDS	V2_5		
M25	IO76_NB2_F7	Spare LVDS Terminated Connection to VHDM Connector	FPGA_LVDS_SPARE_N3_T	port_out_reg2_i(27)	J17 pin B22	OUTBUF_LVDS	V2_5	LVDS output pair only	2
L25	IO76_PB2_F7		FPGA_LVDS_SPARE_P3_T	port_out_reg2_i(27)	J17 pin A22	OUTBUF_LVDS	V2_5		

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
L26	IO75 NB2 F7	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ N4_T	port_out_ reg2_i(26)	J17 pin B23	OUTBUF _LVDS	V2_5	LVDS output pair only	2
K26	IO75 PB2 F7	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ P4_T	port_out_ reg2_i(26)	J17 pin A23	OUTBUF _LVDS	V2_5		
K23	IO64 NB2 F6	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ N5_T	port_out_ reg2_i(24)	J17 pin B24	OUTBUF _LVDS	V2_5	LVDS output pair only	2

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
J23	IO64 PB2 F6	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ P5_T	port_out_ reg2_i(24)	J17 pin A24	OUTBUF _LVDS	V2_5		
J24	IO65 NB2 F6	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ N6_T	port_out_ reg2_i(25)	J17 pin B25	OUTBUF _LVDS	V2_5	LVDS output pair only	2
H24	IO65 PB2 F6	Spare LVDS Terminated Connection to VHDM Connector	FPGA_ LVDS_ SPARE_ P6_T	port_out_ reg2_i(25)	J17 pin A25	OUTBUF _LVDS	V2_5		
U25	IO10 6PB 3F9	Spare Terminated HSTL Signal	SPARE_ HSTL1	port_in_ reg3_i(6)	RN1 pin 4	INBUF_ HSTL_I	V1_5	HSTL input only	

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
AC 26	IO12 2NB 3F11	Spare Terminated HSTL Signal	SPARE_HSTL2	port_in_reg3_i(7)	RN1 pin 1	INBUF_HSTL_I	V1_5	HSTL input only	
AB 26	IO12 2PB 3F11	Spare Terminated HSTL Signal	SPARE_HSTL3	port_out_reg3_i(30)	RN1 pin 3	OUTBUF_HSTL_I	V1_5	HSTL output only	
AF 28	IO12 3PB 3F11	Spare Terminated HSTL Signal	SPARE_HSTL4	port_out_reg3_i(31)	RN1 pin 2	OUTBUF_HSTL_I	V1_5	HSTL output only	
R6	IO22 5PB 7F21	Test Header P5 pin 1	P5_1	port_out_reg7_i(1)	P5 pin 1	OUTBUF_LVCMOS25	Selectable		6, 7
R4	IO22 6NB 7F21	Test Header P9 pin 19	P9_19	port_out_reg7_i(2)	P9 pin 19	OUTBUF_GTLP25	Selectable		6, 7
R5	IO22 6PB 7F21	Test Header P9 pin 20	P9_20	port_out_reg7_i(3)	P9 pin 20	OUTBUF_GTLP25	Selectable		6, 7
P1	IO22 8NB 7F21	Test Header P5 pin 4	B7_IN_0	port_in_reg7_i(0)	P5 pin 4	INBUF_GTLP25	Selectable		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
R1	IO228PB7F21	Test Header P5 pin 5	B7_IN_1	port_in_reg7_i(1)	P5 pin 5	INBUF_GTLP25	Selectable		6, 7
P9	IO229NB7F21	Test Header P5 pin 2	P5_2	port_in_reg7_i(2)	P5 pin 2	INBUF_GTLP25	Selectable		6, 7
P8	IO229PB7F21	Test Header P5 pin 3	P5_3	port_in_reg7_i(3)	P5 pin 3	INBUF_GTLP25	Selectable		6, 7
P2	IO230PB7F21	Test Header P5 pin 7	B7_IN_3	port_in_reg7_i(5)	P5 pin 7	INBUF_GTLP25	Selectable		6, 7
P7	IO231NB7F21	Test Header P9 pin 1	P9_1	port_out_reg7_i(4)	P9 pin 1	OUTBU_GTLP25	Selectable		6, 7
P6	IO231PB7F21	Test Header P9 pin 2	P9_2	port_out_reg7_i(5)	P9 pin 2	OUTBUF_GTLP25	Selectable		6, 7
N3	IO232NB7F21	Test Header P9 pin 3	P9_3	port_out_reg7_i(6)	P9 pin 3	OUTBUF_GTLP25	Selectable		6, 7
P3	IO232PB7F21	Test Header P9 pin 4	P9_4	port_out_reg7_i(7)	P9 pin 4	OUTBUF_GTLP25	Selectable		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
P4	IO23 3NB 7F21	Test Header P9 pin 5	P9_5	port_out_ reg7_i(8)	P9 pin 5	OUTBUF _GTLP25	Select-able		6, 7
P5	IO23 3PB 7F21	Test Header P9 pin 6	P9_6	port_out_ reg7_i(9)	P9 pin 6	OUTBUF _GTLP25	Select-able		6, 7
L1	IO23 4NB 7F21	Test Header P9 pin 7	P9_7	port_out_ reg7_i(10)	P9 pin 7	OUTBUF _GTLP25	Select-able		6, 7
M1	IO23 4PB 7F21	Test Header P9 pin 8	P9_8	port_out_ reg7_i(11)	P9 pin 8	OUTBUF _GTLP25	Select-able		6, 7
M4	IO23 5NB 7F21	Test Header P5 pin 6	B7_IN_2	port_in_ reg7_i(4)	P5 pin 6	INBUF_G TLP25	Select-able		6, 7
N4	IO23 5PB 7F21	Test Header P9 pin 9	P9_9	port_out_ reg7_i(12)	P9 pin 9	OUTBUF _GTLP25	Select-able		6, 7
N8	IO23 7NB 7F22	Test Header P9 pin 10	P9_10	port_out_ reg7_i(13)	P9 pin 10	OUTBUF _GTLP25	Select-able		6, 7
M5	IO23 8NB 7F22	Test Header P9 pin 11	P9_11	port_out_ reg7_i(14)	P9 pin 11	OUTBUF _GTLP25	Select-able		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
N5	IO23 8PB 7F22	Test Header P9 pin 12	P9_12	port_in_ reg7_i(6)	P9 pin 12	INBUF_ GTLP25	Select-able		6, 7
L2	IO23 9NB 7F22	Test Header P9 pin 13	P9_13	port_out_ reg7_i(15)	P9 pin 13	OUTBUF _GTLP25	Select-able		6, 7
M2	IO23 9PB 7F22	Test Header P9 pin 14	P9_14	port_out_ reg7_i(16)	P9 pin 14	OUTBUF _GTLP25	Select-able		6, 7
L3	IO24 0NB 7F22	Test Header P9 pin 15	P9_15	port_out_ reg7_i(17)	P9 pin 15	OUTBUF _GTLP25	Select-able		6, 7
M3	IO24 0PB 7F22	Test Header P9 pin 16	P9_16	port_out_ reg7_i(18)	P9 pin 16	OUTBUF _GTLP25	Select-able		6, 7
M8	IO24 1NB 7F22	Test Header P9 pin 17	P9_17	port_out_ reg7_i(19)	P9 pin 17	OUTBUF _GTLP25	Select-able		6, 7
M7	IO24 1PB 7F22	Test Header P9 pin 18	P9_18	port_out_ reg7_i(20)	P9 pin 18	OUTBUF _GTLP25	Select-able		6, 7
L6	IO24 3NB 7F22	Test Header P10 pin 1	P10_1	port_out_ reg7_i(23)	P10 pin 1	OUTBUF _GTLP25	Select-able		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
M6	IO24 3PB 7F22	Test Header P10 pin 2	P10_2	port_out_ reg7_i(24)	P10 pin 2	OUTBUF _GTLP25	Select-able		6, 7
K5	IO24 4NB 7F22	Test Header P10 pin 3	P10_3	port_out_ reg7_i(25)	P10 pin 3	OUTBUF _GTLP25	Select-able		6, 7
L5	IO24 4PB 7F22	Test Header P10 pin 4	P10_4	port_out_ reg7_i(26)	P10 pin 4	OUTBUF _GTLP25	Select-able		6, 7
G2	IO24 6NB 7F22	Test Header P10 pin 5	P10_5	port_out_ reg7_i(27)	P10 pin 5	OUTBUF _GTLP25	Select-able		6, 7
H2	IO24 6PB 7F22	Test Header P5 pin 8	B7_IN_4	port_in_ reg7_i(7)	P5 pin 8	INBUF_ GTLP25	Select-able		6, 7
L8	IO24 7NB 7F23	Test Header P10 pin 6	P10_6	port_out_ reg7_i(28)	P10 pin 6	OUTBUF _GTLP25	Select-able		6, 7
L7	IO24 7PB 7F23	Test Header P10 pin 7	P10_7	port_out_ reg7_i(29)	P10 pin 7	OUTBUF _GTLP25	Select-able		6, 7
G3	IO24 8NB 7F23	Test Header P10 pin 8	P10_8	port_out_ reg7_i(30)	P10 pin 8	OUTBUF _GTLP25	Select-able		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
H3	IO24 8PB 7F23	Test Header P10 pin 9	P10_9	port_out_ reg7_i(31)	P10 pin 9	OUTBUF _GTLP25	Select-able		6, 7
G4	IO24 9NB 7F23	Test Header P10 pin 10	P10_10	port_out_ reg7_i(32)	P10 pin 10	OUTBUF _GTLP25	Select-able		6, 7
H4	IO24 9PB 7F23	Test Header P10 pin 11	P10_11	port_out_ reg7_i(33)	P10 pin 11	OUTBUF _GTLP25	Select-able		6, 7
J6	IO25 0NB 7F23	Test Header P10 pin 12	P10_12	port_out_ reg7_i(34)	P10 pin 12	OUTBUF _GTLP25	Select-able		6, 7
K6	IO25 0PB 7F23	Test Header P10 pin 13	P10_13	port_out_ reg7_i(35)	P10 pin 13	OUTBUF _GTLP25	Select-able		6, 7
H5	IO25 1NB 7F23	Test Header P10 pin 14	P10_14	port_out_ reg7_i(36)	P10 pin 14	OUTBUF _GTLP25	Select-able		6, 7
J5	IO25 1PB 7F23	Test Header P10 pin 15	P10_15	port_out_ reg7_i(37)	P10 pin 15	OUTBUF _GTLP25	Select-able		6, 7
F2	IO25 2NB 7F23	Test Header P10 pin 16	P10_16	port_in_ reg7_i(8)	P10 pin 16	INBUF_ GTLP25	Select-able		6, 7

Table B-17. Spares Pin Definitions

FPGA Pin No.	FPGA Pin Name	Signal Description	Schematic Net Name	FPGA I/O Ring Net Name	External Connector	FPGA Buffer Type	Power Domain	Required Default Logic Level	Note
F1	IO25 2PB 7F23	Test Header P10 pin 17	P10_17	port_out_ reg7_i(38)	P10 pin 17	OUTBUF _GTLP25	Select-able		6, 7
K8	IO25 3NB 7F23	Test Header P5 pin 9	B7_IN_5	port_in_ reg7_i(9)	P5 pin 9	INBUF_ GTLP25	Select-able		6, 7
K7	IO25 3PB 7F23	Test Header P5 pin 10	B7_IN_6	port_in_ reg7_i(10)	P5 pin 10	INBUF_ GTLP25	Select-able		6, 7
G6	IO25 5NB 7F23	Test Header P10 pin 18	P10_18	port_out_ reg7_i(39)	P10 pin 18	OUTBUF _GTLP25	Select-able		6, 7
H6	IO25 5PB 7F23	Test Header P10 pin 19	P10_19	port_out_ reg7_i(40)	P10 pin 19	OUTBUF _GTLP25	Select-able		6, 7
F5	IO25 6NB 7F23	Test Header P10 pin 20	P10_20	port_out_ reg7_i(41)	P10 pin 20	OUTBUF _GTLP25	Select-able		6, 7

The Required Default Logic Level column defines the default state that the specified pin must remain at in a user-specific implementation (i.e., a demo system that has been populated with an FPGA other than the FPGA originally shipped with the demo system). This logic level is required so that specific inputs on the demo board are not left floating, and thus avoiding potential damage to the demo system.

Note:

(1) This signal has been setup with on-board termination for an input LVDS signal. This signal will have indeterminate behavior if it is used as anything other than an LVDS input

(2) This signal has been setup with on-board termination for an output LVDS signal. This signal will have indeterminate behavior if it is used as anything other than an LVDS output

(3) This signal must be used as an input only, unless the PowerQUICC II Processor Module is not attached to the Axcelerator Motherboard

(4) This signal drives an individual LED (a logic 0 turns on the LED)

(5) This is an unused spare signal that is connected to a header and may be used as needed. Note that P8 is not populated in the standard configuration. P8 can be populated with Mil-Max part number 850-10-020-30-001000 or Digi-Key part number ED1050-ND (snap-to-fit)

(6) This is an unused spare signal that is connected to a header and may be used as needed. Note that P5, P9 and P10 are not populated in the standard configuration. P9 and P10 can be populated with Mil-Max part number 850-10-020-30-001000 and P5 can be populated with Mil-Max part number 850-10-010-30-001000, or Digi-Key part number ED1050-ND (snap-to-fit) can be used.

(7) This is a configurable I/O bank. It can be configured to any I/O standard using configuration jumpers on the demo board. However, if this bank is configured for a voltage standard that exceeds 2.5 volts, then U5 and U15 must be removed from the board in order to avoid damaging the devices.

C

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

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Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Website

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

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Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

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You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

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