I/O Features in Axcelerator Family Devices

Introduction and Feature Summary

The Axcelerator family offers I/O features to support a very wide variety of user designs. An outline of the features is as follows:

- Support for multiple I/O specs
- Mixed-voltage operation – 1.5V, 1.8V, 2.5V, 3.3V
- Bank-Selectable I/Os – 8 Banks per Chip
- Registered I/O with 64-bit PerPin FIFO on Each Pin
- DDR Operation
- Hot-Swap Compliant I/Os
- Programmable Slew Rate, Output Drive, and Input Delay
- Integrated Pull-Up and Pull-Down Circuits
- Boundary-Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)

A separate Axcelerator I/O Selection Guide gives an overview of the supported standards and features as well as performance information. This document provides details on configuration of the various basic I/O options.

Selecting Axcelerator I/Os

The following three steps in configuring Axcelerator I/O structures are summarized below:

- Select the Default I/O Standard in Designer's Device Selection Wizard (Figure 1)
- Use ACTgen to configure I/Os by generating specific library macros
- Use Designer's PinEdit to change characteristics of individual I/Os.

The options available in the latter two choices are described in greater detail below.

Using ACTgen for I/O Configuration

The ACTgen tool in Actel's Designer tool suite provides a GUI-based method of configuring the I/O. The first step is configuring ACTgen is as follows:

- Invoke ACTgen (Figure 1)
- Select File -> New to select the Axcelerator Family as shown in Figure 2 on page 2. Click OK.
- Click on the I/O Icon under the Macro window (Figure 3 on page 2).
- At this point the user has six configuration options (Figure 4 on page 3). Again, this document provides information on the basic options — input, output, bidirectional, and tristate buffers. See the separate sections below for details. If further information on PerPin FIFO and DDR configuration is needed, please refer to the *Using the Axcelerator PerPin FIFOs* application note.

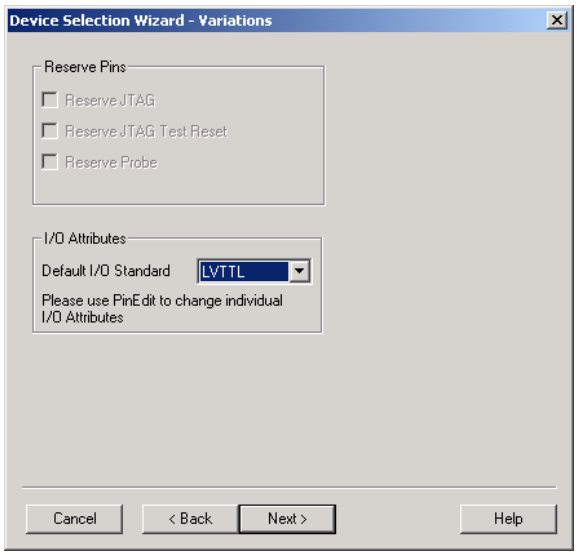

Figure 1 • *Default I/O Standard Selection in Designer*

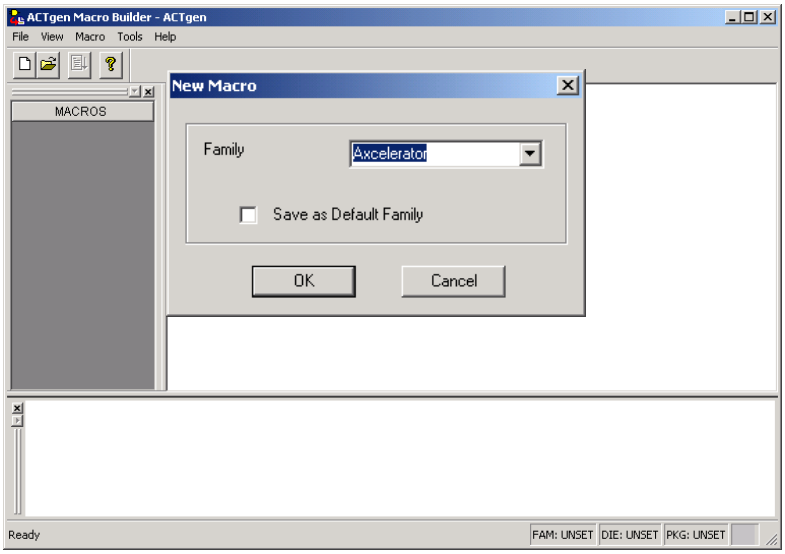

Figure 2 • *Invoking ACTgen and Choosing the AX Family*

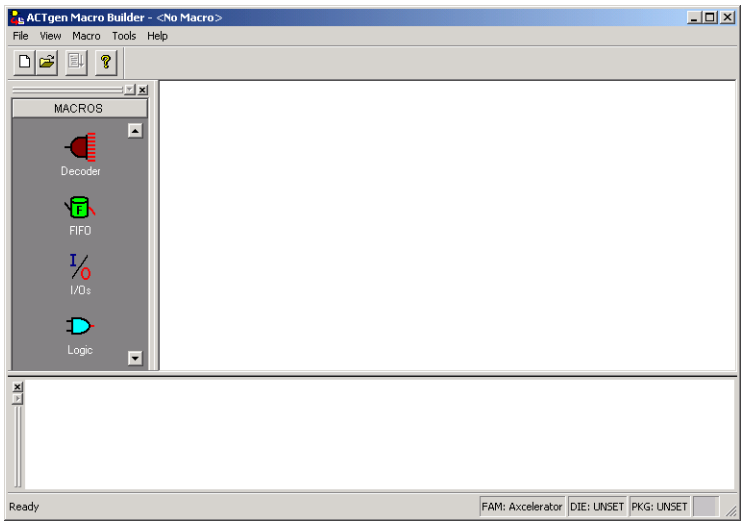

Figure 3 • *Selecting the I/O Macro*

Input Buffers

The Input Buffer is configured using the following options:

- Select the Input Buffers tab (see Figure 4 on page 3).
- Choose one of the Variations (see below)
- Choose Width – 1 (default) to 99
- Select Generate. You will be prompted for a file name, and the file format can be selected as EDIF, VHDL, VERILOG, ADL, or WV.

Note that the Variation illustrated is Regular. Other options include:

- Special – Type choices are LVCMOS25 (2.5v LVCMOS) (default), LVCMOS18 (1.8v LVCMOS), LVCMOS15 (1.5v LVCMOS), PCI, PCIX, GTLP25 (GTL+ 2.5v), GTLP33 (GTL+ 3.3v), HSTL_I, HSTL_II, SSTL3_I, SSTL3_II, SSTL2_I, SSTL2_II
- Pull Up – Includes a weak pull-up resistor. Type choices are LVCMOS25 (default), LVCMOS18, LVCMOS15
- Pull Down – Includes a weak pull-down resistor. Type choices are LVCMOS25 (default), LVCMOS18, LVCMOS15

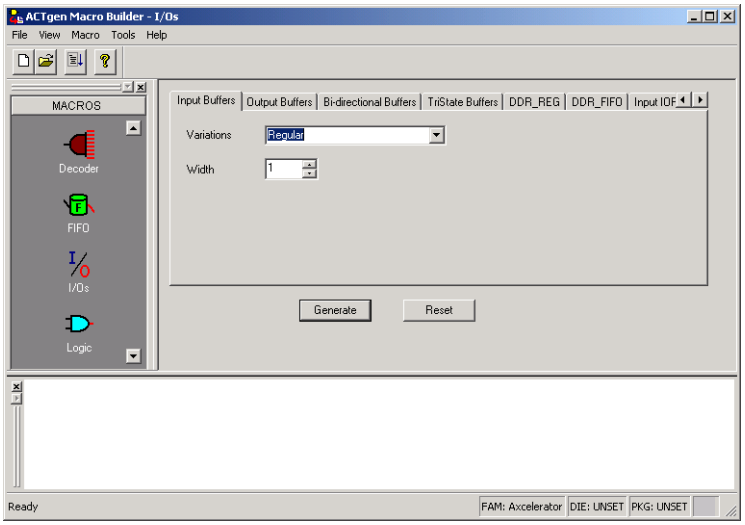

Figure 4 • I/O Options

Output Buffers

Configuring the Output Buffer is very similar to the Input Buffer:

- Select the Output Buffers tab (Figure 5)
- Choose one of the Variations – Regular or Special
- Choose Width – 1 (default) to 99
- If the Special Variation is selected …
- … Select Output Drive – 8mA, 12mA, 16mA, 24 mA (default)
- … Select Slew Rate – Low or High (default)
- Select Generate. You will be prompted for a file name, and the file format can be selected as EDIF, VHDL, VERILOG, ADL, or WV.

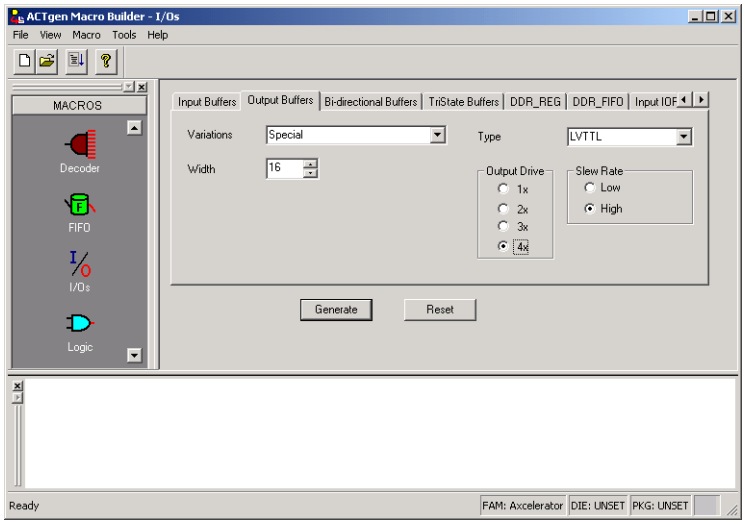

Figure 5 • Output Buffer Selection

Output Buffers and Tristate Buffers

The Bidirectional and Tristate Buffers have identical configuration options. The method is as follows:

Select the Bidirectional Buffers or TriState Buffers tab (Figure 6 on page 4).

- Choose one of the Variations (see below)
- Choose Width – 1 (default) to 99

- Select Enable Polarity – Active Low (default) or Active High
- If the Special, Pull Up, or Pull Down Variation is selected …
- … Select Output Drive – 8mA, 2mA, 16mA, 24 mA – default
- … Select Slew Rate - Low or High (default)
- Select Generate. You will be prompted for a file name, and the file format can be selected as EDIF, VHDL, VERILOG, ADL, or WV.

The Variations options include:

- **Regular**
- **Special, Pull-Up, or Pull-Down** – Type choices are LVTTL (default), LVCMOS25, LVCMOS18, LVCMOS15, PCI, PCI-X, GTLP25, GTLP33

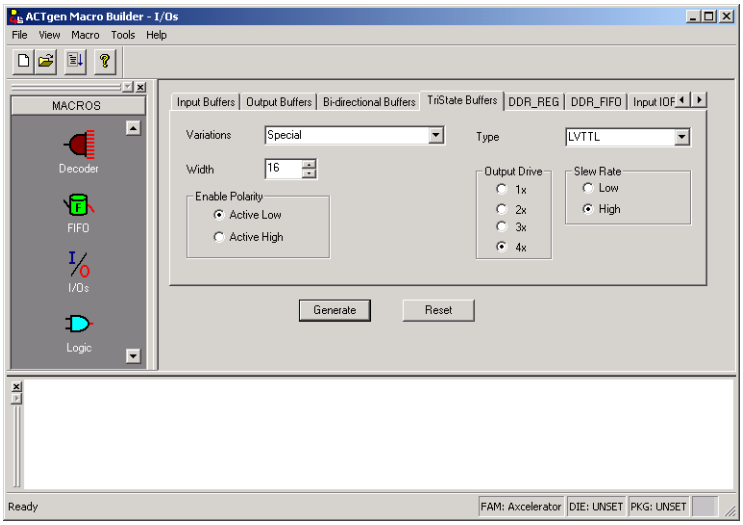

Figure 6 • *Tristate Buffer Selection*

Using PinEdit for I/O Configuration

Although selection of I/O characteristics for a bus is done most easily with ACTgen, many of the I/O options can also be selected in GUI-based fashion in PinEdit. PinEdit is invoked from Designer as shown in Figure 7 on page 5. The PinEdit window is shown in Figure 8 on page 5. The I/O configuration options are given below:

- I/O Standard
- Output Drive (mA)
- Slew
- Resistor Pull
- Input Delay
- Output Load
- Use Register
- Hot Swappable

Note that the last four options can ONLY be selected in PinEdit. The choices for each option are given in the following subsections.

I/O Standard

Here the choices depend on compatibility of I/O standards within a given bank. If ACTgen has generated macros associated with several pins in a bank, then the pins need to be of compatible types. Note that only single-ended standards are acceptable here. In addition, ACTgen's choices for compatibility are only those which are independent of V_{REF} (Table 1 on page 6). Choices dependent upon V_{REF} are omitted.

Output Drive mA

Here the choices correspond to selections in ACTgen although the nomenclature is different. The choice list is as follows:

- 8mA (x1 in ACTgen)
- 12 mA (x2)
- 16 mA (x3)
- 24 mA (x4)

Slew

Choices are High and Low, as in ACTgen.

Resistor Pull

This option allows inclusion of a weak resistor for either pull-up or pull-down of the input buffer. The choices are None, Up (Pull Up) or Down (Pull Down). Again, these choices are all available in ACTgen.

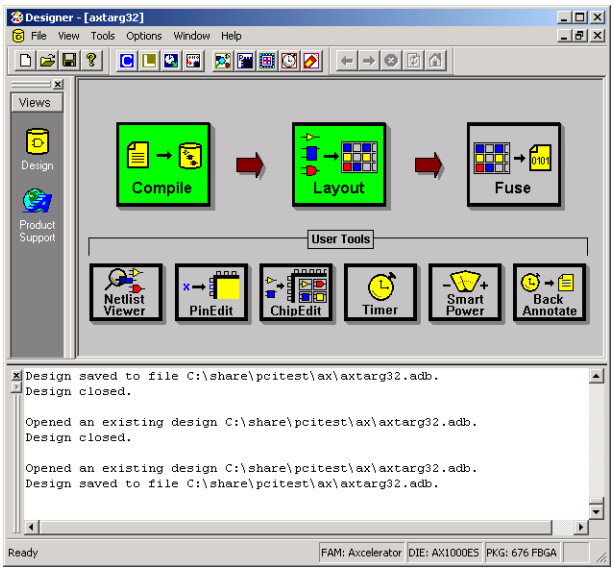

Figure 7 • *Invoking PinEdit*

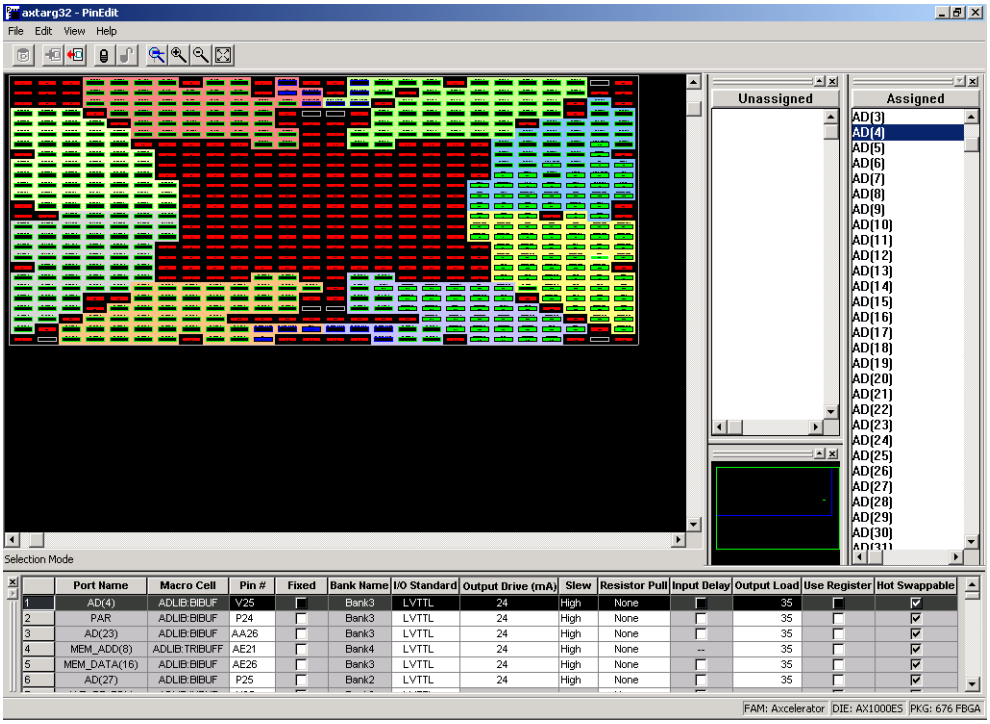

Figure 8 • *I/O Option Selection in Designer's PinEdit*

Table 1 • Single-Ended I/O Compatibility Matrix

	LVTTL 3.3v	LVCMOS 2.5v	LVCMOS 1.8v	LVMCOS 1.5v	3.3v PCI/PCI-X	GTL+ 3.3v	GTL+ 2.5v	HSTL I	SSTL2 I and II	SSTL3 I and II
I & II	X									
I & II										
LVTTL 3.3v	X				X					
LVCMOS 2.5v		X								
LVCMOS 1.8v			X							
LVCMOS 1.5v				X				X		
3.3v PCI/PCI-X	X				X					
GTL+ 3.3v	X				X	X				
GTL+ 2.5v		X					X			
HSTL I				X				X		
SSTL2 I and II		X							X	
SSTL3 I and II	X				X					X

Input Delay

A programmable input delay element is associated with each I/O bank. The delay is programmable in steps from approximately 0.54ns to 3.41ns. The delay can be switched in and out for each input buffer in PinEdit by checking the associated box. If the input register is selected (see next section), the delay element is activated (i.e., the box is checked) by default. The user can override this default setting. Input delay selection is not included in ACTgen.

Use Register

The input and output registers for each individual I/O can be activated by checking the box associated with an I/O. The I/O registers are NOT selected by default.

Output Load

The user can enter a capacitive load as an integral number of picofarads. 35pF is the default. This option is not available in ACTgen.

Hot Swappable

This box indicates whether or not the I/O is hot swappable. If checked (all standards except PCI and PCI-X) a clamp diode is NOT included to allow proper hot-swap behavior. If not checked (PCI and PCI-X only), the clamp diode is included as required by those specifications, but the I/O is NOT hot swappable.

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