CoreU1LL – UTOPIA Level 1 Link-Layer Interface

DirectCore

Product Summary

Intended Use

- Standard UTOPIA Level 1 Interface to any ATM PHY-Layer Device

Key Features

- Standard 8-bit, 25 MHz UTOPIA Level 1 Link-Layer (Master) Interface Complies with the ATM Forum UTOPIA Specification, Level 1 Version 2.01 (af-phy-0017.000)
- Separate Tx and Rx Clocks and Interface Pins
- Supports Cell-Level Handshake for 53 or 54-byte ATM Cells with Automatic Add/Drop of the UDF2 Field in the ATM Header in 53-byte Mode
- 16-bit (54-byte) User Interfaces can be Used Directly or Bolt-Up to One of Actel's ATM Cell Buffer Blocks: ATMBUFx

Supported Families

- ProASIC^{PLUS} Family
- Axcelerator Family

Core Deliverables

- Netlist Version
  - Compiled RTL Simulation Model Fully Supported in Actel's Libero™ Integrated Design Environment (IDE)
  - Structural VHDL and Verilog Netlists (with and without I/O Pads) Compatible with Actel's Libero IDE and Industry Standard Synthesis and Simulation Tools
- RTL Version
  - VHDL Source Code
  - Core Synthesis and Simulation Scripts
- Actel-Developed Testbench (VHDL) Fully Supported by Industry Standard Simulation Tools

Design Tools Support

- Simulation: VITAL-Compliant VHDL and OVI-Compliant Verilog Simulators
- Synthesis: Leonardo Spectrum, Synplify, Design Compiler, FPGA Compiler, and FPGA Express

General Description

CoreU1LL is a UTOPIA Level 1 Link-Layer (Master) interface core that connects directly to any ATM PHY-Layer (slave) device and user logic (or optional ATM cell buffer blocks) to provide an interface between the PHY-Layer device and a non-standard Link-Layer device or user logic (Figure 1).

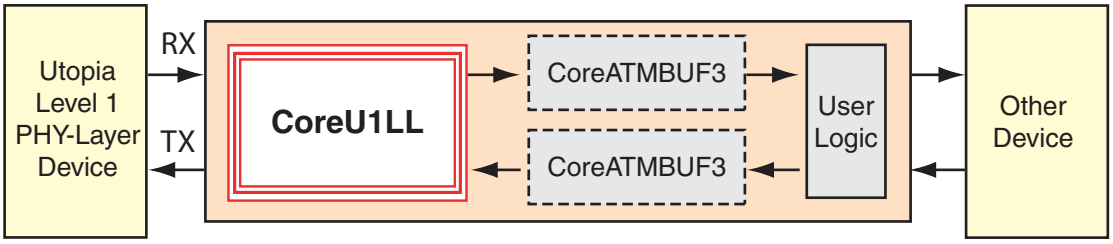

Figure 1 • Block Diagram

Device Requirements

CoreU1LL can be implemented in either ProASIC^{PLUS} or Axcelerator device families. Table 1 indicates the number of core logic cells required in each technology.

Table 1 • Device Utilization and Performance

Family	Cells or Tiles		Total Utilization		Performance
	Sequential	Combinatorial	Device	Percentage	
ProASIC^{PLUS}	51	79	APA075	4.2%	>25 MHz
Axcelerator	53	64	AX125	6.0%	>25 MHz

UTOPIA Interface

CoreU1LL implements a standard 8-bit point-to-point PHY-Layer interface that supports cell lengths of either 53 or 54 bytes. If the cell_size bit is low, a 53 byte cell is transferred and the UDF2 byte is inserted on ingress to and dropped on egress from the user interface; otherwise, 54 bytes are transferred. The UTOPIA interface signals are summarized in Table 2.

Table 2 • UTOPIA Interface Signals

Signal	Type	Description
U1_tx_clk	in	Tx interface clock
U1_tx_clav	in	Active high cell buffer space available
U1_tx_en	out	Active low data transfer enable
U1_tx_soc	out	Active high start-of-cell indication
U1_tx_data	out	8-bit egress data
U1_rx_clk	in	Rx interface clock
U1_rx_clav	in	Active high cell buffer space available
U1_rx_en	out	Active low data transfer enable
U1_rx_soc	in	Active high start-of-cell indication
U1_rx_data	in	8-bit ingress data

Tx Interface (Egress)

The process of transferring a cell on the UTOPIA level 1 Tx interface begins with r_avail. User logic asserts r_avail high whenever it has a cell available to send. The CoreU1LL waits until the PHY-Layer device indicates that it is ready to receive a cell by asserting u1-tx_clav high.

To begin sending cells on the Tx interface, the CoreU1LL asserts u1_tx_en low (Figure 2). CoreU1LL simultaneously asserts u1_tx_soc and u1_tx_data (Figure 2). The core sends 53 bytes (or 54 bytes) and does not monitor u1_tx_clav during cell transfers.

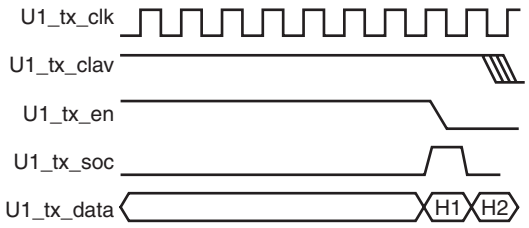

Figure 2 • Tx Start of Cell

If the user interface indicates that there are no more cells to send, or if polling during the current cell transfer indicates that the PHY-Layer device is not ready to accept another cell, the CoreU1LL deselects the physical interface by deasserting u1_tx_en after the last word of the transfer (Figure 3).

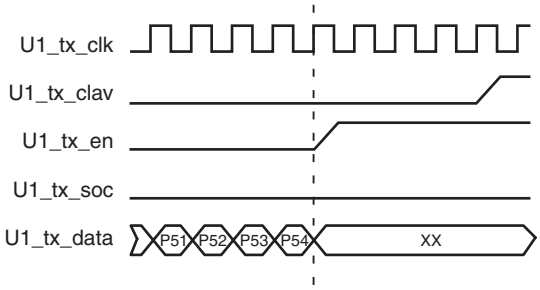

Figure 3 • Tx Transfer Complete

If the user interface has another cell to send to the PHY-Layer device, and if polling during the current cell indicates that the PHY-Layer device can accept another cell, the CoreU1LL PHY-Layer device sends cells back-to-back (Figure 4 on page 3).

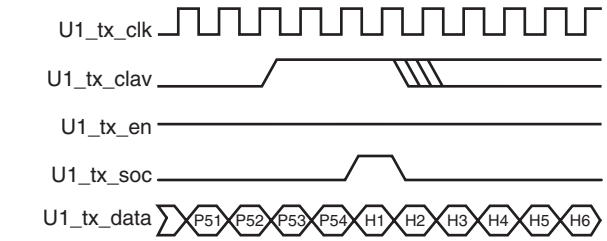

Figure 4 • *Tx Back-to-Back Transfer*

Rx Interface (Ingress)

The Rx interface operates in a similar manner to the Tx interface. The PHY-Layer device indicates that it has a cell ready to transfer by asserting ul_rx_clav high. Then, the user interface is ready to accept a cell (w_avail high). The CoreU1LL will initiate a transfer on the Rx interface by asserting u1_rx_en low (Figure 5).

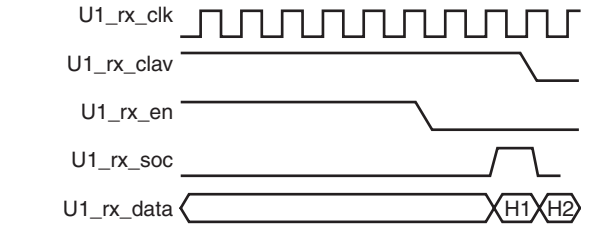

Figure 5 • *Rx Start of Cell Transfer*

The PHY-Layer device then asserts u1_rx_soc high, indicating that the first word of the cell transfer is active on the bus. Once a transfer has begun, all 53 or 54 bytes of the cell are transferred without interruption.

If polling during the current transfer indicates that there are no more cells available, or if the CoreU1LL is unable to accept another cell from the PHY-Layer device, the CoreU1LL deselects the physical interface by deasserting u1_rx_en after receiving the last byte of the current cell, as illustrated in Figure 6.

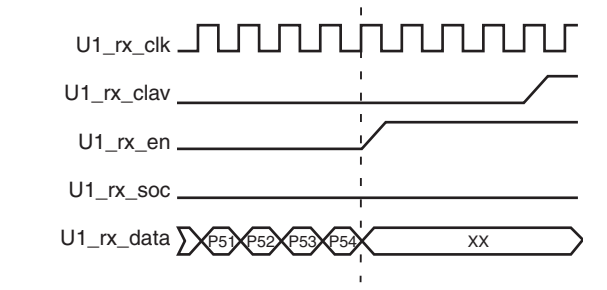

Figure 6 • *Rx End of Transfer*

If the user interface continues to assert w_avail during the last two bytes of the current cell transfer, and one or more complete ATM cells are ready to be transferred (u1_rx_clav is high), the CoreU1LL accepts back-to-back cells, as shown in Figure 7.

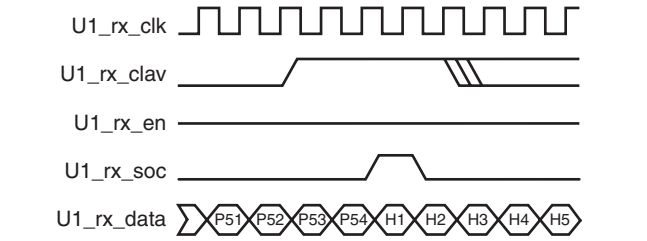

Figure 7 • *Rx Back-to-Back Transfer*

User Interface

The user interface can connect directly to Actel's CoreATMBUF3 cell buffer, an intellectual property core that provides buffering for up to three, 54-byte ATM cells in each direction (Figure 1 on page 1). Alternatively, the designer may connect his/her own cell buffer or user logic function directly to the user interface. The signals associated with the user interface are summarized in Table 3.

Table 3 • *User Interface Signals*

Signal	Type	Description
reset	in	Active high – resets all registers
xlate	in	53 / 54-byte cell size control
w_avail	in	Active high – user ready to receive
w_phy_act	out	Active high physical selected
w_enable	out	Active high data enable
w_adr	out	5-bit word count
w_data	out	16-bit data bus
r_avail	in	Active high – user ready to send
r_buf_en	out	Active high read enable
r_adr	out	5-bit word count
r_data	in	16-bit data bus

When reset is asserted high, all registers in the CoreU1LL are cleared. They will remain in this state as long as reset is asserted.

If the xlate input is low, the CoreU1LL transfers data to/from the PHY-Layer device as 53-byte ATM cells. On ingress (Rx), the CoreU1LL will duplicate the fifth byte of the ATM header and insert it as the sixth byte (UDF2) in order to create a standard 54-byte ATM cell on the user 'write' interface. Conversely, the CoreU1LL accepts a standard 54-byte cell at the user 'read' interface and drops the sixth byte during the transfer to the egress (Tx) interface. If xlate is high, no translation is performed; 54-byte cells are transferred on all interfaces.

The user interface is divided into write (Rx) and read (Tx) interfaces. The control signals and data for the write interface are associated with the u1_rx_clk, while control signals and data for the read interface are associated with the u1_tx_clk.

Each interface is controlled from the user logic by the w_avail and r_avail signals, respectively.

When the cell buffer or user logic is ready to receive or send a cell on either interface, the user must assert x_avail high. In turn, this causes the CoreU1LL to assert u1_x_en to the PHY-Layer device provided that u1_x_clav is asserted (high).

Write Interface

Whenever the CoreU1LL asserts u1_rx_en low, the w_phy_act signal is asserted high to indicate that the ingress user interface is active. The w_enable signal will remain low until the Link-Layer begins to transfer a cell. Since the CoreU1LL translates from 8-bit data at the UTOPIA interface to 16-bit data at the user interface, w_enable is asserted for one clock cycle while a data word is valid. W_adr is incremented on the next rising-edge of u1_rx_clk, and then w_enable is deasserted for one clock cycle (except during insertion of the UDF2 byte, as shown in Figure 8). W_adr increments from 00 to 1B hex (27 words).

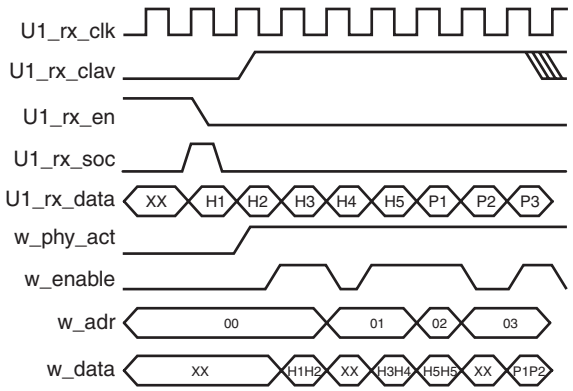

Figure 8 • *Write Interface Cell Transfer*

Once a complete 54-byte cell has been written to the user interface (w_adr = 1B hex and w_enable high), w_adr will reset to 00 hex, and w_enable will be deasserted. If either u1_rx_clav or w_avail are deasserted (low), then the CoreU1LL deselects the PHY-Layer device and w_phy_act returns low (inactive). On the other hand, if the PHY-Layer device is prepared to send another cell (u1_rx_clav is high) and user logic is able to accept another cell (w_avail remains high), the w_phy_act signal remains active (high), and the CoreU1LL block accepts a back-to-back cell from the PHY-Layer device. The CoreU1LL will wait for the PHY-Layer to assert u1_rx_soc and then begins asserting w_enable during each valid data word and incrementing w_adr (Figure 8).

Read Interface (egress)

When r_avail is asserted high at the user interface and the u1_tx_en signal is asserted low by the CoreU1LL, the CoreU1LL begins accepting data on the user interface. Once a cell transfer has begun, the CoreU1LL transfers 27 words of data regardless of the state of r_avail. The CoreU1LL asserts r_buf_en high, expecting to accept data at the r_data inputs on the next rising-edge of u1_tx_clk, as illustrated in Figure 9.

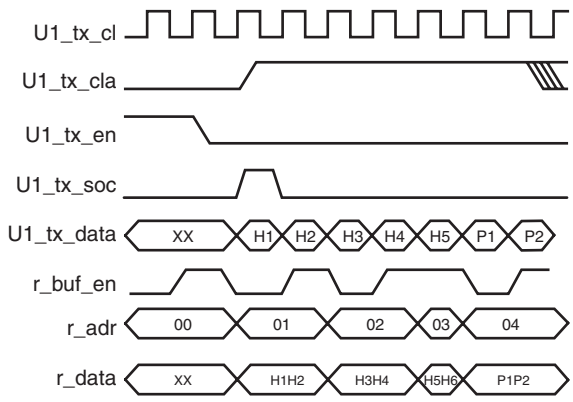

Figure 9 • *Read Interface Cell Transfer*

The CoreU1LL provides r_adr as a word count (00 to 1B hex) and increments whenever the core accepts data at the r_data pins. Since the CoreU1LL translates from 16-bit data at the user interface to 8-bit data at the UTOPIA interface, r_buf_en is asserted for one clock cycle. Data is accepted on the following rising edge of u1_tx_clk, and the r_adr is incremented.

Then r_buf_en is deasserted for one clock cycle except after the third data word when xlate is low (53-byte mode), or when a back-to-back read operation is needed in order to get the first payload byte in time.

The cycle is repeated until r_adr reaches 1B hex and the last two bytes of the ATM cell are sent. At this point, r_adr is reset to 00 hex. If r_avail indicates that another cell is immediately available, and u1_tx_clav remains high, the CoreU1LL will immediately begin sending the next cell (Figure 10 on page 5). Otherwise, r_buf_en remains low until the CoreU1LL begins to transmit another cell.

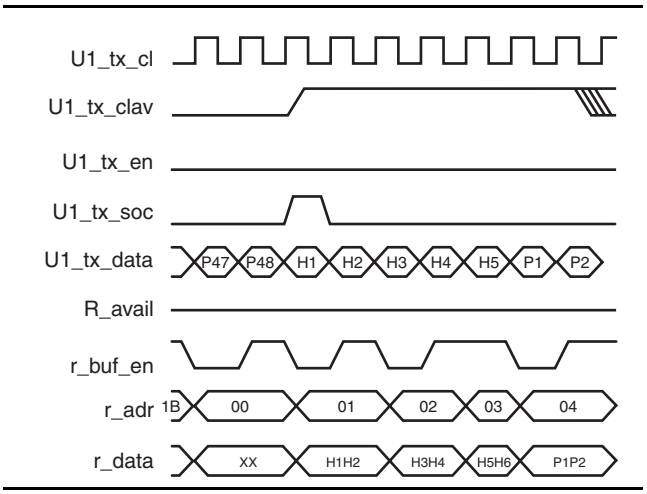

Figure 10 • *Back-to-Back Read Cell Transfer*

Ordering Information

Order CoreU1LL through your local Actel sales representative. Use the following numbering convention when ordering: CoreU1LL-XX, where XX is listed in Table 4. All four options include both VHDL and Verilog netlists, testbench source files, and simulation models targeting both ProASIC^{PLUS} and Axcelerator device families.

CoreU1LL-XX, where XX is:

Table 4 • *Ordering Codes*

XX	Description
EV	Evaluation Version
SN	Single-use Netlist for use on Actel devices
AN	Netlist for unlimited use on Actel devices
AR	RTL for unlimited use on Actel devices
UR	RTL for unlimited use and not restricted to Actel devices

Datasheet Categories

Product Definition

This version of the datasheet is the definition of the product. A prototype may or may not be available. Data presented is subject to significant changes.

Advanced

This version of the datasheet provides nearly complete information for a prototype IP product. Code is fully operational, but may not support all features expected in the production release. A prototype core and a preliminary testbench are available.

Production (unmarked)

This version of the datasheet contains complete information on the final core. All components are fully operational and the core has been thoroughly verified.

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