Actel eX, SX-A and RT54SX-S I/Os

Introduction

The eX, SX-A and RT54SX-S devices have a variety of advanced I/O features, which are not available in other Actel devices, such as PCI compliance, slew-rate control and pull-up/pull-down resistor. Furthermore, these devices are the first to support both hot swap and cold sparing with the new I/O features. This application note provides guidelines for designing with selectable I/O standards in eX, SX-A and RT54SX-S devices and covers I/O architectural features, all I/O standard supports, operating condition and unused I/Os. Additionally, this document also contains some design tips regarding eX, SX-A and RT54SX-S I/Os.

I/O Architectural Features

To support hot-swap provisions of the CompactPCI specification, the PCI device buffers must meet the AC specifications for 5V signaling. Input buffers require a clamping diode to ground. The clamp diode to V_{CCI} is required in the 3.3V PCI system only.

As shown in Figure 1, for the Input Buffer configuration, the pull-up clamp diode is ON ONLY for 3.3V PCI I/O standard, and OFF for all other I/O standards. The pull-down clamp diode is always ON regardless of the I/O standards.

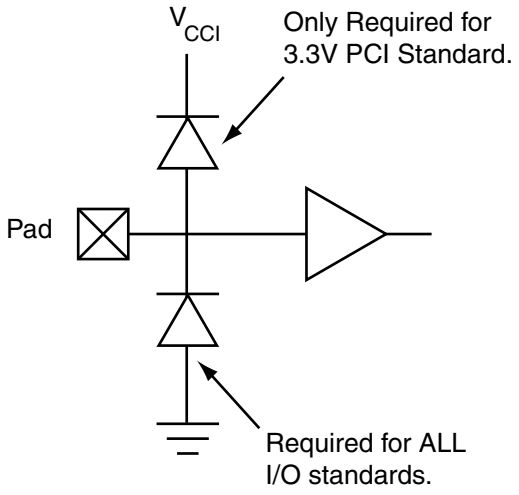

Figure 1 • *Input Buffer*

I/O Standards Support

Table 1 lists the supported I/O standards for eX, SX-A and RT54SX-S device families in addition to all supported I/O features or with standard default setting, such as the high output slew-rate for PCI mode and loading value for different I/O standards shown in Table 1. The user can also modify the default setting for each standard. This will be discussed in more detail in the next section.

Table 1 • *Summary of All Supported I/O Features*

I/O Standard	Device			Output Slew-rate Control	Power Up State Control	Hot-Swap	Loading (pf)
	SX-A	eX	RT54SX-S				
2.5V LVCMOS	✔	✔		✔	✔	Yes	35
3.3V LVTTL	✔	✔	✔	✔	✔	Yes	35
5V TTL	✔	✔	✔	✔	✔	Yes	35
3.3V PCI	✔		✔	High*	✔	**NO**	10
5V PCI	✔		✔	High*	✔	Yes	50
5V CMOS			✔	✔	✔	Yes	35

Note: ** PCI mode sets output slew-rate High by default.*

Designing I/Os With Actel Software

Table 1 on page 1 indicates that pull-up/pull-down state during power-up is controllable for all the I/O standards and output slew-rate is selectable in TTL (LVTTL) and CMOS mode. The loading is set for all the standards to the defined value as shown in Table 1 on page 1.

We can also set CUSTOM mode as an I/O standard in the PinEdit tool of the Designer Series software, by selecting CUSTOM from the I/O standard cell in the desired macro row. In CUSTOM mode, all output slew rates and loadings are user selectable on an individual basis. For example, PCI mode output can be set to low slew-rate (Figure 2). Please check the Actel web site for future application notes concerning the slew rate for different devices.

	Port Name	Macro Cell	Pin #	Fixed	I/O Standard	IO Threshold	Slew	Power Up State	Hot Swap	Loading (pf)
1	L32_O_CMOS_H	ADLIB:OUTBUF	193	☑	CUSTOM	PCI	Low	None	On	60
2	MCLK_O_CMOS_H	ADLIB:OUTBUF	187	☑	PCI	PCI	High	None	On	50
3	SB2_O_CMOS_H	ADLIB:OUTBUF	199	☑	CUSTOM	CMOS	High	None	On	50
4	MCLKX4_O_PCI_H	ADLIB:OUTBUF	177	☑	PCI	PCI	High	None	On	50
5	SB2_O_TTL_H	ADLIB:OUTBUF	197	☑	TTL	TTL	High	None	On	35

Figure 2 • *Setting I/O Features in PinEdit of Designer Software*

Operating Condition

Table 2 lists the specific power supply requirements for eX, SX-A and RT54SX-S FPGAs. The maximum input tolerance is 5V for all of the I/O standards except 3.3V PCI. When input signal V_{IN} is greater than V_{CCI} (3.3V or 2.5V), the maximum leakage current can be reached 1mA at about V_{CCI} + 0.7V. This amount of maximum current will be clamped down due to the hot-swapping feature and will not damage the device.

The eX, SX-A and RT54SX-S devices are designed to accommodate any possible power-up sequence. However there are some recommendations for SX-A and RT54SX-S to comply with hot-swap and cold-sparing requirements. Both V_{CCA} and V_{CCI} should be tied LOW during cold sparing. For more information, please refer to the application note, Actel *SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 2 • *Power Supply*

V_{CCI} (V_{CCA}=2.5V)	Device			Maximum Input Tolerance	Maximum Output Drive
	SX-A	eX	RT54SX-S		
2.5V	✔	✔		5.0V	2.5V
3.3V	✔	✔	✔	5.0V*	3.3V
5.0V	✔	✔	✔	5.0V	5.0V

Note: **3.3V PCI mode is not 5.0V tolerance due to the clamp diode, but 3.3V tolerance.*

Unused I/Os And Clocks

In the eX, SX-A and RT54SX-S families, unused I/O pins are automatically tristated by the Designer software. Although termination is not required, Actel recommends to tie unused pins to "LOW" for safety, in case undesired signal is applied to an unused I/O. Driving unused I/Os is acceptable if the driving signal is under I/O tolerance level. For SX-A and RT54SX-S, if the clamping diode is disabled in Designer software, the unused I/Os are 5V tolerance. The user can specify this by selecting the check box for fuse generation; otherwise, the unused I/Os are 3.3V tolerant at 3.3V V_{CCI}.

If JTAG is not reserved in the design, the unused JTAG pins will behave as normal unused I/Os, so user should follow the above recommendation. If JTAG is reserved, then JTAG pins are dedicated test pins. These pins are 5V tolerance as well if the clamping diode is disabled in Designer software.

For RTSX72S and A54SX72A, CLKA/B and QCLKA/B/C/D are Clock-I/O pins (can be configured as clock and/or user I/O). When these pins are not used, Actel recommends to tie them to "HIGH" or "LOW" on the board to avoid power dissipation due to "floating" the clock input buffer. For all other eX, SX-A and RT54SX-S devices, their CLKA/B pins are clock-only pins (not clock-I/Os). Unused CLKA/B pins must NOT be left floating.

Design Tips

How To Achieve 5V Drive with 3.3V V_{CCI}?

To configure an Actel SX-A or RT54SX-S device to drive 5V with V_{CCI}=3.3V, users can utilize an Open Drain configuration of the I/O cell with an array inverter cell and an external pull-up resistor to 5V. The recommended configuration is as shown in Figure 3 on page 3. The I/O configuration must be set to LVTTL to disable the PCI Clamp Diode.

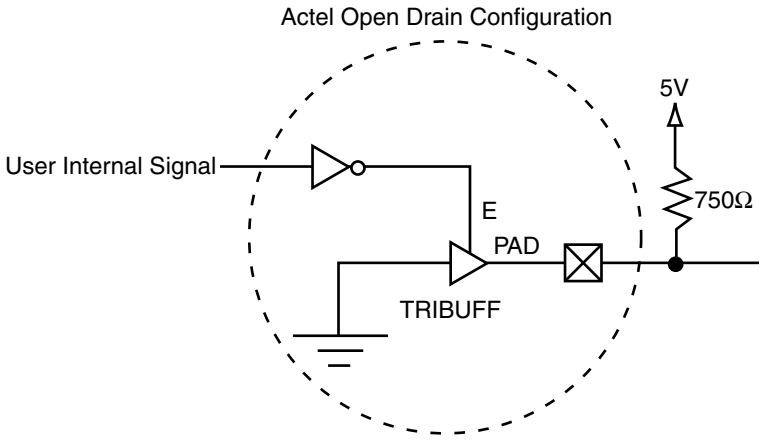

Figure 3 • Open Drain Configuration for SX-A or RT54SX-S

TRST Pin For RT54SX-S In Space Application

The TRST pin is a dedicated reset pin for RT54SX-S, and therefore, the user should reserve TRST pin in SX-A prototyping design. After prototyping a design with SX-A, users may need to fix TRST to GND in final production with RT54SX-S for space applications. The layout on TRST should include a 0Ω resistor or bus wire to be installed for flight usage, where an actual bus wire jumper has a very low probability for failure. This does require an additional step for the customer's board after debug verification is complete and system burn-in begins, but it is the best option.

Conclusion

Actel eX, SX-A, and RT54SX-S devices support a variety of advanced I/O features for commercial and aerospace applications. To take advantage of high performance, low power consumption, hot-swap and cold sparing features, please follow the recommendations described in this documentation and refer to the following references for more information.

References

All application notes can be found at:

http://www.actel.com/techdocs/appnotes/index.html

eX: *Design for Low Power in Actel Antifuse FPGAs*

SX-A/RT54SX-S: *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*

TRST pin: How do I Set the TRST Pin during JTAG and Debug Mode for the RTSX, RT54SX-S, and SX-A Devices

http://www.actel.com/apps/guru/feb00/jy1316.html

http://www.actel.com

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