ProASIC PLUS FPGA Family

Key Features

- Reprogrammable / Nonvolatile Flash Technology
- Low Power
- Secure
- Single Chip / Live at Power Up
- 1M Equivalent System Gates
- Cost Effective ASIC Alternative
- ASIC Design Flow
- FlashLock™ — Secured by Actel's unique FlashLock™ technology. ProASIC PLUS devices have a 79 to 263 bit Flash-based lock to secure programmed I/P and configuration data.

The Capabilities of ASICs with the Flexibility of FPGAs

Actel's second generation Flash product, ProASIC PLUS, expands on all the features and benefits offered by the original ProASIC family. Now ASIC capabilities are available in a single chip, high-density programmable product. Based on cost-effective .22µ Flash technology, ProASIC PLUS offers a unique combination of features and benefits that provide designers the best of both worlds. Like an ASIC, nonvolatile ProASIC PLUS is live at power up, offers a wide range of densities, and has very low power consumption. ProASIC PLUS also adds reprogrammability and enhanced security to protect sensitive Intellectual Property. Its fine-grained architecture enables designers to leverage existing ASIC or FPGA design flows and tools. ProASIC PLUS is the first high-density reprogrammable product that combines the capabilities of ASICs with the flexibility of FPGAs.

ProASIC PLUS

High Density

With densities ranging from 75,000 to 1,000,000 system gates and up to 198kbits of embedded SRAM, Actel's ProASIC PLUS family delivers high density programmable logic solutions. Using a standard Flash-based CMOS process, ProASIC PLUS devices combine high performance and low power with nonvolatility and in-system reprogrammability. Combining industry standard ASIC or FPGA design methodologies and tools, ProASIC PLUS devices offer true reprogrammable system integration solutions.

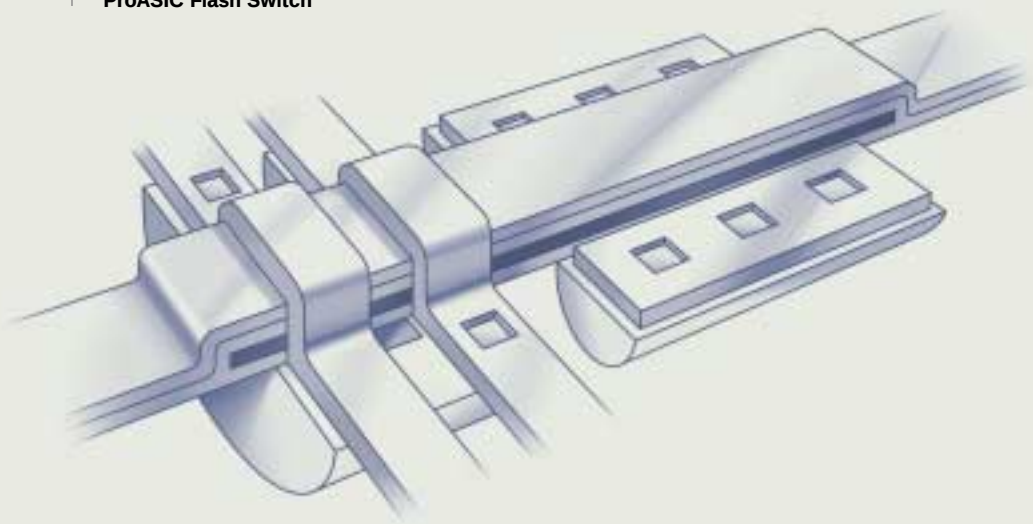
High Performance Architecture

Based on .22µm Flash technology that allows for performance enhancing architectural innovations, the small size of the Flash cell allows more programmable switches to be added into the routing, resulting in low resistance and low capacitance routing segments. These segments offer predictable performance, improved utilization, and greater routing efficiency. The fine-grained logic dramatically improves logic utilization and predictability. The ProASIC PLUS devices also offer the ability to fix pins at close to 100% logic utilization, resulting in easier system design and less design iterations. ProASIC PLUS devices are the optimal programmable solution to allow designers to easily meet performance goals.

Nonvolatile and Reprogrammable

Because the ProASIC PLUS devices are nonvolatile, they retain their configuration. This eliminates the cost of a boot PROM and the associated board space. Nonvolatile also means live at power up, so there is no period of nonfunctionality while configuration data is being downloaded from an external device as required in the case of SRAM-based programmable devices. Additionally, ProASIC PLUS devices allow designers the flexibility to reprogram their devices if design changes are necessary. As they are live at power up, ProASIC PLUS devices may implement the logic to control the power up sequencing of other parts on the board.

ProASIC Flash Switch



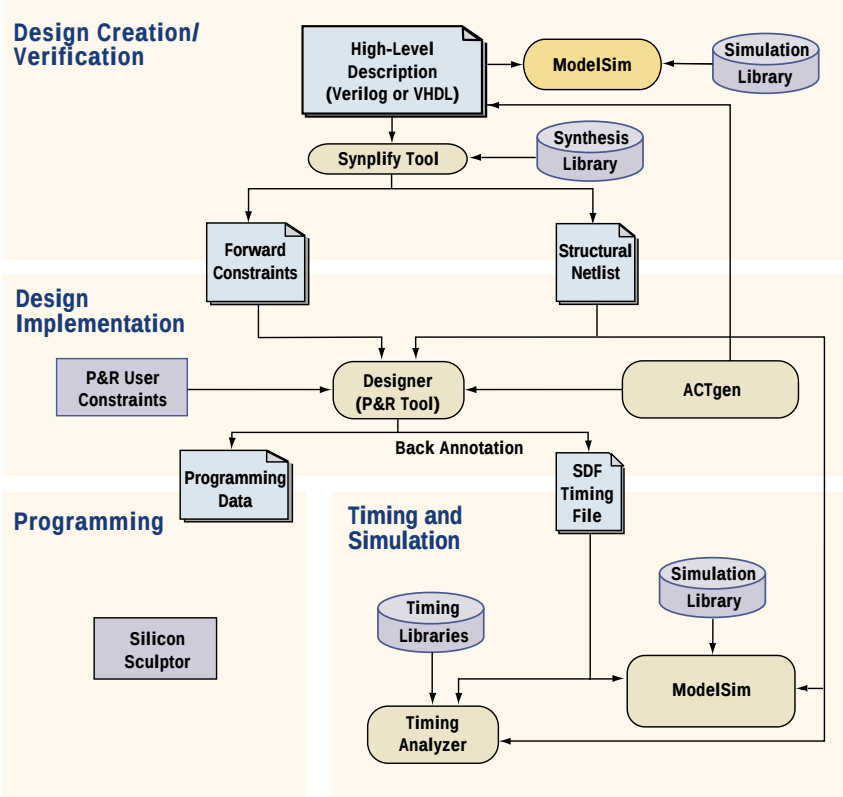
Design Security That Really Works

The nonvolatile Flash-based ProASIC PLUS family requires no boot prom so there is no vulnerable external bitstream that can be easily copied. ProASIC PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security. A private key set by the user enables FlashLock. Once enabled, the contents of a programmed ProASIC PLUS device cannot be read back without first unlocking the User Key. This built-in security feature requires no external battery or additional components; it's one of the built-in advantages of Flash FPGAs. The Flash cells are located beneath four metal layers. Since these layers cannot be removed without disturbing the charge on the gate, devices cannot be easily deconstructed to decode the design. ProASIC PLUS with FlashLock is highly resistant to both invasive and non-invasive attacks, valuable IP is protected and design security is assured.

Low Power

ProASIC PLUS exhibits power characteristics similar to an ASIC, making it an ideal choice for battery-operated and other power-sensitive applications.

Unlike SRAM FPGAs, ProASIC PLUS is live at power up, retains configuration information in nonvolatile Flash, and does not have to be re-initialized each time power is applied. In addition, with ProASIC PLUS there is no power-on current surge and no high current transition, which exists on SRAM FPGAs. ProASIC PLUS also has significantly lower dynamic power consumption than SRAM FPGAs to further maximize power savings.

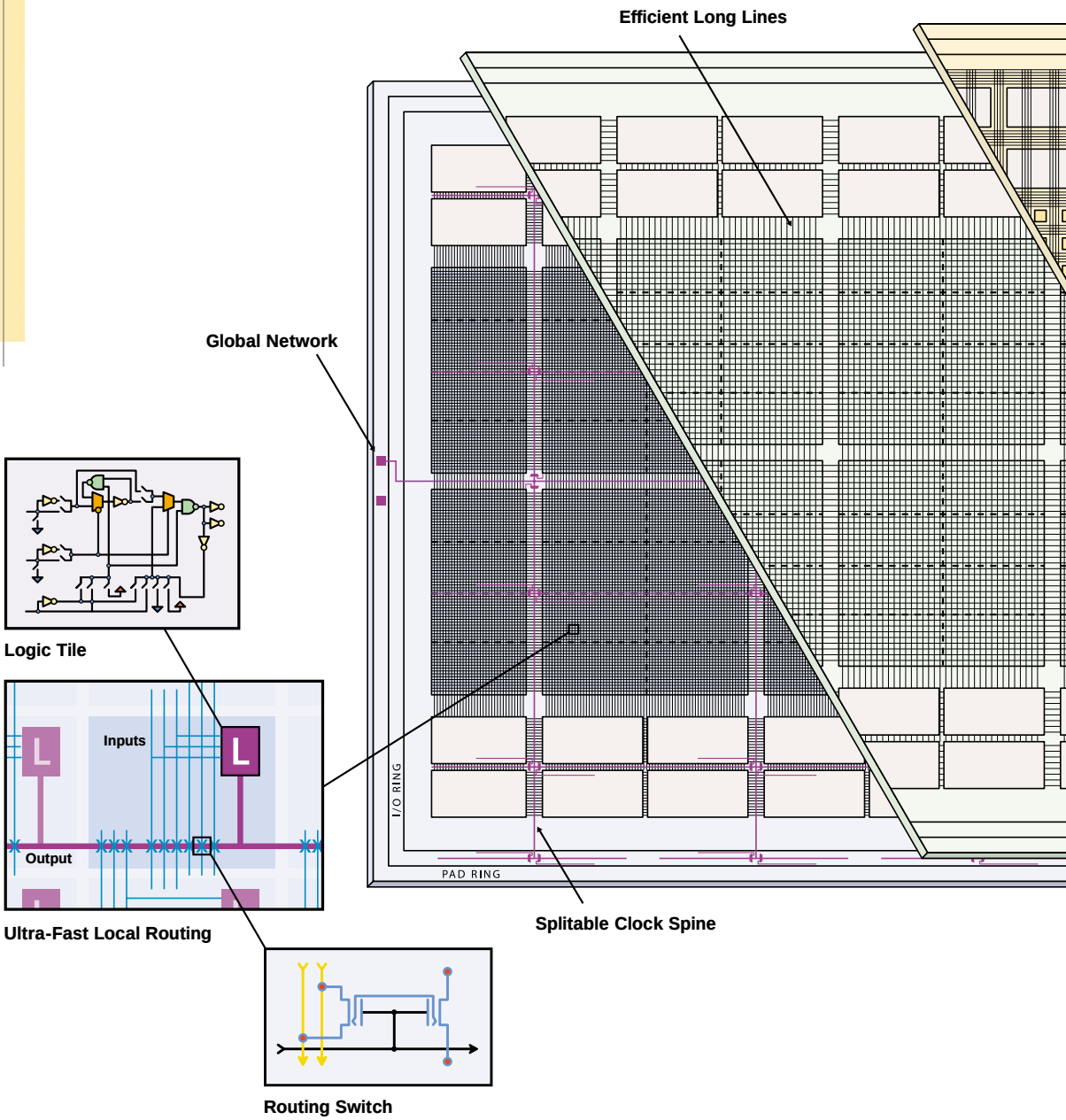


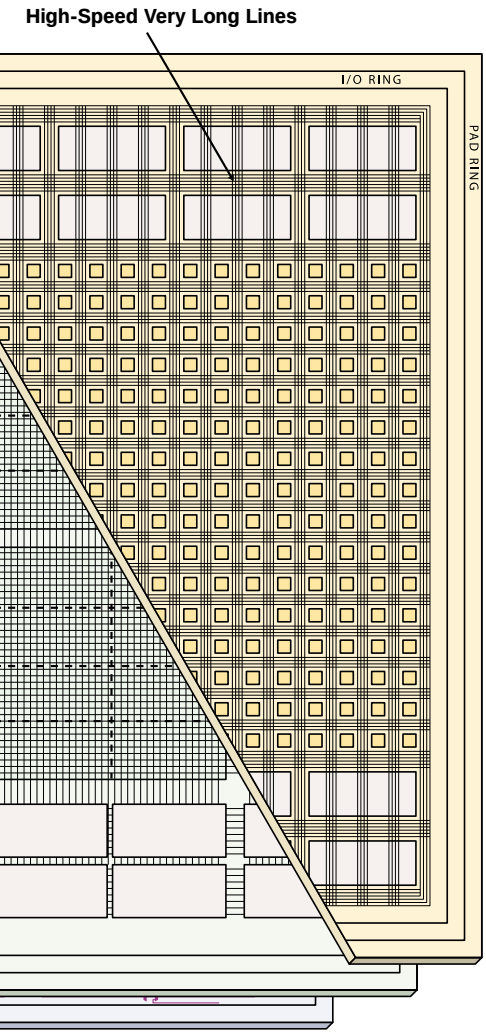
ASIC and FPGA Design Flows

ProASIC PLUS is supported equally well in ASIC and FPGA design flows. Designers accustomed to working in an FPGA design flow can take advantage of the ease of use and fast run times they have come to expect. ASIC designers will appreciate the high degree of user control and easy integration into their existing design environment and tools.

Because of the architecture, ProASIC PLUS devices can use the same VHDL and Verilog HDL descriptions that are targeted for gate arrays and standard cells, freeing the designer from the limitations imposed upon HDL by some FPGA architectures. Additionally, standard ASIC tools are supported, protecting the designers' investment in tools and training while streamlining the design environment. As a result, the design team can focus on getting the design to market faster.

ProASIC PLUS Routing Hierarchy



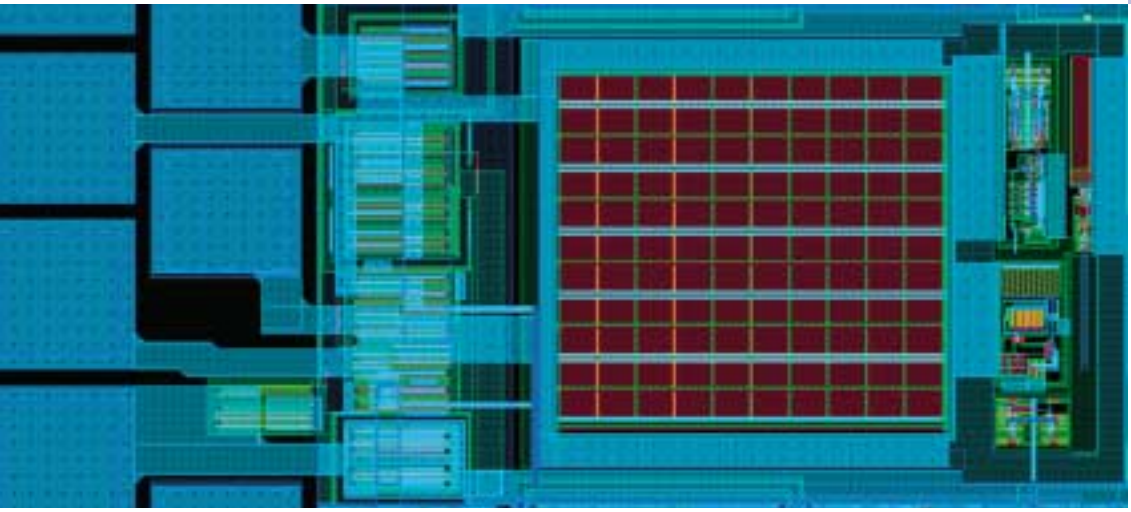


The Density and Flexibility of Sea-of-Tiles

ProASIC PLUS's unique architecture provides the granularity expected of gate arrays but in an FPGA. The device core consists of a Sea-of-Tiles, each of which can be configured into 3-input/1-output logic function by programming the appropriate Flash switches. The family offers from 3,072 to 56,320 tiles on a die. Combined with abundant routing resources, this approach also enables nearly 100% logic utilization and successful implementation of highly congested designs.

User-Friendly Hierarchical Routing

Routing resources are organized in four hierarchical levels to provide maximum routability performance with optimal interconnect routing flexibility. Ultra fast local resources allow a direct connection from the output of every tile to I/O buffers, memory blocks, or the eight surrounding tiles. Efficient long line resources, of 1, 2, or 4-tile length, provide greater distance routing and higher fanout connections. At the third level, high-speed very long line resources run vertically and horizontally across the chip to minimize delay, and accommodate high fanout nets. At the highest level, high performance global networks are used to distribute clocks, resets, and other nets requiring high fanout with minimal delay and skew. These clock networks can be split into multiple segments to accommodate external or internal clock intensive applications.



Innovative High-Density Memory Schemes

ProASIC PLUS devices provide up to 198kbits of embedded two-port SRAM, organized in 256x9 blocks. Each block can be configured as synchronous or asynchronous, FIFO or SRAM. The designer can configure the block as an independent memory or link it to other blocks to form larger, more complex memories. Each block also includes hardwired decoder logic, I/O circuits, parity generation/detection circuits, FIFO flag generation logic and timing and control circuits, therefore minimizing external logic gate counts and complexity. All these embedded features provide users with 24 various RAM and FIFO configurations and additional depth and width parameters.

User Configurable I/Os

The ProASIC PLUS devices provide fully configurable I/Os for greater flexibility and performance. Each pad can be programmed as an input, an output, a three-state driver, or a bidirectional buffer.

Additional programming options include pull-up resistors and selectable drive and slew rates that enable close matching to a wide range of bus interface conditions. ProASIC PLUS devices provide the capability to individually select each input/output device to interface with either 2.5V or 3.3V components.

Unique Clock Conditioning Circuitry

Each ProASIC PLUS device contains two clock-conditioning blocks, each consisting of a phase lock loop (PLL) core, delay lines, and clock multiplier/dividers. Additionally, each conditioning block contains all the circuitry needed to provide bidirectional access to the PLL, which runs at up to 240 MHz. Furthermore, a wide range of factors of up to 64 can divide incoming clock signals. The clock conditioning circuit can alter clock delay up to 4ns, in increments of 0.25ns, and can provide clock phases of 90, 180 or 270 degrees. The PLL can be re-configured dynamically during operation to change its parameters. In addition, two LVPECL differential input pairs accommodate high-speed clock inputs.

Design Tools

ProASIC PLUS devices are supported by Actel Designer Software as well as by industry standard ASIC and FPGA CAE tools. This open design environment allows designers to easily leverage their existing tool sets.

Actel's Designer Software includes place-and-route, timing analysis, and ACTgen for arithmetic, logic, memory, and PLL. ACTgen also provides all the software needed for configuration of the PLL clock conditioning circuit. While the PLL has no placement mobility, ACTgen allows users to associate placement and routing floorplan constraints hierarchically in order to more easily and efficiently explore floorplan alternatives.

Available for Solaris,™ HP™-UX and Windows 98/NT 4.0/2000/XP, Designer Software accepts standard netlists in Verilog, VHDL or EDIF formats, performs place-and-route of the design into the selected device, and provides pre- and post-layout delay reports and SDF files for back annotated simulation or static timing analysis.

Third Party Support

	Synthesis	Simulation	Static Timing
Synopsys	Design Compiler FPGA Compiler II FPGA Express	VSS VCS Scirocco	Prime Time
Cadence	BuildGates	NC-VHDL/NC-Verilog Verilog-XL	
Exemplar	LeonardoSpectrum		
Model Technology		Model*Sim*	
Synplicity	Synplify		

Programming

ProASIC PLUS devices offer in-system programming capabilities. To program a device, the configuration data is supplied through a standard JTAG interface either from a microprocessor, Silicon Sculptor II, or Flash Pro. For applications without a microprocessor, Silicon Sculptor II is best for production volumes while the Flash Programmer, with its small size and ease of portability, is ideal for prototyping.

ASIC Conversion

For high volume designs, Actel offers a proven conversion path for ProASIC PLUS devices. ProASIC PLUS's fine-grained architecture is the closest in the industry to that of an ASIC, simplifying and speeding the conversion process. By remapping the functionality of a ProASIC PLUS design into a standard cell ASIC netlist, designers can achieve both fast time-to-market speed and low production costs. For more information about this service, refer to Actel's Flash to ASIC Conversion Program product information brochure.

ProASIC[PLUS] Product Offering

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Max Registers	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM bits	27k	36k	72k	108k	126k	144k	198k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
Max User I/O	158	242	290	344	454	562	712
Packages	PQ 208 FG 144 TQ 100	PQ 208 BG 456 FG 144 FG 256 TQ 100	PQ 208 BG 456 FG 144 FG 256 FG 484	PQ 208 BG 456 FG 144 FG 256 FG 484	PQ 208 BG 456 FG 256 FG 676	PQ 208 BG 456 FG 676 FG 896	PQ 208 BG 456 FG 896 FG 1152

For more information regarding the ProASIC[PLUS] with FlashLock FPGA Family, please contact your local Actel sales representative.

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