Prototyping for the RT54SX-S Enhanced Aerospace FPGA

Actel provides radiation tolerant FPGA devices for use in Aerospace applications. However, since the enhanced environmental properties of radiation tolerant devices are not required during prototyping, an inexpensive commercial device can be substituted during the design phase. With the introduction of the RT54SX-S family, customers can now use commercial design techniques and devices when designing and prototyping for this radiation tolerant family of devices. While the commercial devices are functionally equivalent to radiation tolerant devices, they differ architecturally and in their timing.

Design Difficulties with Previous Devices

Prior to the introduction of the RT54SX-S devices, designers often had to make the trade-off between SEU requirements and usable gates. While a LETth of 38 MeV-cm^2/mg is typically considered SEU immune, no FPGA device register was able to offer a sufficient LETth value to be considered SEU immune. Users of Actel's radiation tolerant FPGA's had the option of implementing triple module redundancy using three registers and a majority voting module. This method used four logic elements to implement a single register making it an expensive option in terms of utilization, and limited the amount of logic designers were able to implement in each device. These manually created TMR registers are often susceptible to glitches.

The RT54SX-S family of devices introduces a new SEU hardened register. By internally implementing a self-refreshing triple module redundant register, the RT54SX-S device has achieved a register that has a LETth of greater than 40 MeV-cm^2/mg. As a result, customers no longer need to worry about implementing TMR registers in their design or trading off between SEU immunity and sacrificing valuable device logic. Additionally, since these registers are built into the device and are not implemented using placement or routing of user gates, they are not prone to glitches.

Commercial Equivalents for the RT54SX-S Devices

Compatible Devices

Since the RT54SX-S family of devices are 100% library compatible and density-matched with the 54SX-A family of devices, designers can simply select a 54SX-A equivalent device when prototyping for a RT54SX-S device. Refer to the table below for the correlation between the 54SX-A device and matching RT54SX-S device.

	32,000 Gates	72,000 Gates
RT54SX-S device	RT54SX32S	RT54SX72S
54SX-A equivalent	A54SX32A	A54SX72A

In order to facilitate using a commercial device for prototyping, Actel has designed the RT54SX-S device in the CQ208 package to be pin compatible with the equivalent 54SX-A device in the CQ208 and PQ208 packages. This provides a simple method for customers to make a drop-in replacement from prototyping to production. Please refer to the "Prototyping with PQ208 for CQ208 Packages" on page 2 section below for information on solder pad dimensions to be used if a prototype socket or either a CQ208 or PQ208 package is being employed.

Unfortunately, there is no equivalent plastic device for the CQ256 package, so prototyping for this device package will have to be done using a socket in order to match package footprint layout.

Other Device Considerations

Users who employ the 54SX-A devices for prototyping must remember to reserve the JTAG reset pin (TRST) in the device selector window in the Designer software. Reserving this JTAG reset must be done to ensure that no user I/O is assigned to this pin. During prototyping, users can employ JTAG by pulling this pin high. However, during flight, the RT54SX-S devices require the JTAG reset pin to be tied low. The RT54SX-S devices have the JTAG reset pin hardwired. Selecting this pin in the 54SX-A device will help to ensure a compatible pin layout between the 54SX-A prototyping device and the RT54SX-S flight device.

Aside from the enhanced SEU, the RT54SX-S device has another capability, which the 54SX-A device lacks.

The 54SX-A device has adjustable input trip points for TTL and PCI modes of operation. The RT54SX-S device has both of these as well as the addition of 5V CMOS input trip points. This feature allows the device to communicate more easily with certain CMOS devices, which are not designed for TTL noise margins.

Prototyping with PQ208 for CQ208 Packages

Figure 1 combined with Table 1 shows the standard QFP solder pad layout for Actel quad flat packs and their associated dimensions.

Prototyping Methodologies

Because the RT54SX-S device has enhanced SEU hardened registers, users no longer need to employ special design techniques or special macros to improve SEU immunity. This allows the user to utilize commercially available synthesis tools without having to worry about special settings or taking into account extra real estate that special macros would require. The customer can now employ a commercial design flow to design and prototype for an aerospace application.

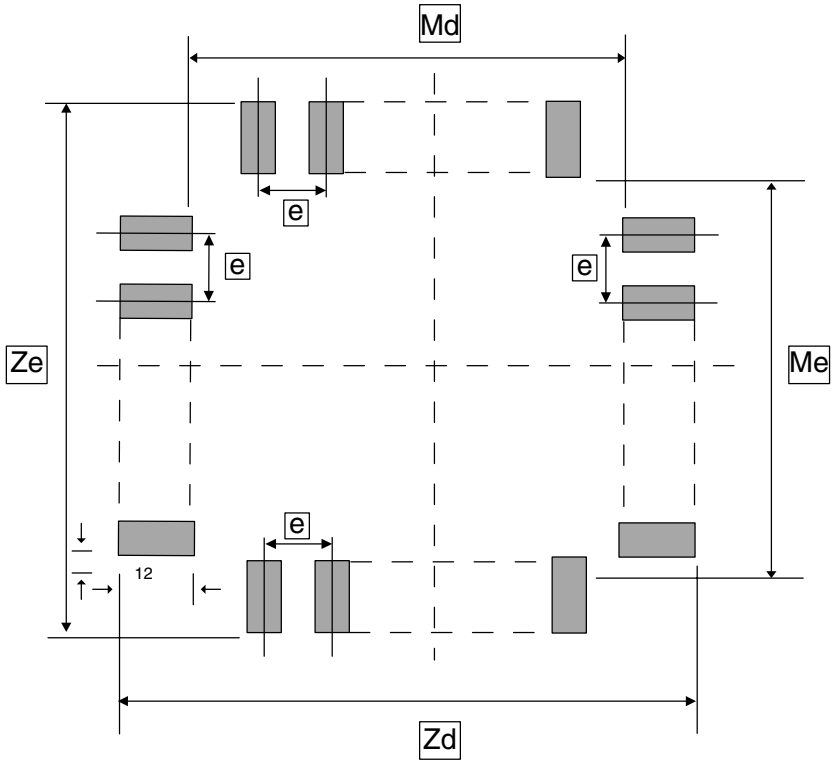


Figure 1 • *Solder Pad Layout for Actel Packages*

Dimension	PQ208/RQ208/CQ208[1]
Md	28.2 mm
Me	28.2 mm
Zd	35.1 mm
Ze	35.1 mm
e	0.5 mm
B2	0.3-0.4 mm
Socket Part Number	SY-PQ208-2

1. *Zd and Ze dimensions are based on trim and form data from Fancort Industries Inc. If using trim and form from another vendor, Zd and Ze could be different.*

Synchronous Design Methodology

Although the RT54SX-S devices are library compatible with the 54SX-A devices, architectural differences between the two devices make their internal timing different. To minimize timing related issues, Actel recommends that users implement fully synchronous designs and make use of either dynamic timing simulation tools or static timing analysis to diagnose any timing problems. Fortunately, most commercial design automation tools are optimized towards fully synchronous methodologies.

Fully synchronous designs follow three basic rules:

1. All registers that share the same data path should be connected to a common, low-skew, high-drive global or quadrant clock network, as shown in Figure 2. The A54SX32A and the RT54SX32S devices have three global clock networks which are accessible from special clock pins. These clock networks are HCLK, CLKA and CLKB. The CLKA and CLKB networks can also be accessed from special internal clock routing macros. The A54SX72A and RT54SX72S have the same three global clock networks as well as four quadrant clocks, which are the local clock network in each of the device's four quadrants. These four quadrant clocks can also be accessed using their own, special internal quadrant clock routing macros.
2. Every element on the same clock should be triggered on the same clock edge. This practice removes any dependencies on the duty cycle of the clock.
3. If multiple clock domains are employed, and data must cross between these domains, the data should be resynchronized between different clock domains using one or two registers to ensure that the data is always in a known state. This is illustrated in Figure 3.

Implementing fully synchronous design techniques may use slightly more resources on the device, but the advantage is a more stable circuit with shorter debug time. Timing verification and analysis takes less time since, in most cases, worst-case static timing analysis will suffice. Designs that are not fully synchronous often require best and worst-case timing analysis, which is not fully automated.

A fully synchronous design is also easier to migrate between process geometries and architectures. When converting from the 54SX-A device to the RT54SX-S device, static timing analysis can be used to verify that timing requirements are met.

Common Violations

Clock/Register Enable

Implementing a gated clock by using an AND gate to enable a clock, as shown in Figure 4 on page 4, could result in a glitch on the clock signal. The registers available in the 54SX-A and RT54SX-S are implemented with an active low enable. Users should employ this enable to gate the register instead of trying to modify the clock signal, illustrated in Figure 5 on page 4.

Using Combination Logic to Derive a Clock

Another common practice is to derive a clock using combinational logic, as shown in Figure 6 on page 4. The problem occurs when the decoding of combinational logic generates glitches. A safer approach is to employ a system clock to drive the clock signal of the register and use the combinational logic as an enable, as shown in Figure 7 on page 4. There is no risk of a glitch being interpreted as a clock in this case.

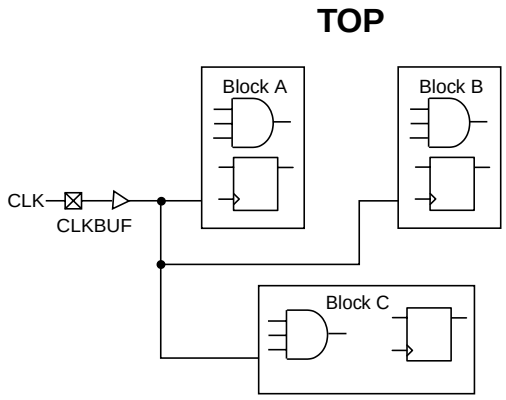
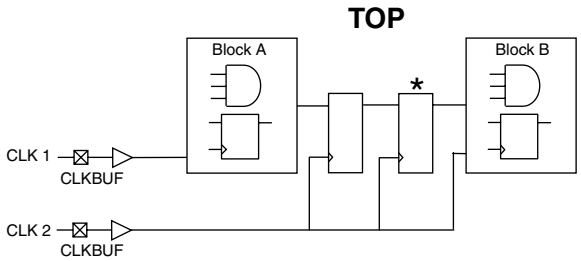


Figure 2 • *Using the Same Clock Network for Each Element*



Note: ** If the metastability settling time is relatively small compared to the CLK2 period, the user may be able to eliminate the second flip-flop.*

Figure 3 • *Synchronizing Data Between Clock Domains*

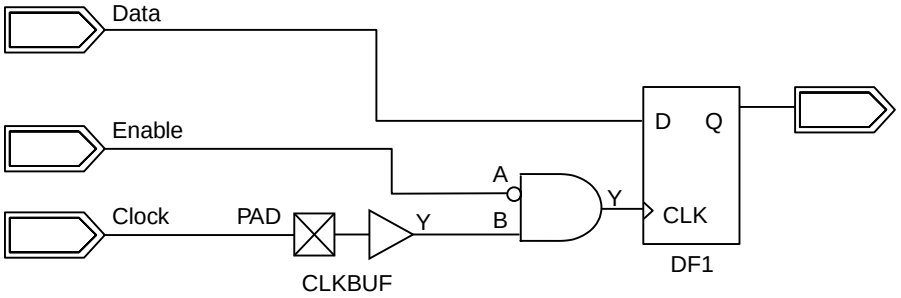


Figure 4 • *Risky Practices of Using an AND Gate as an Enable*

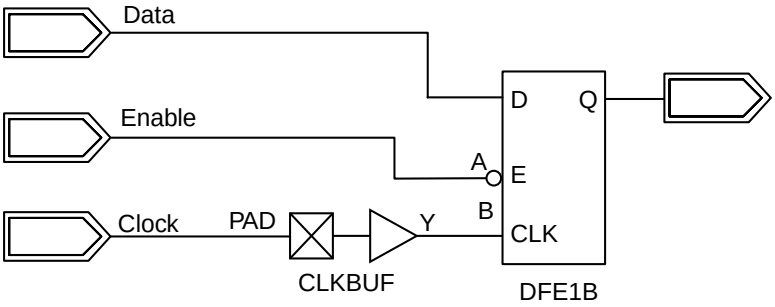


Figure 5 • *Proper Use of the Build-in Register Enable*

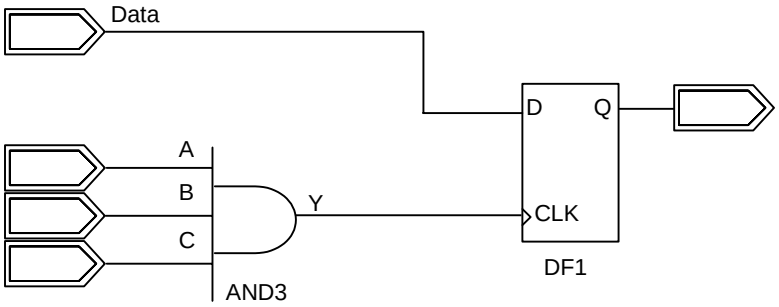


Figure 6 • *Glitch Prone Combinational Logic Used as a Clock*

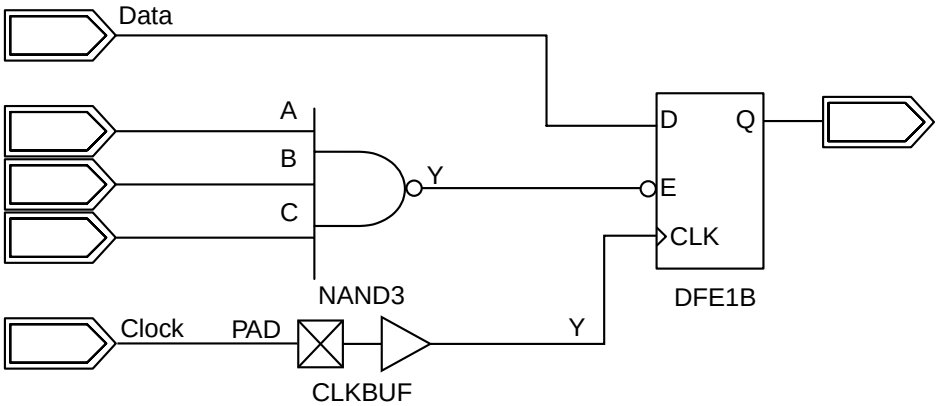


Figure 7 • *Using Combinational Logic as Enable with a System Clock*

Using a Divided Clock

The most common way to divide down a clock is to use a register and an inverted buffer for feedback. This method is acceptable to divide an incoming clock as it enters the device and redistribute it on a global clock network, as shown in Figure 8. This method becomes a problem if there are many small divided clock networks that will share data or merge data back to the original clock, as shown in Figure 8. Since there is a limit to how many internally routed clock networks each device includes, many smaller divided clocks may not be able to use the global routing resources. In this case, the skew incurred by using normal routing resources as well as the delay incurred by dividing the clock would make re-integrating the data path and performing timing analysis on this path very difficult.

A preferable method, in this case, would be to use the divided clock as an enable signal while clocking the registers from the original routed clock, as shown in Figure 9 on page 6. This allows the same system clock to be used throughout the circuit and reduces the number of global clock networks required for this section of the circuit. The disadvantage is that more routing resources are required, but the speed of the circuit and the ease of analysis may improve.

Asynchronous Feedback Loops

Variations in timing delay may make asynchronous feedback circuits unreliable. It is preferable to replace these circuits with one that changes with the system clock, as shown in Figure 10 on page 6. Additionally, note that the circuit shown in the left side of Figure 10 on page 6 may glitch when the count, for example, changes from 0111 to 1000. A reliable timing analysis that will prove the absence of a glitch to the asynchronous clearly is close to impossible to obtain. The circuit on the right hand side of Figure 10 on page 6 can be shown to be highly reliable.

Asynchronous One Shots

Asynchronous one-shot circuits are susceptible to timing problems similar to the asynchronous feedback loop, as shown in Figure 11 on page 6.

Delay insertion

Because of variation in routing and process parameters, the use of delay time specific circuits should be avoided. Circuits that depend on a specific module or buffer delay are vulnerable to routing, process, temperature, and voltage variations. Additionally, the use of delay circuits is not advisable because most EDA tools will optimize out any redundant delay circuits.

Asynchronous Data Sampling

The problems associated with sampling asynchronous data are similar to those encountered when transferring data from one clock domain to another. As in the cross clock domain example above, the use of one or two registers to buffer the data is recommended, as shown in Figure 12 on page 7.

Synchronous Preset and Clear

If the circuit on the left in Figure 13 on page 7 is preset and data is clocked on the same clock edge, the circuit could suffer from metastability problems.

Retargeting from Prototype to Flight

Retargeting from a 54SX-A device to the RT54SX-S device is simple if all of the above considerations have been met. To retarget the design, open the ADB file within Designer. Both the compile and layout icons should be highlighted. Select Tools -> Device Selection from the drop down menu. Select the RT54SX-S equivalent for the 54SX-A device. If the prototype device is an A54SX32A then select RT54SX32S; if the prototype device is an A54SX72A then select RT54SX72S.

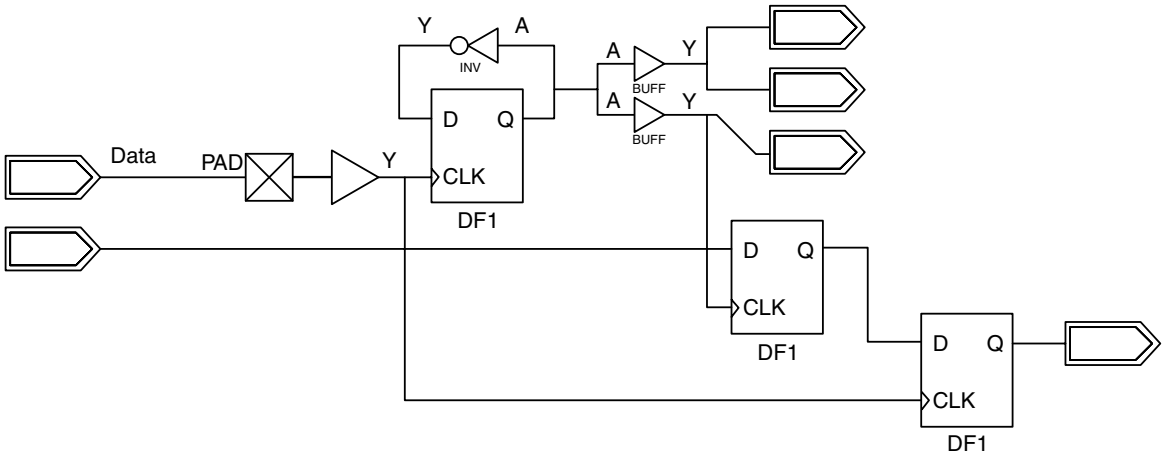


Figure 8 • Merging Clock Domain with the Original

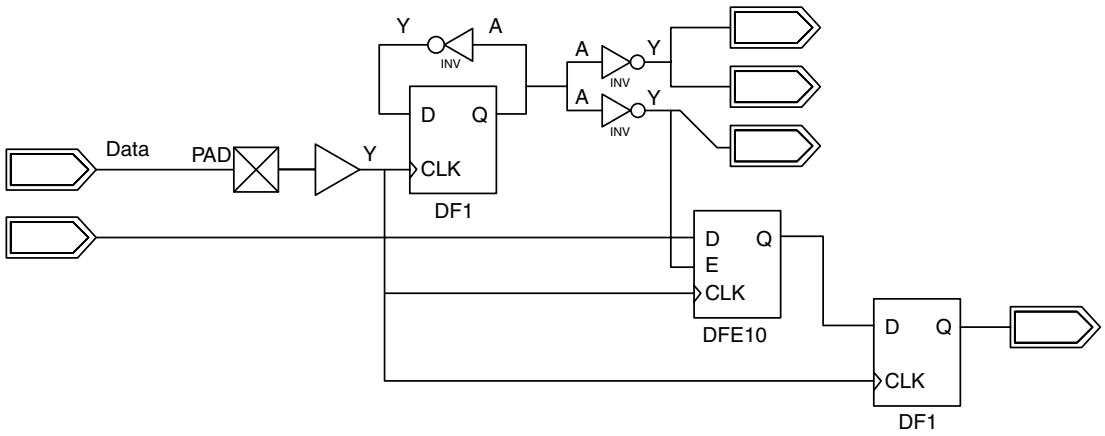
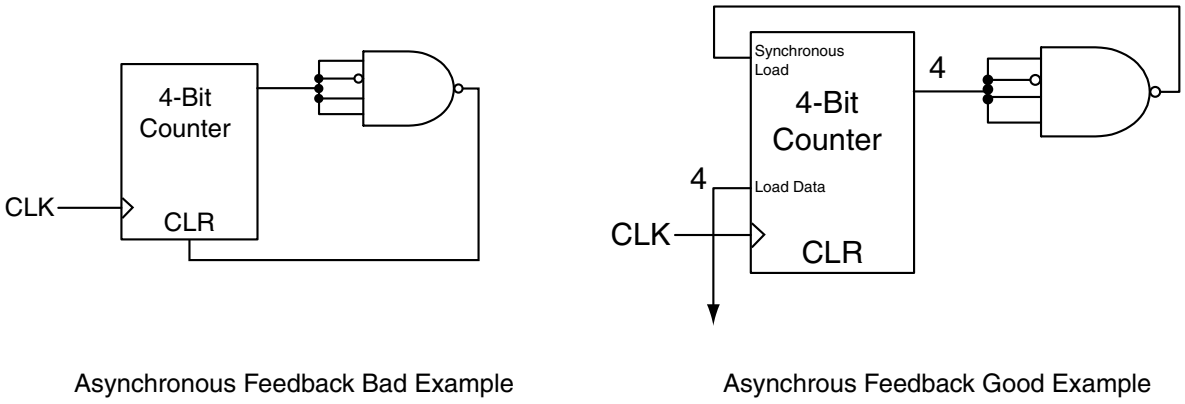


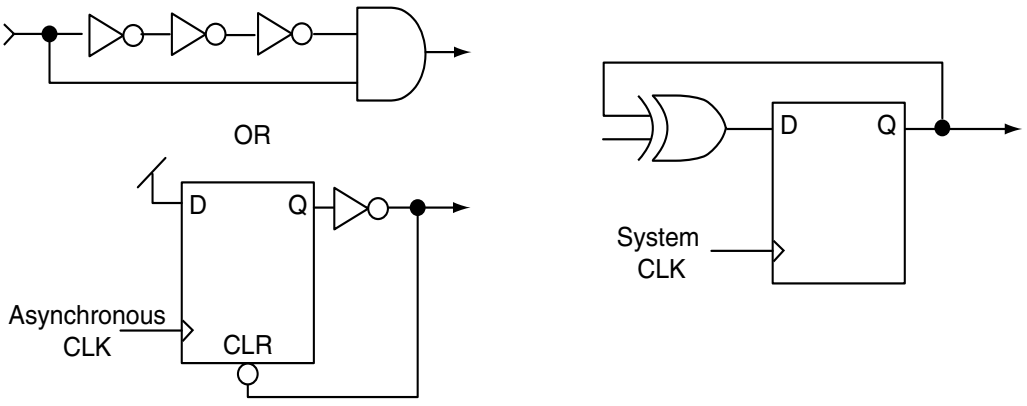
Figure 9 • *Using Single System Clock with Divided Clock Signals*



Asynchronous Feedback Bad Example

Asynchrous Feedback Good Example

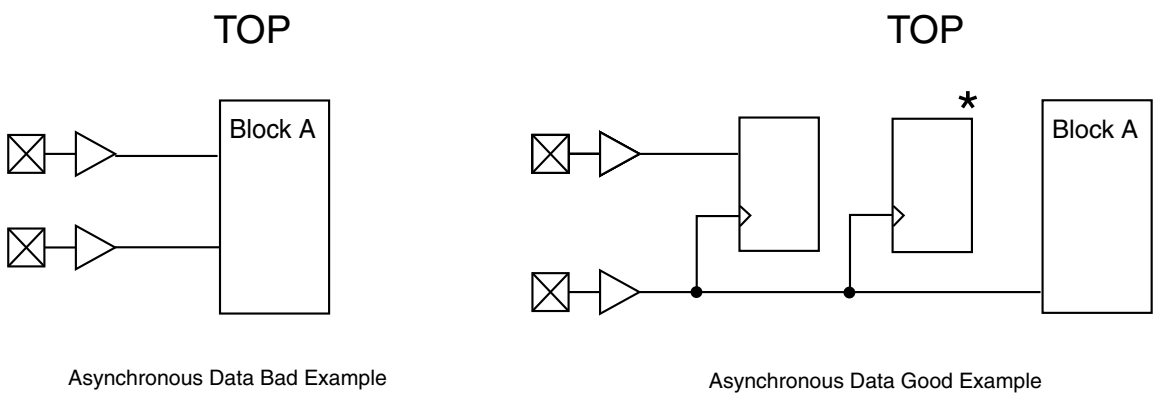
Figure 10 • *Asynchronous Feedback Circuits*



Asynchronous One Shot Bad Examples

Synchronous One shot Good Example

Figure 11 • *Asynchronous One-Shot Circuits*



Note: **If the metastability settling time is relatively small compared to the Clock period, the user may want to eliminate the second flip-flop.*

Figure 12 • *Asynchronous Data Sampling*

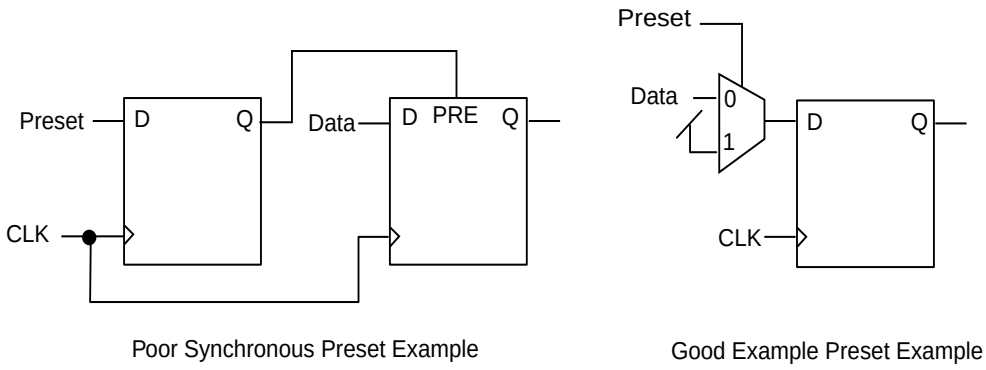


Figure 13 • *Preset and Clear*

If the CQ208 or the PQ208 was the package used during prototyping, select the CQ208 package. Since the pinouts for these device and package combinations are compatible, no pin redefining or re-layout is required. However, since timing can differ significantly, be sure to re-verify the timing of the design. If a package besides the CQ208 or PQ208 was employed, use the PinEdit tool to redefine the pinout for the new package and re-run the layout.

Even if no re-layout was required when switching from the 54SX-A to the RT54SX-S, a new AFM file must be generated for programming. While the devices are similar, the AFM programming files are different between the two devices and are NOT compatible with each other.

Conclusion

Actel's RT54SX-S devices allow aerospace designers to not only use commercial devices for prototyping but also design using commercial design techniques and "off the shelf" EDA software. The RT54SX-S family's SEU hardened registers, along with it's similarity in features, packaging pin options, and library compatibility with the 54SX-A family make it very easy for users to transition from prototyping using a 54SX-A device to using a RT54SX-S device in production. As long as the user follows some basic design guidelines, the user will only have to re-verify timing to be confident that the production device will function as expected, thereby greatly reducing the amount of time required during the design cycle.

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