In-System Programming ProASIC™ 500K and ProASIC^PLUS Devices with Silicon Sculptor and Flash Pro

FlashLock

Introduction

In order to decrease time-to-market, designers often use field programmable gate arrays (FPGAs) with the capability to be programmed in a system (in-system programming – ISP). ProASIC 500K and ProASIC^PLUS devices have this capability and can be used to get designs to market faster. This application note describes the procedure for in-system programming of ProASIC and ProASIC^PLUS devices using Silicon Sculptor and Flash Pro.

ISP Kit

To facilitate ISP of ProASIC 500K and ProASIC^PLUS devices, Actel recommends an ISP kit for use with the Silicon Sculptor or Flash Pro device programmers (Figure 1). The programming cable provides all the necessary connections, data, and supply voltages to program a device on the system board.

Figure 2 and Figure 3 show a programming header on a PCB and how it connects to a programmer. Additionally, the programming connector and header pinout are shown in Figure 4 on page 2 and Figure 5 on page 4.

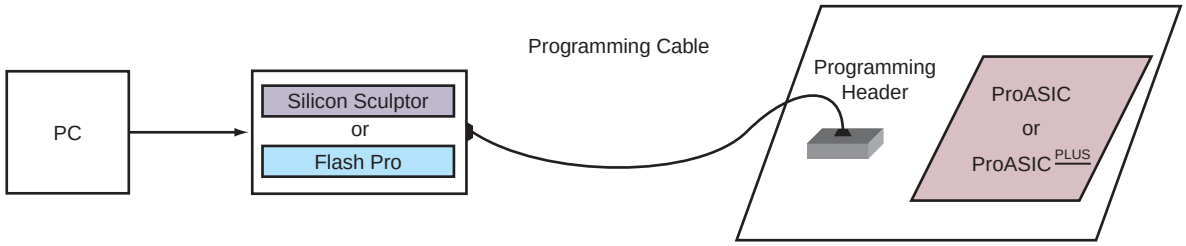


Figure 1 • Programming Setup with Silicon Sculptor and Flash Pro

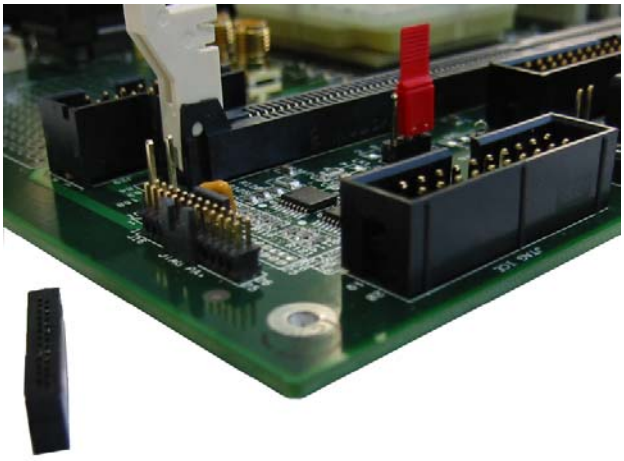


Figure 2 • Programming Header and Plug-In Header

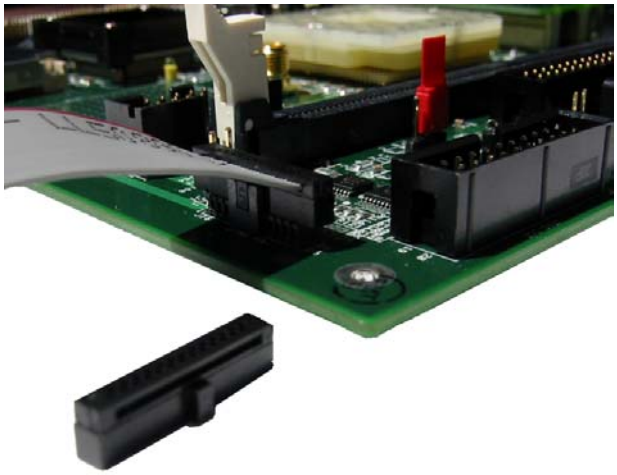
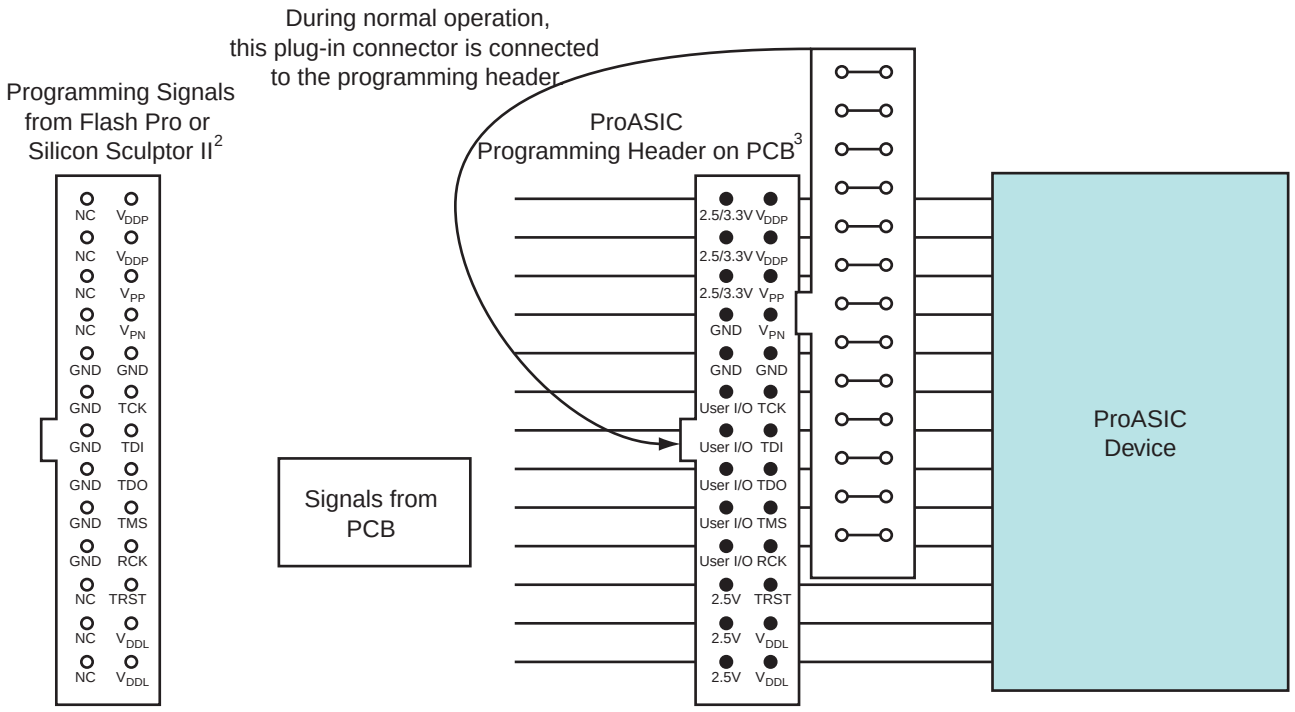


Figure 3 • Programming Cable on Header



Notes:

1. *For Flash Pro, use TCK. For Silicon Sculptor, use both RCK and TCK.*
2. *This is the output of the programmer. This diagram shows the signals that the programmer will drive onto the header in programming mode.*
3. *This is the pinout of the programming header on the PCB. The signals that appear on the header must be connected to the ProASIC device.*

Figure 4 • *ProASIC Programming Connectors and Header Top View*

ProASIC Programming Setup with Silicon Sculptor and Flash Pro

Plug-in Header

During the programming of the ProASIC 500K device, the programmer will drive V_{DDP} to 2.5V. If any other devices on the system drive a 3.3V signal to any I/O of the ProASIC 500K device, it will cause the I/O to latch up. Actel recommends shutting down the system during the programming of the ProASIC 500K device.

Also during programming, the programmer will be controlling all the power supplies (V_{DDL}, V_{DDP}, V_{PP}, V_{PN}) of the ProASIC 500K device. Note: We do not want the programmer to control the PCB board power supplies. To prevent this from happening, Actel recommends connecting the board power supplies to the left side of the programming header, the programmer connections to the right side of the programming header, thereby separating the power to the ProASIC device from the rest of the PCB. After successful programming, a plug-in header is put onto the programming header, allowing power from the PCB board to reach the ProASIC device (Figure 4).

Programming Pins

ProASIC 500K devices use the JTAG pins TCK, TMS, TDI, and TDO for programming. The TRST pin, an optional JTAG pin, is not used during programming.

TCK vs. RCK

The TCK pin is required during JTAG instruction shifting. During programming, the device needs a set-frequency, free-running clock to determine the length of the programming pulse. This clock can either be fed in through the TCK pin or RCK pin of the device. If TCK is used, then the clock must be controllable during the JTAG instruction shifting phase and free running during the programming pulse phase. If TCK is not guaranteed, then RCK must be used. Since RCK is not used during the JTAG instruction shifting phase, it could be free running at all times. The ProASIC 500K device simply ignores the RCK during all other operations.

For Silicon Sculptor, both TCK and RCK are used. This requires both TCK and RCK to be connected to the programming header.

For Flash Pro, only TCK is used, so only TCK needs to be connected to the programming header.

During normal operation, the TMS, TDI, TCK, and TDO are dedicated ports for the JTAG TAP controller inside the FPGA. They may be left floating in this mode as internal pull-up resistors are present on TMS and TDI, and TDO is an output. For more information, please refer to Actel's *Using JTAG with ProASIC 500K Devices* application note.

Power Supply Configurations

Normal Operation

The ProASIC device requires V_{DDL} and V_{DDP} to be connected. V_{DDL} is used to power the core and V_{DDP} powers the I/O pads. V_{DDL} must be set to 2.5V, and V_{DDP} can be set to either 2.5V or 3.3V (Table 1).

Table 1 • *Normal Operation*

Power Supply	ProASIC Voltage
V_{DDL}	2.5V
V_{DDP}	2.3V to 2.7V or 3.3V to 3.6V*
V_{PP}	V_{DDP}
V_{PN}	0V

Note: **Stresses beyond the maximum voltages listed in the table may causes permanent damage to the device. Devices should not be operated outside the Recommended Operating Conditions.*

Programming

For ProASIC devices, V_{DDP} supplies the programming circuit with power during programming. In addition to the low voltage power supplies (V_{DDL} and V_{DDP}), two high voltage sources (V_{PP} and V_{PN}) are necessary (Table 2).

Table 2 • *Programming Mode*

Power Supply	ProASIC Voltage
V_{DDL}	0V
V_{DDP}	2.5V
V_{PP}	16.5V
V_{PN}	–12V

For ProASIC, the typical current consumption for each programming pin during programming is as follows:

- $I_{VPP} < 35\ mA @ V_{PP} = +16.5V$
- $I_{VPN} < 15\ mA @ V_{PN} = -12V$
- $I_{VDDP} < 20\ mA @ V_{DDP} = +2.5V$
- $I_{VDDL} = 0\ mA @ V_{DDL} = +0V$

Power Supply Considerations

During ISP

All I/O pins except for JTAG interface pins are tristated and pulled up to V_{DDP} during programming. This isolates the part and prevents the signals from floating.

For ProASIC only, Actel recommends powering down the board during programming. Since V_{DDP} for ProASIC 500K must be 2.5V during programming, the tristated I/Os must not be driven by 3.3V signals. If this occurs, the pads will latch-up and a high current will flow through the pad cell, which can damage the device.

Interruptions in the programming sequence may result in unpredictable behavior of a partially programmed device. Additionally, switches that are programmed incorrectly can cause high current flow through the circuitry, resulting in permanent damage to the device.

ProASIC^{PLUS} Programming Setup with Silicon Sculptor and Flash Pro

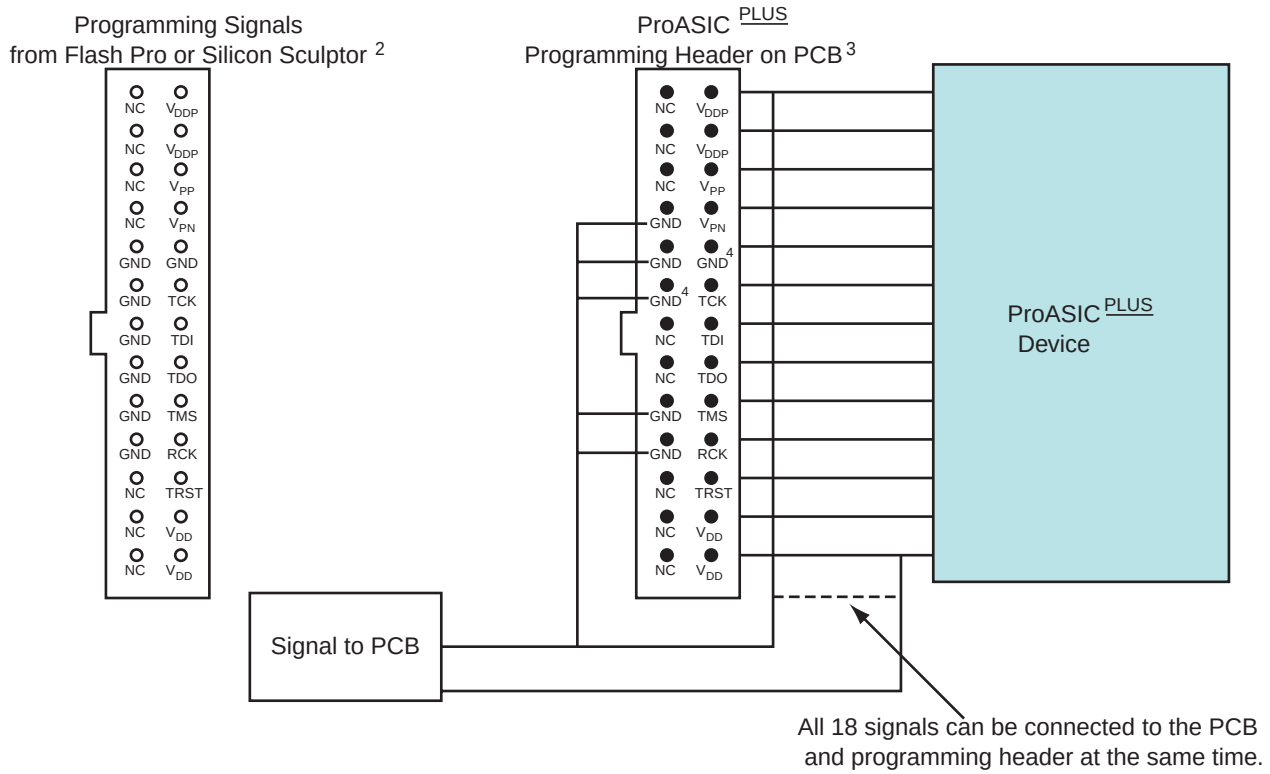
No plug-in connector is needed for ProASIC^{PLUS}. V_{DD}, V_{DDP}, V_{PP}, and V_{PN} only need to be connected to the programming header, if they are not supplied by the board during programming. The programmer will supply the necessary voltages during programming. GND, TCK, TDI, TDO, and TMS must be connected to the header. RCK is optional (Figure 5).

ProASIC^{PLUS} devices also use the JTAG (IEEE Standard 1149.1 1990) pins TCK, TMS, TDI, and TDO for programming. The TRST pin, an optional JTAG pin, is not used during programming, but it must remain high during programming. For Silicon Sculptor, the RCK pin is also required during programming; it is not required for Flash Pro.

Power Supply Configurations

Normal Operation

Two power supplies, one for the V_{DD} pins and a second for the V_{DDP} pins, are needed in normal operation. V_{DD} is used to power the core, and V_{DDP} powers the I/O pads. V_{DD} must be set to 2.5V, and V_{DDP} can be set to either 2.5V or 3.3V (Table 3 on page 5).



Notes:

1. *For Flash Pro, use TCK, and for Silicon Sculptor use both RCK and TCK.*
2. *This is the output of the programmer. This diagram shows the signals that the programmer will drive onto the header in programming mode.*
3. *This is the pinout of the programming header on the PCB. The signals that appears on the header must be connected to the ProASIC device.*
4. *GND pins 10 and 11 are the minimum number of pins required. Having the remaining GNDs will reduce noise.*

Figure 5 • *ProASIC^{PLUS} Programming Connectors and Header Top View*

Table 3 • Normal Operation

Power Supply	ProASIC^{PLUS} Voltage
V_{DD}	2.5V
V_{DDP}	2.3V to 2.7V or 3.0V to 3.6V[1]
V_{PP}	0V to 16.5V or floating[2]
V_{PN}	–13.8V to 0V or floating[3]

Note:

1. *Stresses beyond the maximum voltages listed in the table may causes permanent damage to the device. Devices should not be operated outside the Recommended Operating Conditions.*
2. *There is a nominal 40kΩ pull-up resistor on V_{PP}.*
3. *There is a nominal 40kΩ pull-down resistor on V_{PN}.*

Programming

For ProASIC^{PLUS} devices, both V_{DDP} and V_{DD} supply power to the programming circuit. In addition to the low voltage power supplies (V_{DD} and V_{DDP}), two high voltage sources (V_{PP} and V_{PN}) are necessary (Table 4).

Table 4 • Programming Mode

Power Supply	ProASIC^{PLUS} Voltage
V_{DD}	2.3V to 2.7V
V_{DDP}	2.3V to 2.7V or 3.0V to 3.6V
V_{PP}	15.9V to 16.5V
V_{PN}	–13.8V to –13.4V

The typical current consumption for each programming pin during programming is as follows:

- I_{VPP} < 35 mA @ V_{PP} = + 16.5V
- I_{VPN} < 15 mA @ V_{PN} = –13.8V
- I_{VDDP} < 20 mA @ V_{DDP} = + 3.6V
- I_{VDD} < 20 mA @ V_{DD} = + 2.7V

Power Supply Considerations

During ISP

All I/O pins, except for JTAG interface pins, are tristated and pulled up to V_{DDP} during programming. This isolates the part and prevents the signals from floating.

Interrupting the ISP Sequence

Interruptions in the programming sequence may result in unpredictable behavior of a partially programmed device. Additionally, switches that are programmed incorrectly can cause high current flow through the circuitry, resulting in permanent damage to the device.

Board Consideration

Actel REQUIRES bypass capacitors from V_{PP} to GND and V_{PN} to GND for all ProASIC^{PLUS} devices during programming. These bypass capacitors protect the ProASIC^{PLUS} devices from voltage spikes that occur on the V_{PP} and V_{PN} power supplies during the erase cycle. Two bypass capacitors are required for each supply. One of the bypass capacitors is a 4.7µF (low ESR, <1 Ω, tantalum, 25V or greater rating). The other bypass capacitor is a 0.01µF or 0.1µF ceramic capacitor with a 25V or greater rating (Figure 6). This is also recommended, but not required, for ProASIC. The bypass capacitors must be placed within 2.5cm of the device pins.

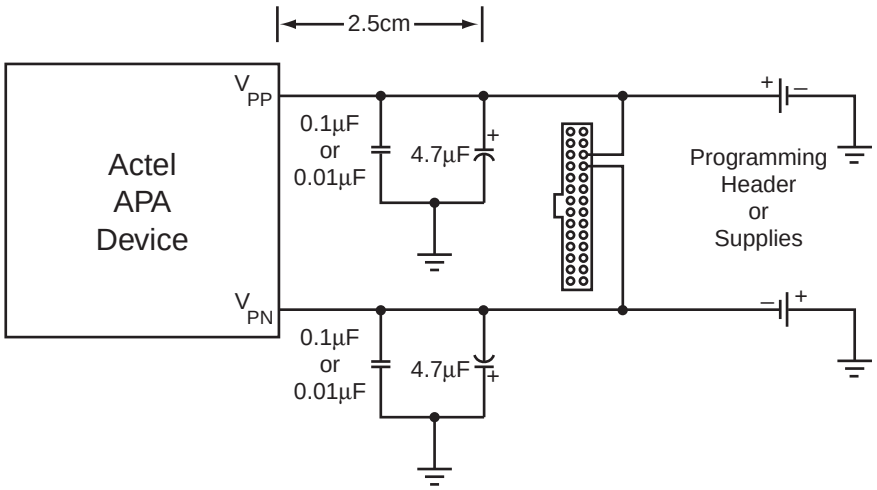


Figure 6 • V_{PP} and V_{PN} Capacitor Requirements

General Information

Actel recommends checking the device ID on the ISP board design before programming a device. This is done by reading the device ID from the device using Silicon Sculptor II or Flash Pro. If there is a problem, the programmer will fail with a "bad IDCODE" error message. If the reason for the failure cannot be found in the connection with the circuitry or the programming voltages, it is possible that the failure was caused by noise on the TCK or RCK signals. It is important to take all noise precautions into account for the TCK and RCK signals. Before programming a device, check the following:

For ProASIC only:

- Make sure all signals driving the device are 2.5V; it is recommended that the board is powered down during this stage.

For ProASIC^{PLUS} only:

- Make sure that the "1" level of all signals driving the device is within ±0.8V of V_{DDP}.
- Make sure that all ESD protection measures are taken.
- Make sure only ProASIC and ProASIC^{PLUS} parts are connected to the switching voltage supplies.
- Make sure not to interrupt the programming.

Programmer Part Number

Silicon Sculptor:	Silicon-Sculptor II
ISP Module:	SMPA-ISP-ACTEL-2
Flash Pro:	Flash Pro

	Programming Header	Plug-in Header
ProASIC^{PLUS}	Vendor: Samtec Part #: FTSH-113-01-L-D-K	N/A
	Vendor: 3M Part #: 3429-6502 For 0.062" board thickness	Vendor: Actel N/A
	Vendor: 3M Part #: 3429-6503 For 0.094-0.125" board thickness	Vendor: Actel N/A
ProASIC	Vendor: Samtec Part #: FTSH-113-01-L-D-K	Vendor: Actel N/A
	Vendor: 3M Part #: 3429-6502 For 0.062" board thickness	Vendor: Actel Part #: SMPA-ISP-HEADER
	Vendor: 3M Part #: 3429-6503 For 0.094-0.125" board thickness	Vendor: Actel Part #: SMPA-ISP-HEADER

Header Converter

Actel also provides a header converter (Actel Part Number: Header-Converter) to allow the Flash Pro programmer to be used with the older 100 mil spacing header. The header converter also provides an 8-pin connection from the programmer to the board, further reducing the board space required to perform ISP. (Figure 7).

For more information concerning Programming with ProASIC and ProASIC^{PLUS}, please refer to the following documents:

IEEE 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

Designer User's Guide

Silicon Sculptor User's Guide

Flash Pro User's Guide

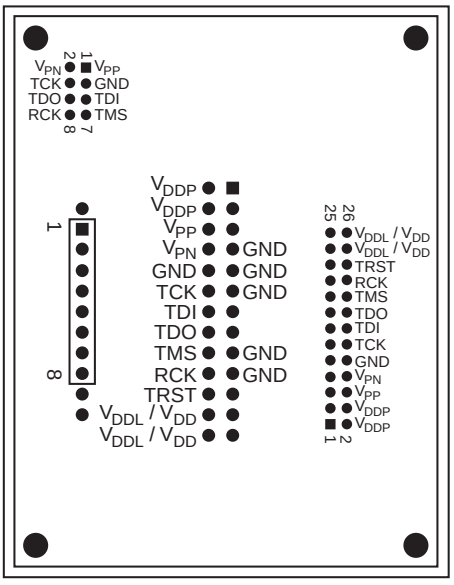


Figure 7 • *Head Converter Assembly*

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