ProASIC™ 500K Family

Features and Benefits

- High Capacity
  - 98,000 to 1.1 Million System Gates
  - 14K to 138K Bit of Two-Port SRAM
  - 210 to 623 User I/Os
- Performance
  - Corner-to-Corner Delay < 4 ns (Typical)
  - Clock-to-Out < 7 ns
  - System Performance > 200MHz
- Low Power
  - Segmented Hierarchical Routing Structure
  - Small Efficient Logic Cells
  - Low-Power FLASH Switches
- High Performance Routing Hierarchy
  - Ultra Fast Local Network
  - Efficient Long Line Network
  - High Speed Bus Network
  - High Performance Global Network
- Nonvolatile and Reprogrammable FLASH Technology
  - Live at Power-Up
  - No Configuration Boot Device Required
  - Retains Programmed Design During Power-Down/ Power-Up Cycles
- I/O
  - Mixed 3.3/2.5 Volt Support
  - 3.3V, 33MHz PCI Compliance (PCI Revision 2.2)
  - Individually Selectable 3.3V or 2.5V I/Os and Slew Rate (25, 50, and 100 mA/nsec)
- Secure Programming
  - Security Bit Prevents Read Back of Programming Bit Stream
- Standard FPGA and ASIC Design Flow
  - Flexibility to Choose Vendor-Specific Front-End Tools
  - Provide Efficient Design Through Front-End Timing and Gate Optimization
- In-System Programming (ISP) with Silicon Sculptor
- Embedded Memory Generator for SRAMs and FIFOs
  - Ensures Optimal Memory Usage
  - Up to 133MHz Synchronous and Asynchronous Operation
- IEEE Std. 1149.1 (JTAG) Compliant
- Individual ProASIC Device ID
  - Control and Restrict IP Delivery to Individual ProASIC Device

ProASIC Product Profile

	A500K050	A500K130	A500K180	A500K270	A500K350	A500K440	A500K510
Maximum System Gates	98,000	287,000	369,000	473,000	638,000	956,000	1,100,000
Typical Gates	43,000	105,000	150,000	215,000	280,000	350,000	410,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Embedded RAM Bits	14K	46K	55K	65K	74K	124K	138K
Embedded RAM Blocks (256 X 9)	6	20	24	28	32	54	60
Logic Tiles	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Maximum User I/Os	210	312	368	446	496	570	623
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by Pin Count)							
PQFP	208	208	208	208			
PBGA	272	272, 456	456	456			
FBGA			580	580	580	580	580

General Description

The 0.25µ ProASIC 500K family combines the advantages of ASICs with the benefits of programmable devices through its nonvolatile FLASH technology. ProASIC 500K devices make it possible to create high-density systems using existing ASIC or FPGA design flows and tools, shortening time-to-production. ASIC migration is not necessary for any volume because the family offers cost effective reprogrammable solutions, ideal for applications in the networking, telecom, computer, and consumer markets.

The ProASIC 500K family offers seven devices with 98K to 1.1M system gates and includes up to 138K bits of embedded two-port memory. These memory blocks include hardwired decoders, I/O circuits, parity generation and detection circuits, FIFO flow generation logic, and timing and control circuits to minimize external logic gate count and complexity while maximizing flexibility and utility.

Ordering Information

A500K130 – 1 PQ 208

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- PP = Pre-production
- ES = Engineering Samples

Package Lead Count

Package Type
- BG = Ball Grid Array
- PQ = Plastic Quad Flat Pack

Speed Grade
- Blank = Standard Speed
- –1 = TBD

Part Number
- A500K050 = 98,000 Gates
- A500K130 = 287,000 Gates
- A500K180 = 369,000 Gates
- A500K270 = 473,000 Gates
- A500K350 = 638,000 Gates
- A500K440 = 956,000 Gates
- A500K510 = 1,100,000 Gates

Product Plan

	Speed Grade		Application	
	Std	–1*	C	I
A500K050 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
272-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
A500K130 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
272-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
A500K180 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K270 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✔	P	P	P
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K350 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K440 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K510 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P

Contact your Actel sales representative for package availability.

Applications: C = Commercial I = Industrial

Availability: ✔ = Limited Availability.Contact your Actel Sales representative for the latest availability information. P = Planned

**Speed Grade: –1 = TBD*

Plastic Device Resources

	User I/Os			
Device	**PQFP 208-Pin**	**PBGA 272-Pin**	**PBGA 456-Pin**	**FBGA 580-Pin**
A500K050	170	210	—	—
A500K130	170	210	312	—
A500K180	170	—	368	368
A500K270	170	—	368	446
A500K350	—	—	—	496
A500K440	—	—	—	496
A500K510	—	—	—	496

Package Definitions *(Contact your Actel sales representative for product availability.)*

PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Ball Grid Array

Pin Description

I/O **User Input/Output**

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output signal levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are configured as inputs with pull-up resistor.

N/C **No Connect**

To maintain compatibility with future Actel ProASIC products it is recommended that this pin not be connected to the circuitry on the board.

G_X **Global Input Pin**

Low skew input pin for clock or other global signals. Input only.

GND **Ground**

Common ground supply voltage.

V_{DDL} **Logic Array Power Supply Pin**

2.5V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5V or 3.3V supply voltage.

V_{PP} **Programming Supply Pin**

This pin must be connected to V_{DDP} during normal operation, or it can remain at 16.5V in an ISP application. This pin must not float.

V_{PN} **Programming Supply Pin**

This pin must be connected to GND during normal operation, or it can remain at –12V in an ISP application. This pin must not float.

TMS **Test Mode Select**

The TMS pin controls the use of JTAG circuitry.

TCK **Test Clock**

Clock input pin for JTAG.

TDI **Test Data In**

Serial input for JTAG.

TDO **Test Data Out**

Serial output for JTAG.

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

Process Technology

The ProASIC 500K family achieves its non-volatility and reprogrammability through an advanced 4LM FLASH-based 0.25µ channel length CMOS technology process. Standard CMOS design techniques are used to implement logic and control functions resulting in highly predictable performance and gate array compatibility. FLASH memory bits are distributed throughout each device providing non-volatile, reconfigurable interconnect programming.

ProASIC 500K Architecture

The ProASIC 500K family utilizes a proprietary architecture that results in granularity comparable to gate arrays. Unlike SRAM-based FPGAs, ProASIC devices do not utilize look-up tables or architectural mapping during design. Instead, designs are directly synthesized to gates that streamline the design flow, increase design productivity, and eliminate dependencies on vendor-specific design tools.

The ProASIC 500K device core consists of a Sea-of-Tiles™ (Figure 1). Each logic tile can be configured into a 3-input logic function (i.e. NAND gate, D-Flip-Flop, etc.) by programming the appropriate interconnect FLASH switches. Gates and larger functions are connected together in a similar manner utilizing the four levels of routing hierarchy. FLASH switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew clock distribution throughout the core. All core tiles are configurable as gates, muxes, latches, or flip-flops. Maximum core utilization is possible for virtually any design.

The ProASIC 500K devices also contain embedded two-port SRAM blocks that have built in FIFO control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity selection.

Routing Resources

The routing structure of the ProASIC 500K devices is designed to provide high performance through routing flexibility. It is composed of four levels of hierarchical resources: ultra fast local resources, efficient long line resources, high speed bus resources, and high performance global networks.

The ultra fast local resources are high speed dedicated lines that allow the output of each tile to directly connect to every input of the eight closest tiles (Figure 2).

The efficient long line resources provide routing for longer distance and higher fanout connections. These resources vary in length (typically spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC device (Figure 2). Each tile can drive signals onto the efficient long line resources, and the resources can access every input of a tile. Active buffers are inserted automatically by the ASICmaster software to limit the effects of loading due to distance and fanout.

The high speed bus resources span across the entire device with minimal delay and are used to route very long or very high fanout nets. These resources run vertically and

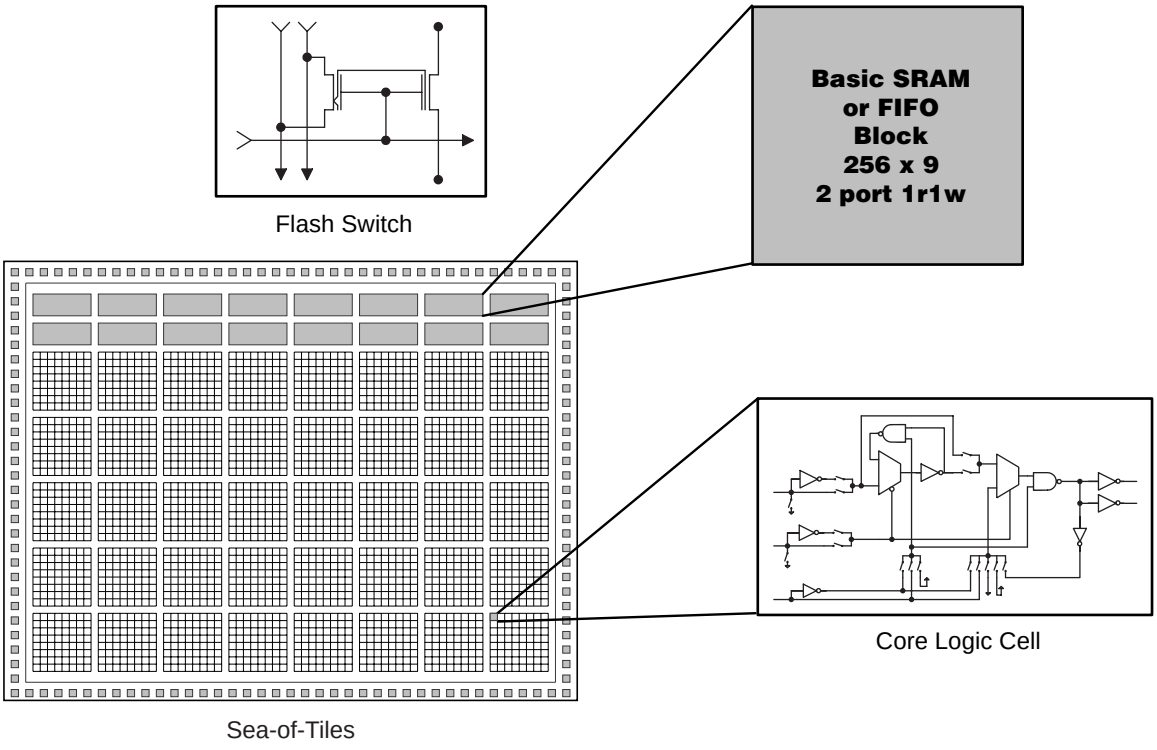


Figure 1 • *The ProASIC Device Architecture*

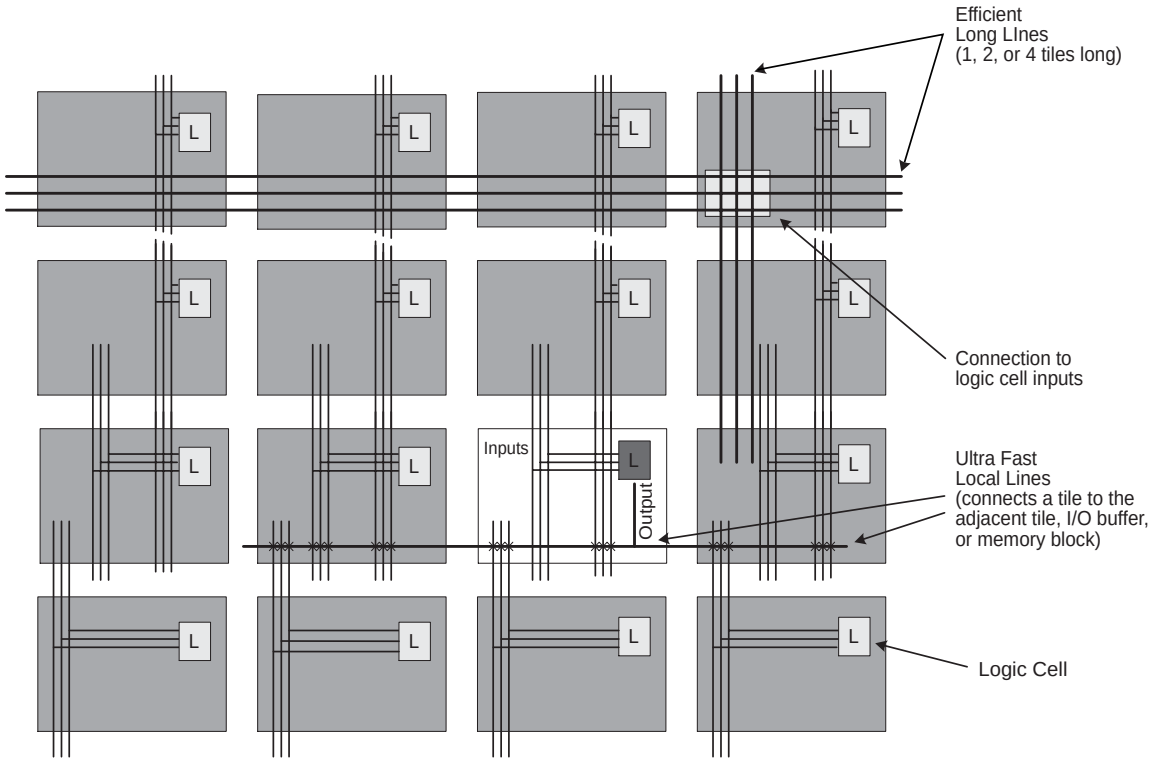


Figure 2 • *High Density Interconnect*

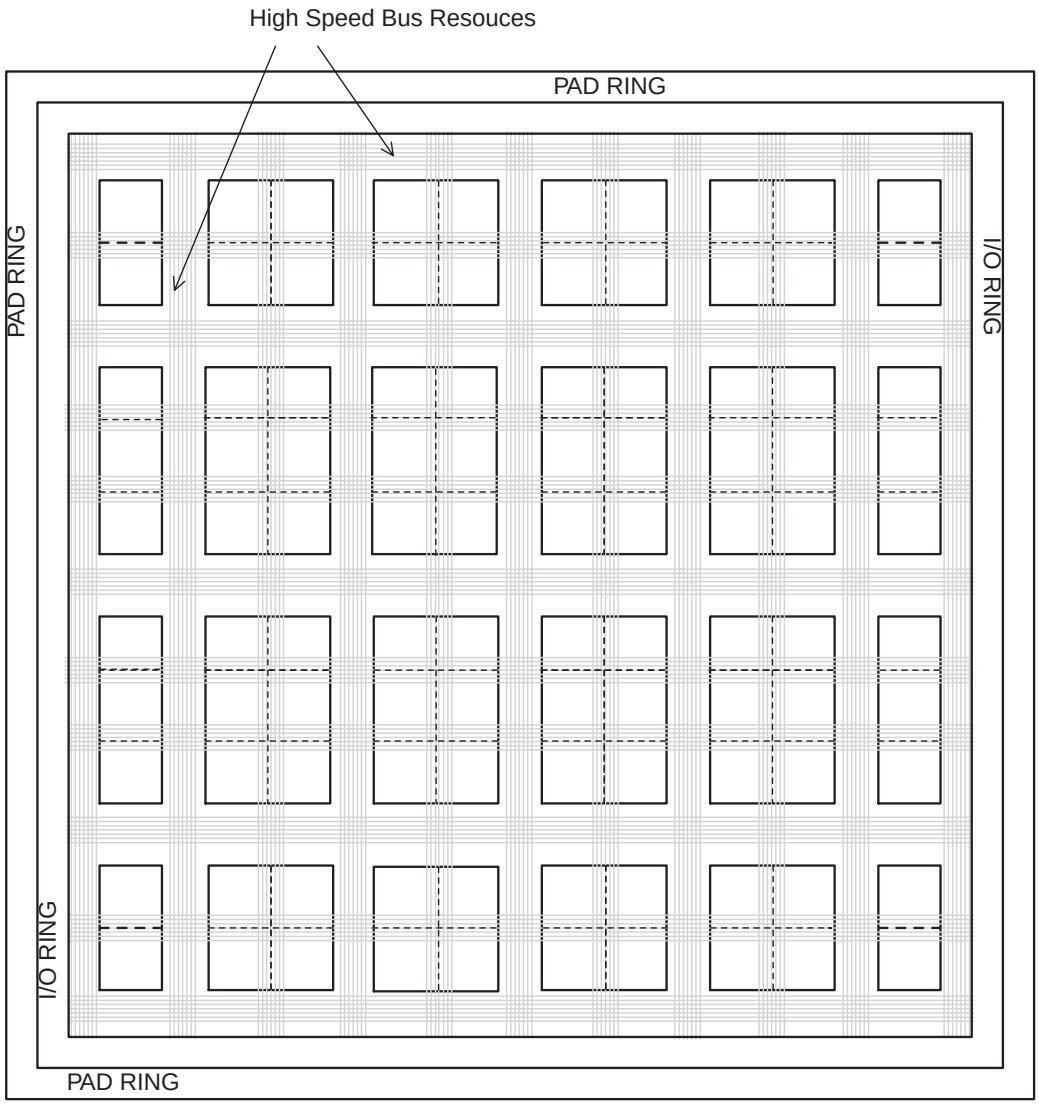


Figure 3 • *High Speed Bus Resources*

horizontally, and provide multiple access to each group of 16 tiles throughout the device (Figure 3).

The high performance global networks are low skew, high fanout nets that are accessible from four dedicated pins or from external logic (Figure 4). These nets are typically used to distribute clocks, resets, and other nets requiring high fanout with guaranteed minimum skew. The maximum delay on these nets is 3.5ns, and maximum skew is 250ps when these signals are used to drive clocks and resets on flip-flops. The global networks are implemented as four H trees, and signals can be introduced at any junction. These can be used hierarchically, with signals accessing every input on all tiles. Any portion of the global resources not required for the four primary global nets are made available to any other net requiring the distribution of high fanout signals.

Input/Output Blocks

To meet the needs of complex system designs, the ProASIC 500K family provides devices with a large number of I/O pins, with the A500K510 device offering up to 623 user I/O pins. The I/O pad is powered at 3.3V, which allows each I/O to be selectively configured at 2.5V and 3.3V compliant threshold levels. Figure 5 illustrates I/O interfaces with other devices. All I/Os also include an ESD protection circuit. Each I/O is tested according to the following models:

Human Body Model (HBM) (Per Mil Std 883 Method 3015)	1500V
Machine Model	200V

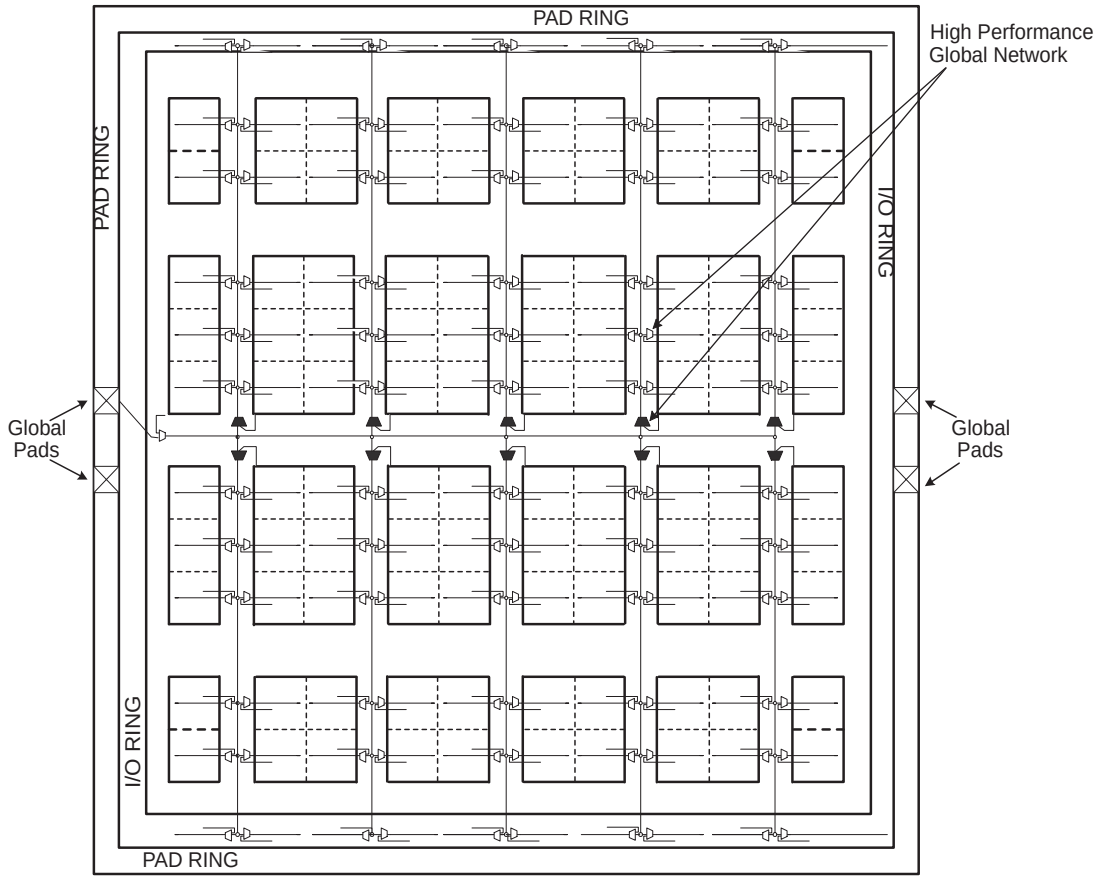


Figure 4 • *High Performance Global Network*

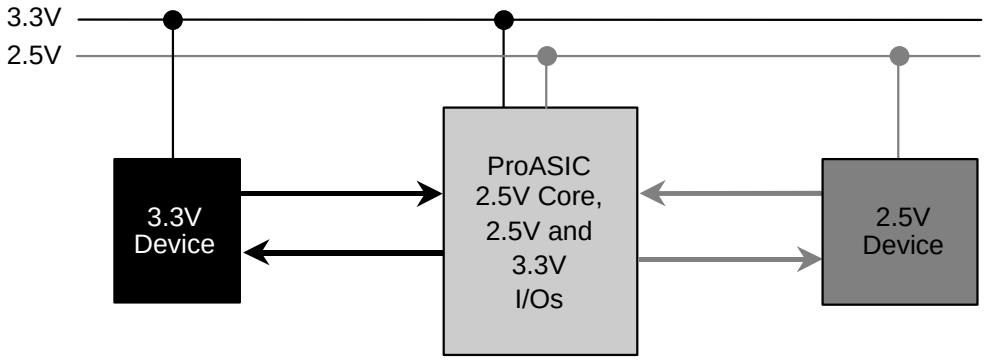


Figure 5 • *I/O Interfaces*

The I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a three-state driver, or a bi-directional buffer (Figure 6). I/O pads configured as inputs have the following features:

- Individually selectable 3.3V or 2.5V compliant threshold levels
- Optional pull-up resistor

I/O pads configured as output have the following features:

- Individually selectable 3.3V or 2.5V compliant output signals
- 3.3V PCI compliant
- Ability to drive TTL and CMOS levels
- Selectable drive strengths
- Selectable slew rates
- Three-state enable (drivable from any internal or external signal)

I/O pads configured as bi-directional have the following features:

- Individually selectable 3.3V or 2.5V compliant output signals and threshold levels
- 3.3V PCI compliant
- Ability to drive TTL level
- Optional pull-up resistor for inputs
- Selectable drive strengths
- Selectable slew rates
- Three-state enable

User Security and Traceability

The ProASIC 500K devices have a read-protect bit that, once programmed, prevents the programming content from being read from the part. To clear the read-protect bit, the entire part must be erased. This capability lets you secure the programmed design and prevent it from being read back and duplicated. For traceability a 12-character alphanumeric user part number field allows the user to assign a user part ID, which can subsequently be read back by the programmer.

Embedded Memory Floorplan

The embedded memory is located across the top of the device (see Figure 1). Depending upon the device, 6 to 60 (256x9) blocks of memory are available to support a variety of possible memory configurations. Each block can be programmed as an independent memory or combined, using dedicated memory routing resources, to form larger and more complex memories.

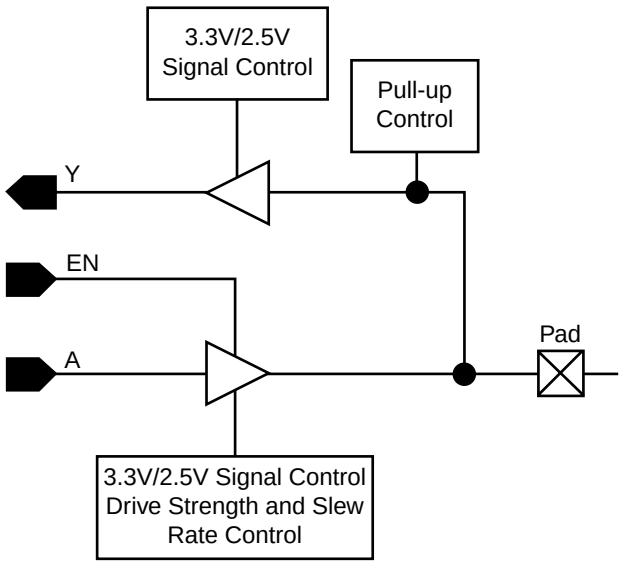


Figure 6 • I/O Block Schematic Representation

Embedded Memory Configurations

The embedded memory in the ProASIC 500K family offers great flexibility in memory configuration. Whereas other programmable vendors typically provide single port memories that can be transformed into a two-port memory at the loss of half the memory, each ProASIC block is designed and optimized as a two-port memory (1r1w). This provides 138K total memory bits for two-port and single port memory usage in the A500K510 device.

Each memory can be configured as a FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports. However, multiple writes are not supported. Additional characteristics include programmable FIFO flags and selectable depth, and parity check and generation. Figure 7 and Figure 8 show the block diagram of the basic SRAM and FIFO blocks. These memories are designed to operate at up to 133 MHz when operated individually. Each block contains a 256 word deep by 9-bit wide (1r, 1w) memory. The memory blocks shown in Figure 9 may be combined in parallel to form wider memories or stacked to form deeper memories. The MEMORYmaster™ software facilitates an easy means of building wider and deeper memories for optimal memory usage. This provides optimal bit widths of 9 (1 block), 18, 36, and 72. MEMORYmaster allows any bit width up to 252 (for the A500K270 device), but if an intermediate bit width is chosen, such as 16 bits, the remaining two bits are no longer accessible for other memories. MEMORYmaster also enables optimal memory stacking in 256 word increments. However, any word depth may be compiled for up to 7,168 words.

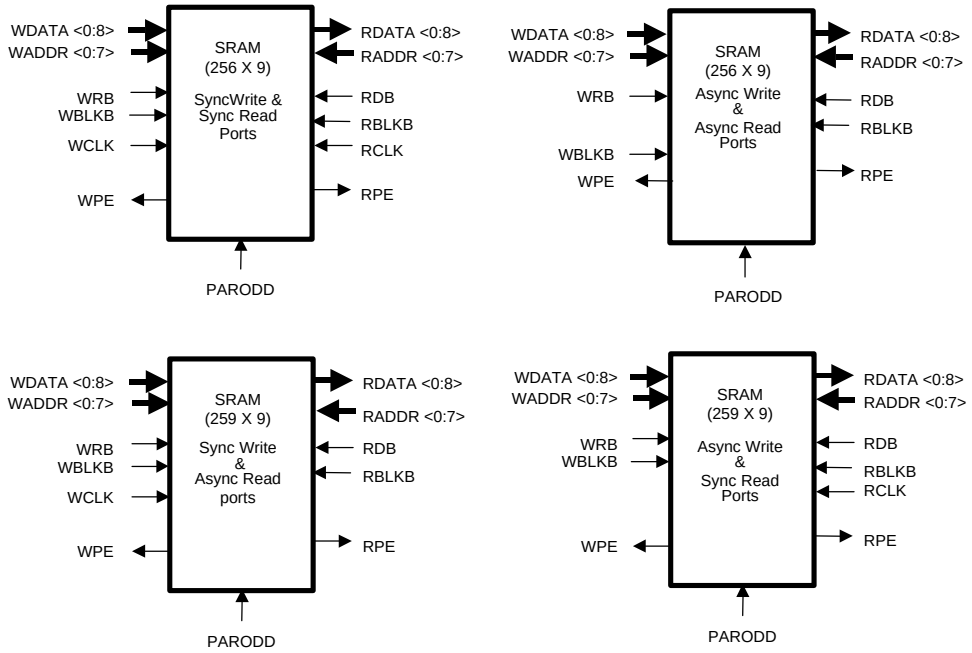


Figure 7 • Example SRAM Block Diagrams

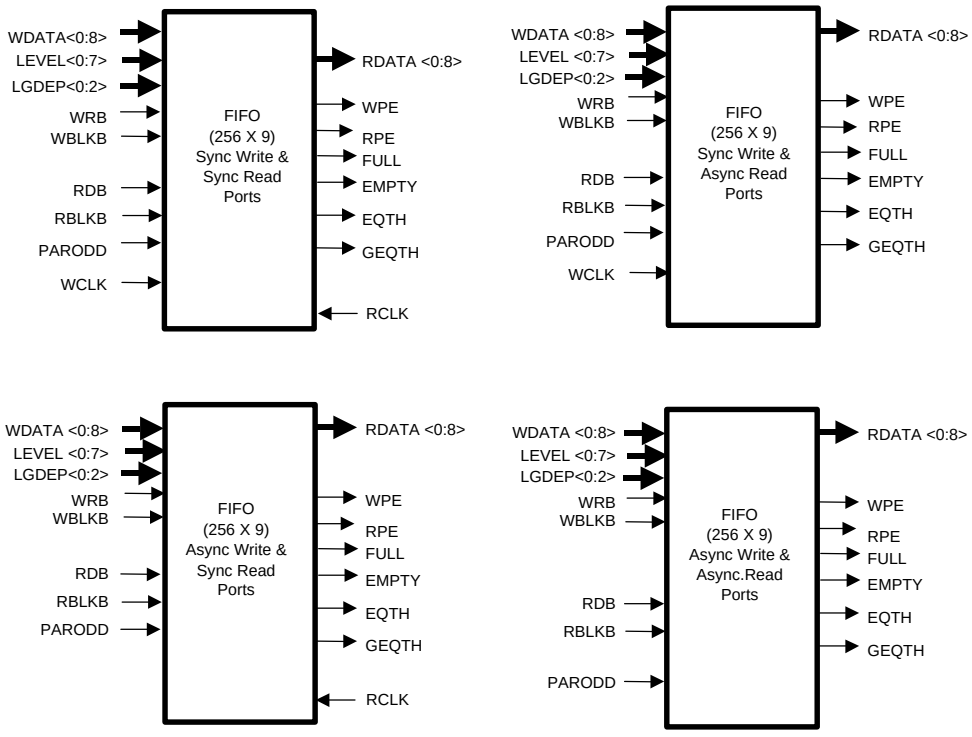


Figure 8 • Basic FIFO Block Diagrams

Figure 10 shows an example of optimal memory usage. Three memories have been compiled with various widths and depths using 10 blocks and consuming all 23,040 bits. Figure 11 shows an example of doubling up memory to create extra read ports. In this example, 10 out of 60 blocks of the A500K510 are fully used, but yield an effective 6,912 bits of multiple port memories.

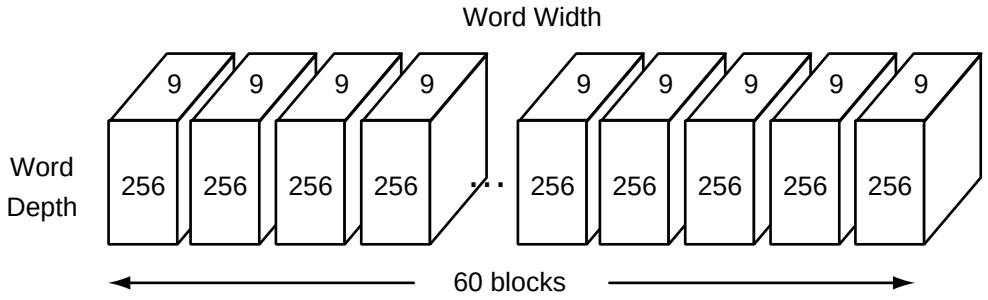


Figure 9 • *A500K510 Memory Block Architecture*

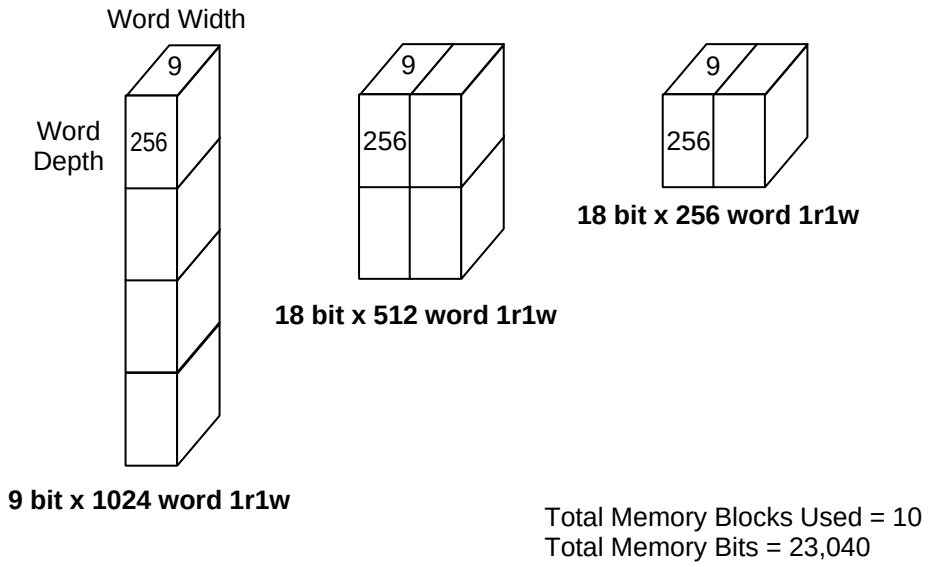


Figure 10 • *Memories with Different Width and Depth*

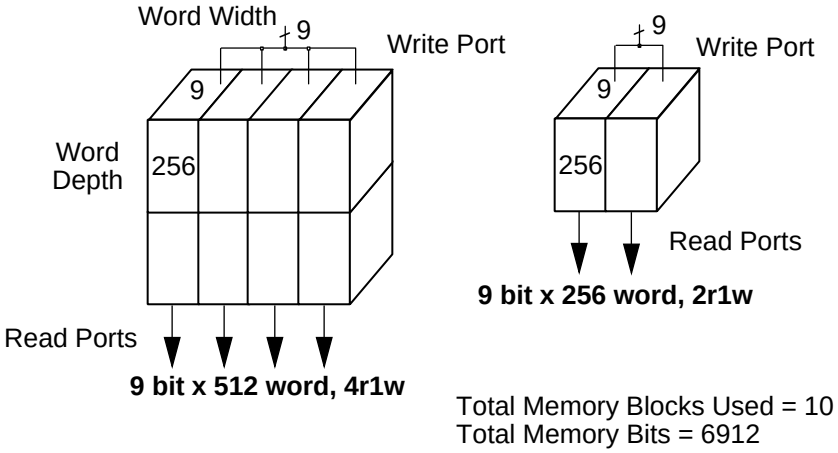


Figure 11 • *Multiport Memory Usage*

Design Environment

ProASIC devices are supported by Actel's ASICmaster and MEMORYmaster software, as well as third party CAE tools. Using the standard VHDL or Verilog HDL descriptions, no special HDL design techniques, required by some FPGA vendors, are needed. This allows designers to use the same code that is used for gate arrays and standard cells for ProASIC devices. The ProASIC design flow also ensures a seamless transition to an ASIC should production volumes warrant a migration to a gate array or a standard cell product. As shown in Figure 12, with identical HDL, design tools, and flow, migration to ASICs for high volume production is greatly simplified. Conversely, migration from ASICs to ProASIC technology is also free of traditional FPGA design requirements.

MEMORYmaster automatically generates memories from inputs given by the designer. The designer can select the depth and width, usage of parity generation or check, and synchronous or asynchronous functionality of the ports. If it is a synchronous read port, the designer can choose whether the output is pipelined or transparent.

Synthesis and simulation is performed by third party CAE tools. ProASIC is currently supported by Synopsys Design Compiler, Prime Time, and VSS, Cadence BuildGates and Verilog-XL, Exemplar Spectrum, and Model Technology ModelSim. Actel's ProASIC libraries and timing models provide the database required for simulation.

Place and route is performed by Actel's ASICmaster software. Available for SunOS, Solaris, HP, and Windows NT, it accepts standard ASIC formatted netlists, performs place and route of the design into the selected device and provides post layout delay information for back annotation simulation or static timing analysis. The ASICmaster software also contains very powerful interactive layout capabilities for the experienced user.

Once the design is finalized, the programming bitstream is downloaded into the device programmer for ProASIC part programming. ProASIC 500K devices can be programmed with the Silicon Sculptor programmer. In-System Programming is available using the Silicon Sculptor programmer and an In-System Programming header.

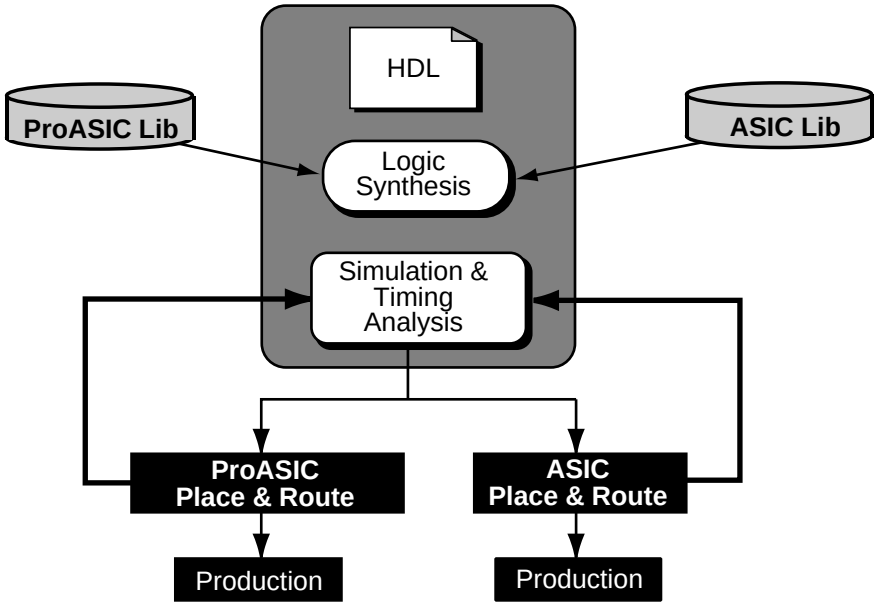


Figure 12 • *Common Design Environment*

Package Thermal Characteristics

The ProASIC 500K family is available in a number of package types. Packages are selected based on high pin count, reliability factors, and superior thermal characteristics.

The ability of a package to conduct heat away from the silicon, through the package to the surrounding air is expressed in terms of thermal resistance. This junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta JA (Θ_{JA}). The lower this thermal resistance, the easier it is for the package to dissipate heat.

The maximum allowed power (P) for a package is a function of the maximum junction temperature (T_J), the maximum ambient operating temperature (T_A), and the junction-to-ambient thermal resistance Θ_{JA}. Maximum junction temperature is the maximum temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{JA}}$$

Θ_{JA} is a function of the rate of airflow in contact with the package, in linear feet per minute (lfpm). When the estimated power consumption exceeds the maximum allowed power, other means of cooling must be used, such as increasing the airflow rate.

The junction-to-case thermal resistance, Theta JC (Θ_{JC}), is the lowest possible thermal resistance of the device. Θ_{JC} is defined as:

$$\Theta = \Theta_{JC} + \Theta_{CA}$$

where

Θ_{CA} = case to ambient thermal resistance

Package Type	Pin Count	Θ_{JC}	Θ_{JA} Still Air	Θ_{JA} 300 ft/min	Units
Plastic Quad Flat Pack (PQFP)	208	3.5	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	16.5	°C/W
Plastic Ball Grid Array (PBGA)	456	3	16.5	14.5	°C/W

Calculating Power Dissipation

ProASIC device power is calculated in the same manner as CMOS gate arrays and includes both a static and an active component. The active component is a function of both the number of tiles utilized and the speed. ASICmaster provides an automatic power calculator that can be used to quickly and easily calculate power dissipation. Power dissipation can also be calculated using the following formula:

$$P = V_{DD} \bullet I_{DD}$$

where

$$I_{DD} = I_{STATIC} + I_{OUTPUT} + I_{LOGIC}$$

and

$$I_{STATIC} = I_{STATIC\ CORE} + I_{STATIC\ I/O}$$

I_{OUTPUT} is the current due to the outputs switching.

I_{LOGIC} is the current due to the internal logic signals switching.

The static power (I_{STATIC}) is the amount of current drawn when no inputs are switching. This is equal to the Quiescent Supply Current I_{DDQ} specified under DC Characteristics.

Active power includes both the current due to outputs switching and the current due to internal logic signals switching.

$$I_{OUTPUT} = \sum_{i=1}^{n} (C_i \cdot V_i \cdot f_i + I_{DCi})$$

where

C_i is the capacitance on the i th output pad.

V_i is the voltage swing on the i th output pad.

f_i is the switching frequency on the i th output pad.

n is the number of outputs.

I_{DCi} is the average DC load on each pad, if any.

In most cases I_{OUTPUT} can be approximated by the following formula, measured in mA:

$$I_{OUTPUT} = n \bullet C_{typ} \bullet V \bullet f_{avg}$$

where

n is the number of active outputs.

C_{typ} is the typical capacitance load on an output.

V is the average voltage swing.

f_{avg} is the average switching frequency of the outputs. Typically this is less than 25% of the clock frequency.

I_{LOGIC} is represented by this formula, measured in mA:

$$I_{LOGIC} = I_E \bullet G \bullet f \bullet F$$

where

I_E is the effective µA per gate per MHz of the Actel parts. For the ProASIC products the value is 1.2.

G is the number of gates used in the design, in thousands.

f is the operating frequency in MHz.

F is the fraction of devices active on each clock edge. F varies for different designs, but 0.15 is a conservative and commonly used value.

For a A500K130 design that has 47,000 used gates, 20 memory blocks, 150 active outputs, an average load of 20 pF, and a 66 MHz clock, resulting in an average switching frequency of 16.5 MHz, the power calculation appears below.

I_{OUTPUT} $= 150 \bullet 20 \bullet 10^{-12} \bullet 3.6 \bullet 16.5 \bullet 10^{6}$mA

$= 140$mA

P_{OUTPUT} $= 3.6V \bullet 140mA = .5W$

I_{LOGIC} $= 1.2 \bullet 47 \bullet 66 \bullet 0.15$mA

$= 558$mA

Therefore

I_{LOGIC} $= 558$mA

P_{Logic} $= 2.75V \bullet 558mA$

$= 1.5$ W

Assumptions .5K gates per 256x9 block

I_{memory} $= 1.2 \bullet .5 \bullet 66 \bullet .15 \bullet 20$mA

$= 118$mA

P_{memory} $= 2.75V \bullet 143mA = .326$

P $= 1.5W + .5W + .32W = 2.32W$

$I_{STATIC\ CORE}$ and $I_{STATIC\ I/O}$ are not included in this calculation.

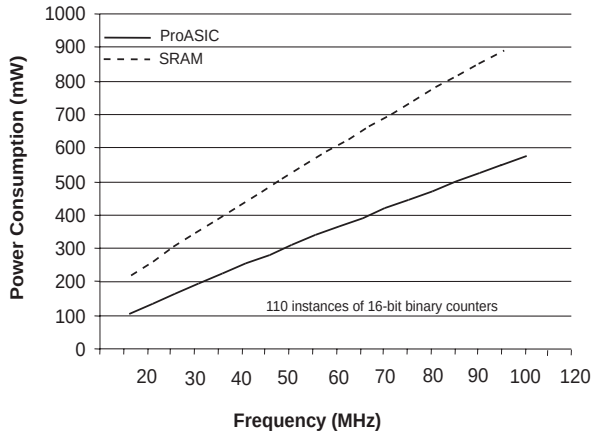


Figure 13 • *Power Consumption of a 500K Device*

Operating Conditions

Absolute Maximum Ratings

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DDL})		–0.3	3.0	V
Supply Voltage IO Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–0.5	V_{DDP} + 0.5	V
DC Input Clamp Current (IIK)	V_{IN} < 0 or > V_{DD}	–10	+10	mA

Note: *Stresses beyond those listed under Absolute Maximum ratings can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can adversely affect device reliability. Operation of the device at these conditions or any others beyond those listed under Recommended Operating Conditions shown in the table below is not implied.*

Temperature Maximums

Parameter	Min.	Max.	Units	Program Retention
Storage Temperature	–65	+150	°C	NA
Storage Temperature—Programmed	–65	+110	°C	20 years

Programming Limits and Recommended Operating Conditions

Product Grade	Programming Cycles	Program Retention	Junction Temperature	
			Min.	Max.
Commercial	500	20 years	0°C	110°C
Industrial	500	20 years	–40°C	110°C

Supply Voltages

V_{DDL}	V_{DDP}	V_{PP}	V_{PN}
2.5V	2.5V	2.5V ≤ V_{PP} ≤ 16.5 V	–12V ≤ V_{PN} ≤ 0V
2.5V	3.3V	2.5V ≤ V_{PP} ≤ 16.5V	–12V ≤ V_{PN} ≤ 0V

Recommended Operating Conditions

Parameter	Symbol	Limits
Commercial		
DC Supply Voltage (2.5V I/Os)	V_{DDL} & V_{DDP}	2.30V to 2.70V
DC Supply Voltage (3.3V I/Os)	V_{DDP}	3.0V to 3.6V
Operation Ambient Temperature Range	T_A	0°C to 70°C
Operation Junction Temperature (maximum)	T_J	≤ 110°C
Industrial		
DC Supply Voltage (2.5V I/Os)	V_{DDL} & V_{DDP}	2.30V to 2.70V
DC Supply Voltage (3.3V I/Os)	V_{DDP}	3.0V to 3.6V
Operation Ambient Temperature Range	T_A	–40°C to 85°C
Operation Junction Temperature (maximum)	T_J	≤ 110°C

DC Electrical Specifications (V_{DDP} = 2.5V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP}, V_{DDL}	Supply Voltage		2.30		2.7	V
V_{OH}	Output High Voltage					
	High Drive	I_{OH} = –2.0 mA	2.1			V
		I_{OH} = –4.0 mA	2.0			
		I_{OH} = –8.0 mA	1.7			
	Low Drive	I_{OH} = –1.0 mA	2.1			
		I_{OH} = –2.0 mA	2.0			
		I_{OH} = –4.0 mA	1.7			
V_{OL}	Output Low Voltage					
	High Drive	I_{OL} = 5.0 mA			0.2	V
		I_{OL} = 10.0 mA			0.4	
		I_{OL} = 15.0 mA			0.7	
	Low Drive	I_{OL} = 2.0 mA			0.2	
		I_{OL} = 3.5 mA			0.4	
		I_{OL} = 5.0 mA			0.7	
V_{IH}	Input High Voltage		1.7		V_{DDP} +.03	V
V_{IL}	Input Low Voltage		–0.3		.7	V
V_T	Switching Threshold			1.20		V
I_{IN}	Input Current (with pull-up)		–20		–100	µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{SS}* or V_{DDL}		1.0	10	mA
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DDL}	–10		+10	µA
I_{OSH}	Output Short Circuit Current High					
	High Drive				–120	mA
	Low Drive				–100	
I_{OSL}	Output Short Circuit Current Low					
	High Drive				100	mA
	Low Drive				30	
$C_{I/O}$	I/O pad capacitance				8	pF
C_{CLK}	Clock input pad capacitance				8	pF

Notes: *All process conditions. Junction Temperature: –40 to +110°C.*
** No pull-up resistor.*

DC Electrical Specifications (V_{DDP} = 3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP}	Supply Voltage		3.0		3.6	V
V_{DDL}	Supply Voltage, Logic Array		2.3		2.7	V
V_{OH}	Output High Voltage					V
	3.3V I/O, High Drive	I_{OH} = –3.0 mA I_{OH} = –5.0 mA I_{OH} = –10.0 mA	V_{DDP} – 0.2 0.9 * V_{DDP} 2.4			
	3.3V I/O, Low Drive	I_{OH} = –2.0 mA I_{OH} = –3.0 mA I_{OH} = –6.0 mA	V_{DDP} – 0.2 0.9 * V_{DDP} 2.4			
	2.5V I/O, High Drive	I_{OH} = –0.5 mA I_{OH} = –1.0 mA I_{OH} = –2.0 mA	2.1 2.0 1.7			
	2.5V I/O, Low Drive	I_{OH} = –0.5 mA I_{OH} = –1.0 mA I_{OH} = –2.0 mA	2.1 2.0 1.7			
V_{OL}	Output Low Voltage					V
	3.3V I/O, High Drive	I_{OL} = 7.5 mA I_{OL} = 12.0 mA I_{OL} = 15.0 mA			0.2 0.1 * V_{DDP} 0.4	
	3.3V I/O, Low Drive	I_{OL} = 2.5 mA I_{OL} = 4.0 mA I_{OL} = 5.0 mA			0.2 0.1 * V_{DDP} 0.4	
	2.5V I/O, High Drive	I_{OL} = 7.5 mA I_{OL} = 15.0 mA I_{OL} = 24.0 mA			0.2 0.4 0.7	
	2.5V I/O, Low Drive	I_{OL} = 2.5 mA I_{OL} = 5.0 mA I_{OL} = 8.0 mA			0.2 0.4 0.7	
V_{IH}	Input High Voltage					V
	TTL		2		V_{DD} + .3	
	LV-CMOS		0.7 * V_{DDP}			
	2.5V Mode		1.7			
V_{IL}	Input Low Voltage					V
	TTL				0.8	
	LV-CMOS		–0.3		0.3 * V_{DDP}	
	2.5V Mode				0.7	
V_T	Switching Threshold	TTL LV-CMOS 2.5V Mode		1.5 0.5 * V_{DDP} 1.2		V
I_{IN}	Input Current					
	CMOS & TTL (with pull-up)		–40		–200	µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{SS}* or V_{DD}		1.0	10	mA

Notes: *Refer to PCI Specifications Revision 2.2. for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads.*
** No pull-up resistor.*

DC Electrical Specifications (V_{DDP} = 3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{OZ}	3-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	–10		+10	µA
I_{OSH}	Output Short Circuit Current High 3.3V I/O, High Drive 3.3V I/O, Low Drive 2.5V I/O, High Drive 2.5V I/O, Low Drive				 –200 –140 –100 –100	mA
I_{OSL}	Output Short Circuit Current Low 3.3V I/O, High Drive 3.3V I/O, Low Drive 2.5V I/O, High Drive 2.5V I/O, Low Drive				 160 50 160 50	mA
$C_{I/O}$	I/O pad capacitance				8	pF
C_{CLK}	Clock input pad capacitance				8	pF

Notes: *Refer to PCI Specifications Revision 2.2. for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads.*
** No pull-up resistor.*

Timing Characteristics

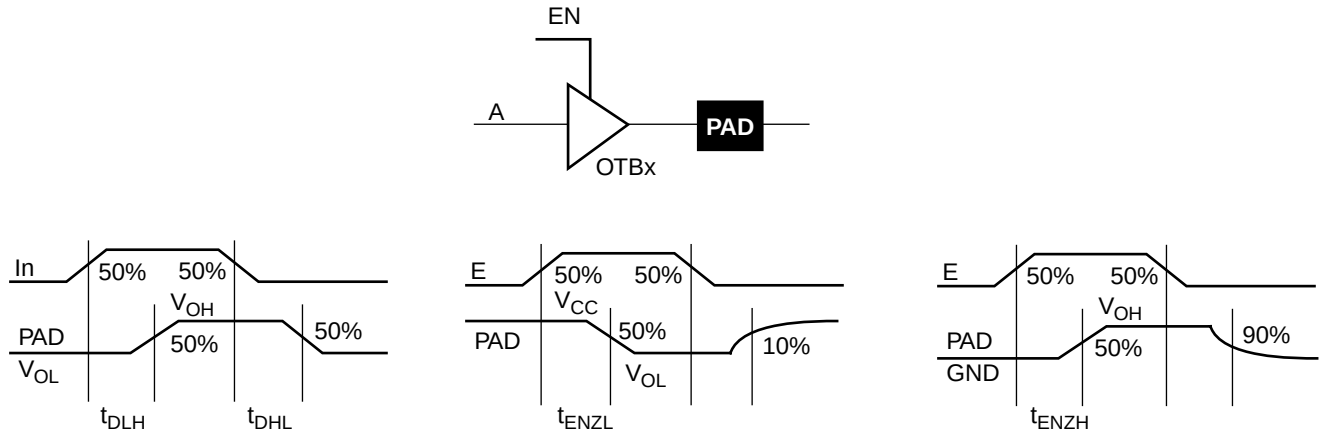


Figure 14 • *Tristate Buffer Delays*

Table 1 • *Tristate Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, 35pF load, T_J = 70°C)*

Macro Type	Description	Max. t_{DLH}	Max. t_{DHL}	Max. t_{ENZH}	Max. t_{ENZL}	Units
OTB33PH	3.3V, PCI Output Current, High Slew Rate	4.20	4.47	4.23	3.85	ns
OTB33PN	3.3V, PCI Output Current, Nominal Slew Rate	5.22	6.96	5.28	6.27	ns
OTB33PL	3.3V, PCI Output Current, Low Slew Rate	6.30	8.61	6.37	7.93	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	6.26	6.76	6.33	5.94	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	7.70	10.80	7.78	10.38	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	9.18	14.15	9.26	13.78	ns
OTB25HH	2.5V, High Output Current, High Slew Rate	7.65	3.95	7.70	3.62	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate	8.77	6.24	8.85	5.87	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate	10.34	7.74	10.42	7.32	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate	13.43	5.71	13.46	5.30	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate	14.74	9.73	14.81	9.39	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate	16.17	12.86	16.23	12.51	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.40	6.02	5.43	5.21	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	7.15	9.99	7.20	9.34	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	8.83	12.82	8.87	12.24	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	8.30	9.28	8.35	8.24	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	10.44	15.38	10.49	14.92	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	12.62	20.63	12.66	20.18	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*
3. *t_{ENZH} = Enable-to-Pad, Z to HIGH*
4. *t_{ENZL} = Enable-to-Pad, Z to LOW*

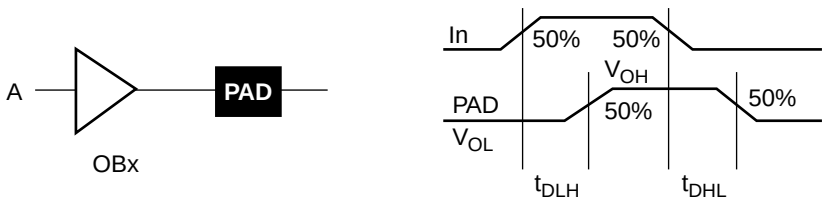


Figure 15 • *Output Buffer Delays*

Table 2 • *Output Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, 35pF load, T_J = 70°C)*

Macro Type	Description	Max. t_{DLH}	Max. t_{DHL}	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	4.20	4.47	ns
OB33PN	3.3V, PCI Output Current, Nominal Slew Rate	5.22	6.96	ns
OB33PL	3.3V, PCI Output Current, Low Slew Rate	6.30	8.61	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	6.26	6.76	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	7.70	10.80	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	9.18	14.15	ns
OB25HH	2.5V, High Output Current, High Slew Rate	7.65	3.95	ns
OB25HN	2.5V, High Output Current, Nominal Slew Rate	8.77	6.24	ns
OB25HL	2.5V, High Output Current, Low Slew Rate	10.34	7.74	ns
OB25LH	2.5V, Low Output Current, High Slew Rate	13.43	5.71	ns
OB25LN	2.5V, Low Output Current, Nominal Slew Rate	14.74	9.73	ns
OB25LL	2.5V, Low Output Current, Low Slew Rate	16.17	12.86	ns
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.40	6.02	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	7.15	9.99	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	8.83	12.82	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	8.30	9.28	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	10.44	15.38	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	12.62	20.63	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*

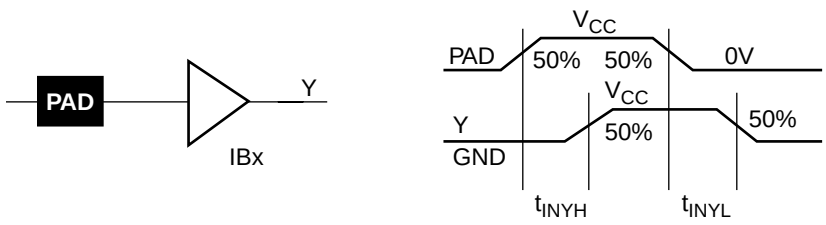


Figure 16 • *Input Buffer Delays*

Table 3 • *Input Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, 35pF load, T_J = 70°C)*

Macro Type	Description	Max. t_{IHYH}	Max. t_{INYL}	Units
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	2.25	0.59	ns
IB25LP	2.5V, CMOS Input Levels, Low Power	3.10	1.47	ns
IB33	3.3V, CMOS Input Levels, No Pull-up Resistor	2.14	0.99	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y HIGH*
2. *t_{INYL} = Input Pad-to-Y LOW*

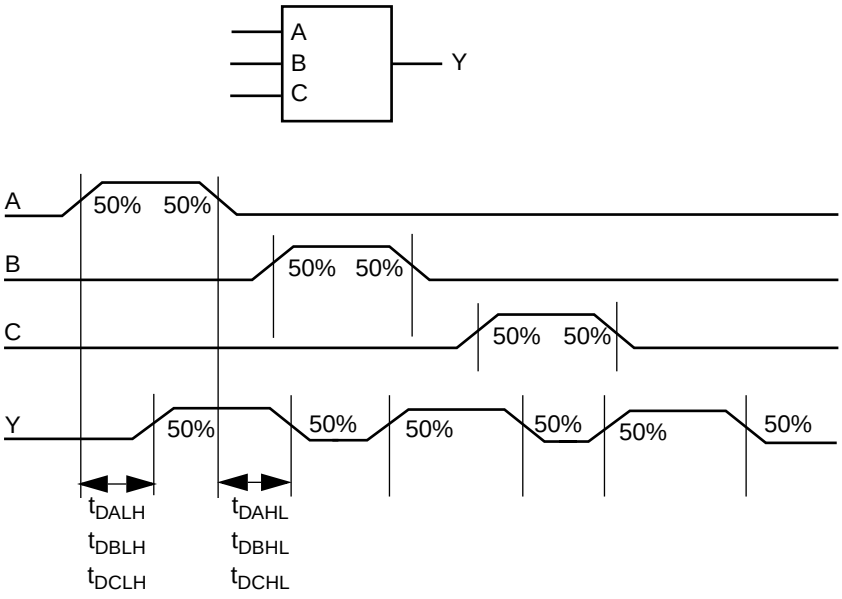


Figure 17 • *Module Delays*

Table 4 • *Sample Macrocell Library Listing (Worst-Case Commercial Conditions, V_{DDL} = 2.3V, 35pF load, T_J = 70° C)*

Cell Name	Description	Maximum Intrinsic Delay	Minimum Setup/Hold	Units
NAND2	2-Input NAND	0.42		ns
AND2	2-Input AND	0.40		ns
NOR3	3-Input NOR	0.42		ns
MUX2L	2-1 Mux with Active Low Select	0.42		ns
OA21	2-Input OR into a 2-Input AND	0.40		ns
XOR2	2-Input Exclusive OR	0.34		ns
LDL	Active Low Latch (LH/HL)	D: 0.26/0.21	t_{setup} 0.54 t_{hold} 0.20	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)	CLK-Q: 0.42/0.37	t_{setup} 0.43 t_{hold} 0.20	ns

Note: *Assumes two standard loads.*

Embedded Memory Specifications

This section focuses on the embedded memory of the ProASIC 500K family. It describes the SRAM and FIFO interface signals and includes timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks. See Table 5.

Enclosed Timing Diagrams—SRAM Mode:

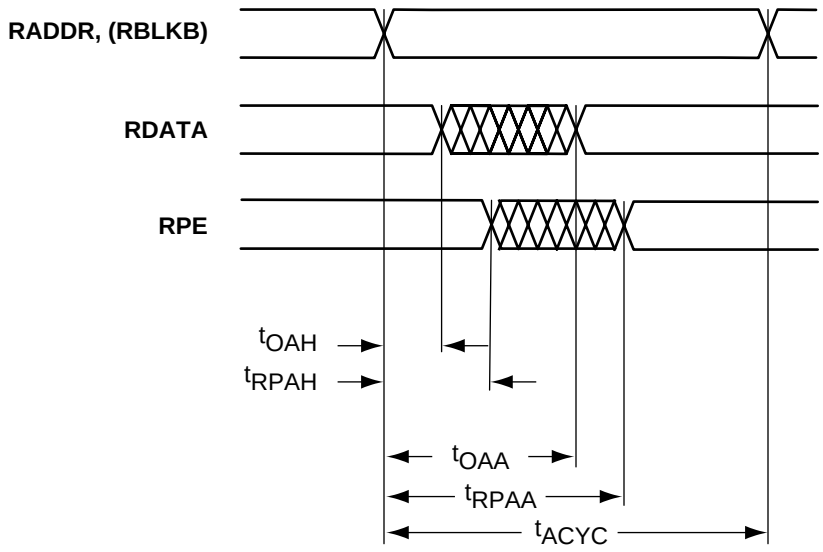
- Asynchronous RAM Read, Address Controlled, RDB=0
- Asynchronous RAM Read, RDB Controlled
- Asynchronous RAM Write
- Synchronous RAM Read, Access Timed Output Strobe
- Synchronous RAM Read, Pipeline Mode Outputs
- Synchronous RAM Write
- Synchronous Write & Read to the Same Location
- Asynchronous Write & Synchronous Read to the Same Location
- Asynchronous Write & Read to the Same Location
- Synchronous Write & Asynchronous Read to the Same Location

Table 5 • *Memory Block SRAM Interface Signals*

SRAM Signal	Hookup	Bits	In/Out	Description
WCLKS	Route	1	IN	Write clock used on synchronization on write side
RCLKS	Route	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	Route	8	IN	Read address.
RBLKB	Route/ Config.	1	IN	Negative true read block select.
RDB	Route/ Config.	1	IN	Negative true read pulse.
WADDR<0:7>	Route	8	IN	Write address.
WBLKB	Route/ Config.	1	IN	Negative true write block select.
DI<0:8>	Route	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true.
WRB	Route	1	IN	Negative true write pulse.
DO<0:8>	Route	9	OUT	Output data bits <0:8>
RPE	Route	1	OUT	Read parity error.
WPE	Route	1	OUT	Write parity error.
PARODD	Config.	1	IN	Selects odd parity generation/detect when high, even when low.

Notes: *Not all signals shown are used in all modes.*
Config. = Configurable

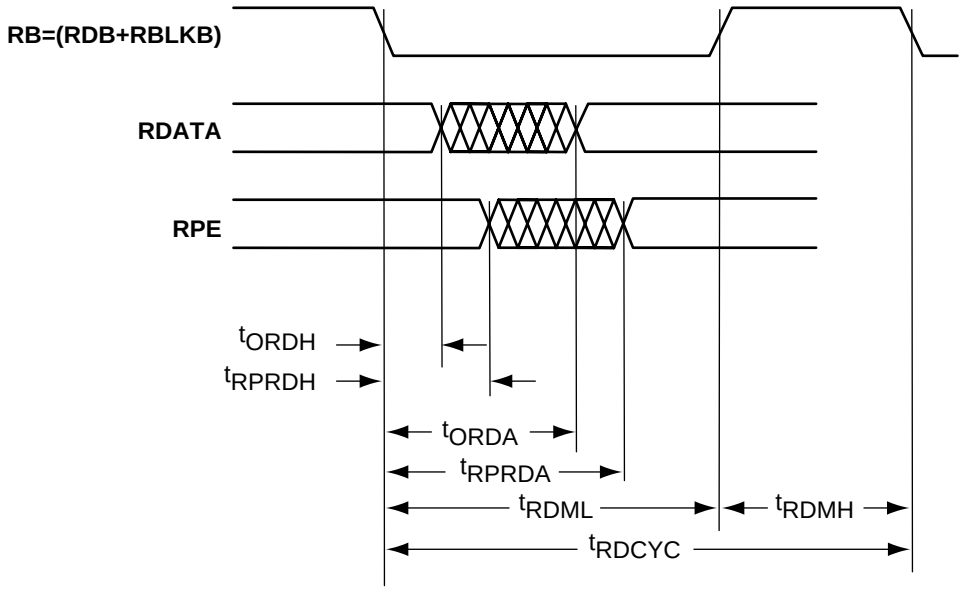
Asynchronous RAM Read, Address Controlled, RDB=0



T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New RDATA access from RADDR stable	7.5		ns	
OAH	Old RDATA hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

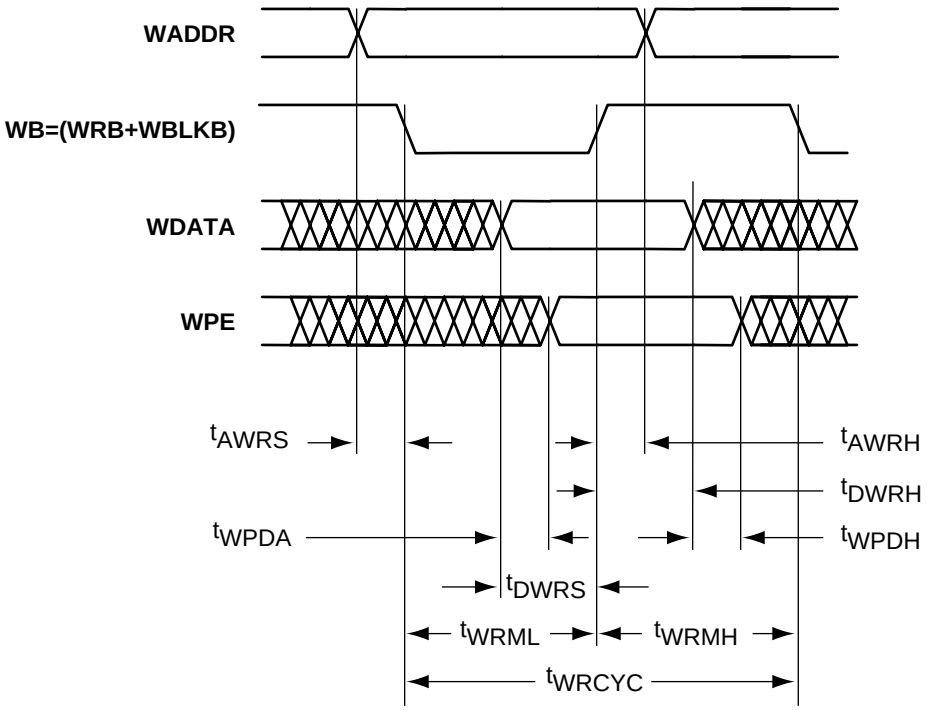
Asynchronous RAM Read, RDB Controlled



T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

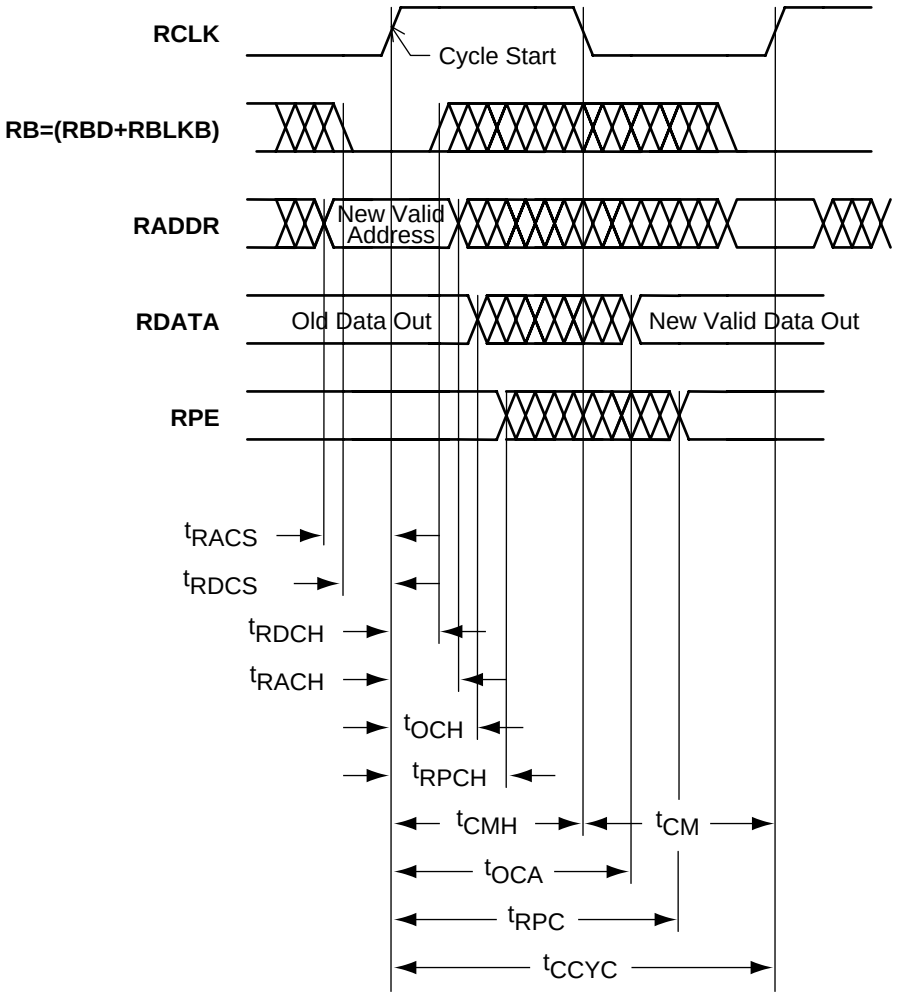
Asynchronous RAM Write



T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	WDATA hold from WB ↑	1.5		ns	
DWRS	WDATA setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	WDATA setup to WB ↑	2.5		ns	PARGEN is active.
WPDA	WPE access from WDATA	3.0		ns	WPE is invalid while
WPDH	WPE hold from WDATA		1.0	ns	PARGEN is active.
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

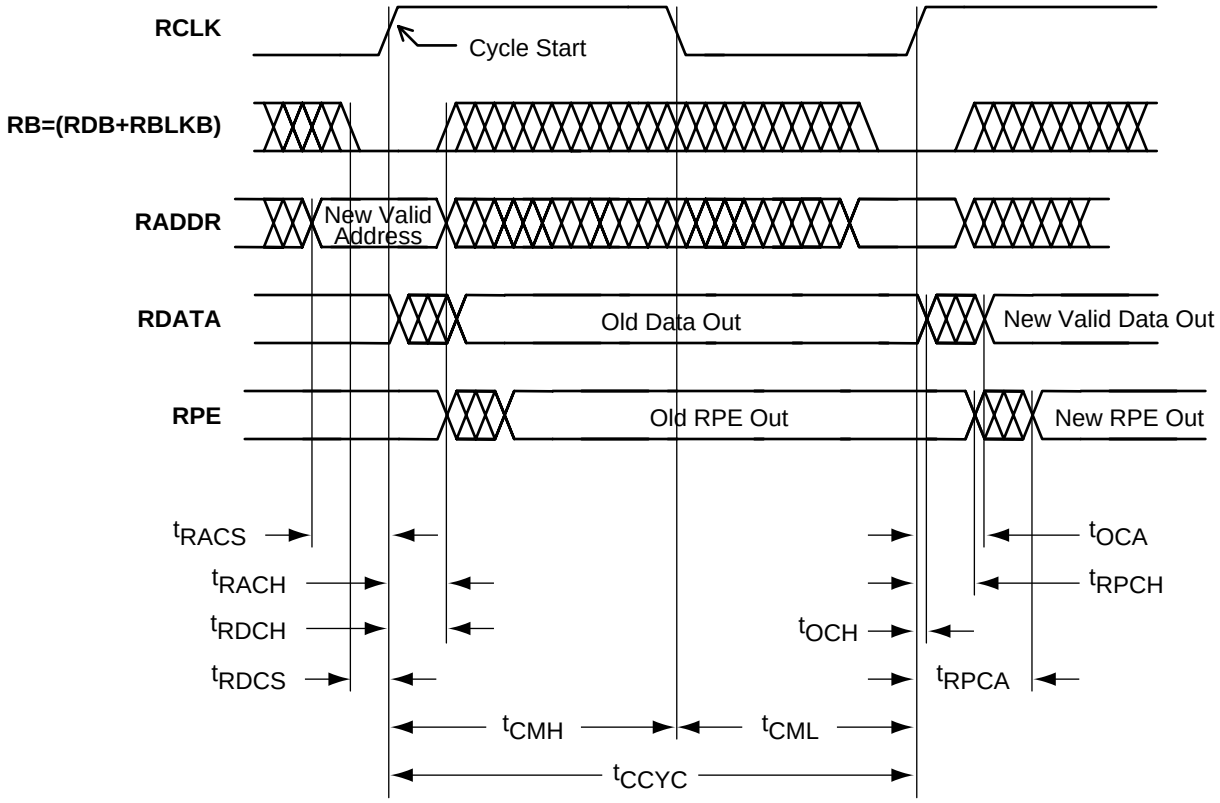
Synchronous RAM Read, Access Timed Output Strobe



T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New RDATA access from CLK ↑	7.5		ns	
OCH	Old RDATA valid from CLK ↑		3.0	ns	
RACH	RADDR hold from CLK ↑	0.5		ns	
RACS	RADDR setup to CLK ↑	1.0		ns	
RDCH	RDB hold from CLK ↑	0.5		ns	
RDCS	RDB setup to CLK ↑	1.0		ns	
RPCA	New RPE access from CLK ↑	9.5		ns	
RPCH	Old RPE valid from CLK ↑		3.0	ns	

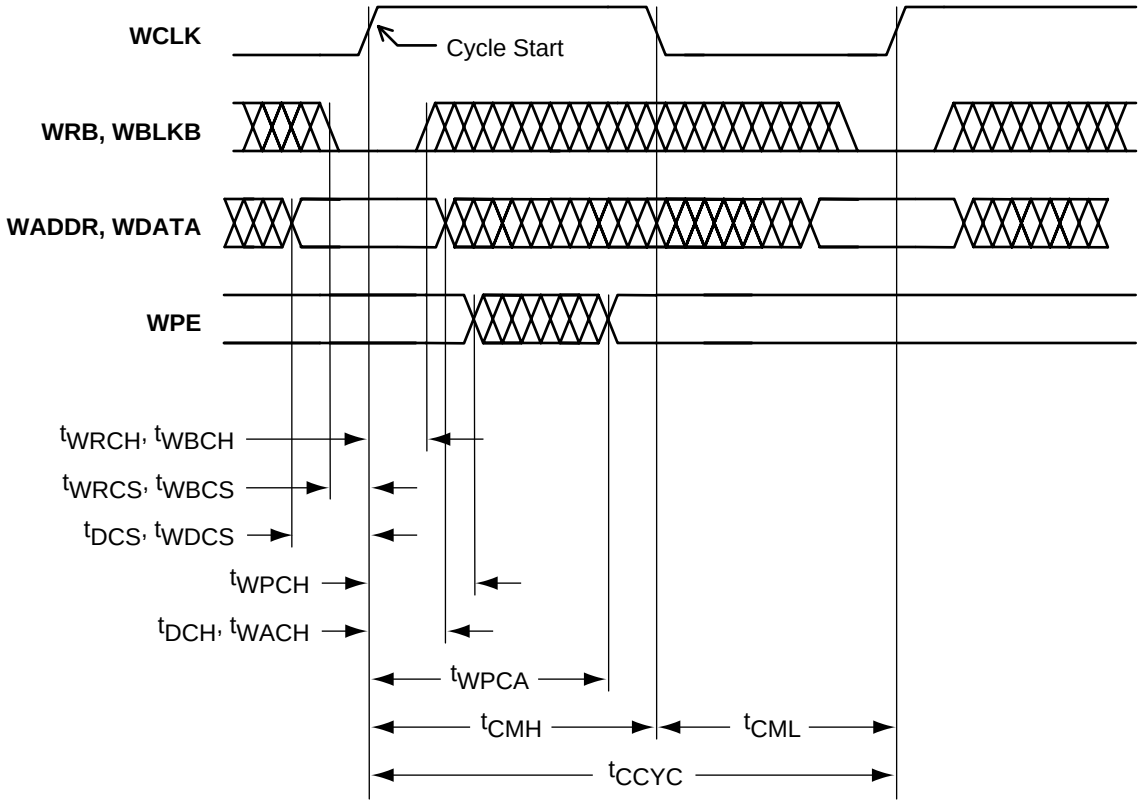
Synchronous RAM Read, Pipeline Mode Outputs



T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New RDATA access from CLK ↑	2.0		ns	
OCH	Old RDATA valid from CLK ↑		.75	ns	
RACH	RADDR hold from CLK ↑	0.5		ns	
RACS	RADDR setup to CLK ↑	1.0		ns	
RDCH	RDB hold from CLK ↑	0.5		ns	
RDCS	RDB setup to CLK ↑	1.0		ns	
RPCA	New RPE access from CLK ↑	4.0		ns	
RPCH	Old RPE valid from CLK ↑		1.0	ns	

Synchronous RAM Write

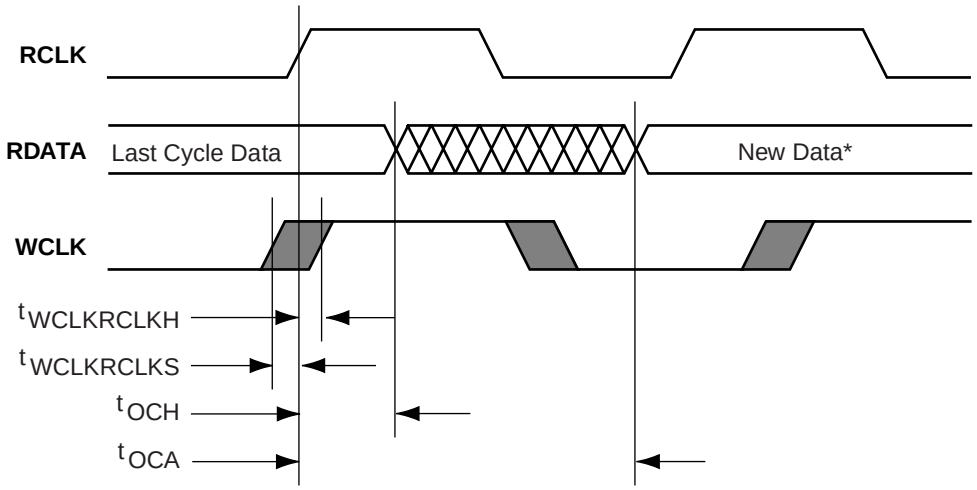


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	WDATA hold from CLK ↑	0.5		ns	
DCS	WDATA setup to CLK ↑	1.0		ns	
WACH	WADDR hold from CLK ↑	0.5		ns	
WACS	WADDR setup to CLK ↑	1.0		ns	
WPCA	New WPE access from CLK ↑	3.0		ns	WPE is invalid while PARGEN is active.
WPCH	Old WPE valid from CLK ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from CLK ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to CLK ↑	1.0		ns	

Note: *On simultaneous read and write accesses to the same location WDATA is output to RDATA*

Synchronous Write & Read to the Same Location



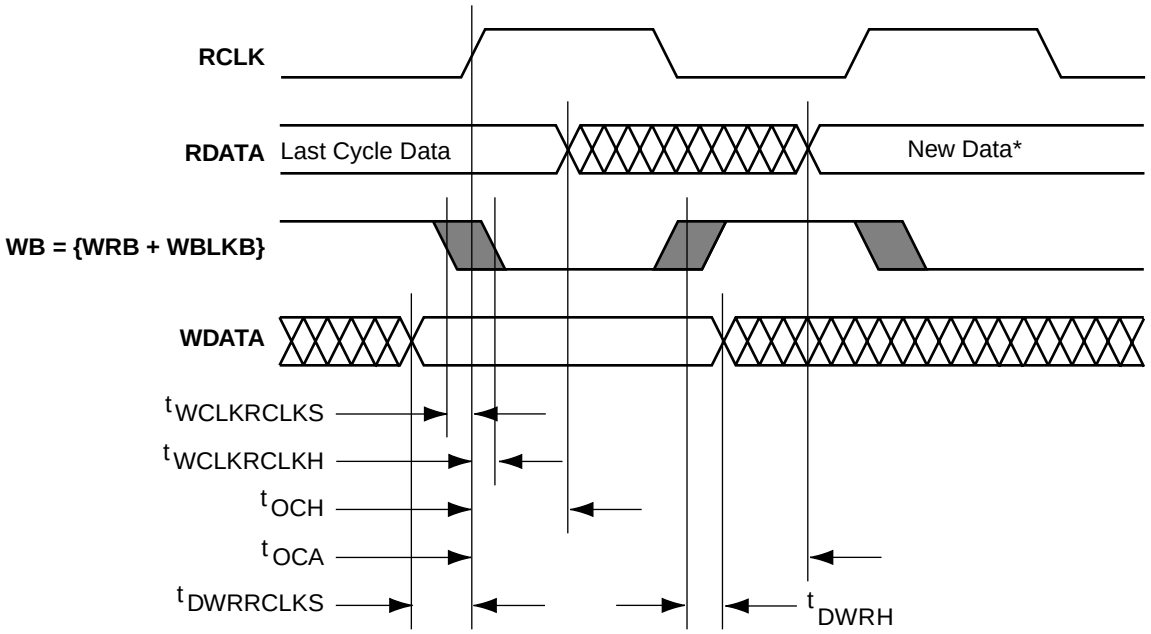
* New data is read if WCLK ↑ occurs before setup time.
The data stored is read if WCLK ↑ occurs after hold time.

TJ=0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLK ↑ to RCLK ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLK ↑ to RCLK ↑ hold time		7.0	ns	
OCH	Old RDATA valid from RCLK ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New RDATA valid from RCLK ↑	7.5		ns	

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLK and RCLK driven by the same design signal.*
3. *If WCLK changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write & Synchronous Read to the Same Location



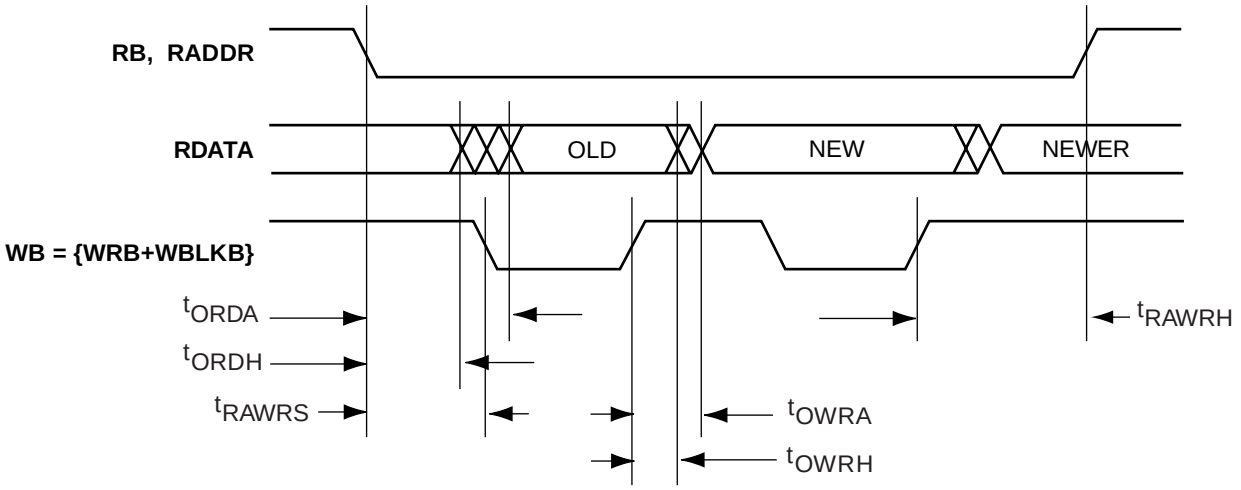
* New data is read if WB ↓ occurs before setup time.
The stored data is read if WB ↓ occurs after hold time.

TJ=0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLK ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLK ↑ hold time		7.0	ns	
OCH	Old RDATA valid from RCLK ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New RDATA valid from RCLK ↑	7.5		ns	
DWRRCLKS	WDATA to RCLK ↑ setup time	0		ns	
DWRH	WDATA to WB ↑ hold time		1.5	ns	

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write & Read to the Same Location

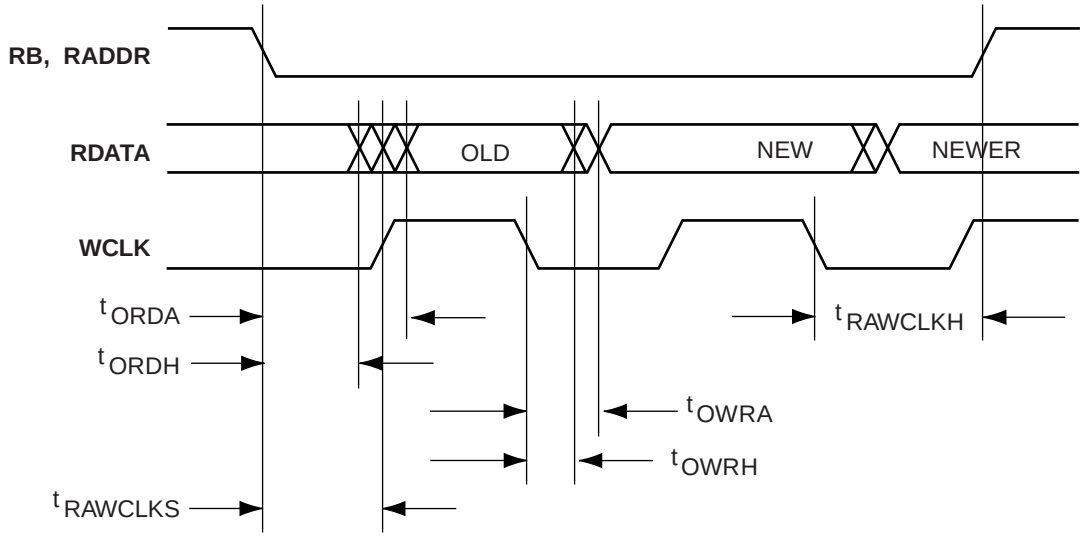


TJ=0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
OWRA	New RDATA access from WB ↑	3.0		ns	
OWRH	Old RDATA valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

1. *During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation or RAWRS will disturb access to the OLD data.*
3. *Violation of RAWRH will disturb access to the NEWER data.*

Synchronous Write & Asynchronous Read to the Same Location



TJ=0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
OWRA	New RDATA access from WCLK ↓	3.0		ns	
OWRH	Old RDATA valid from WCLK ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLK ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLK ↓	5.0		ns	

1. *During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation of RAWCLKS will disturb access to OLD data.*
3. *Violation of RAWCLKH will disturb access to NEWER data.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty respectively. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write (read) operation changes from inhibited to accepted after the read (write) signal which causes the transition from Full (Empty) to not Full (Empty) is indeterminate. This indeterminate period start 1ns after the RB (WB) transition which deactivates Full (Not Empty) and ends 3ns after the RB (WB) transition, for slow cycles. For fast cycles, the indeterminate period ends 7.5ns—RDL (WRL) or 3ns after the RB (WB) transition whichever is later.

The timing diagram for write is shown in Figure 18. The timing diagram for read is shown in Figure 19.

Enclosed Timing Diagrams—FIFO Mode:

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe
- Synchronous FIFO Read, Pipeline Mode Outputs
- Synchronous FIFO Write
- FIFO Reset

Table 6 • *Memory Block FIFO Interface Signals*

FIFO Signal	Hookup	Bits	In/Out	Description
WCLKS	Route	1	IN	Write clock used on synchronization on write side
RCLKS	Route	1	IN	Read clock used on synchronization on read side
LEVEL <0:7>	Route/ Config.	8	IN	Direct configuration implements static flag logic.
RBLKB	Route/ Config.	1	IN	Negative true read block select.
RDB	Route/ Config.	1	IN	Negative true read pulse.
RESET	Route	1	IN	Negative true reset for FIFO pointers.
WBLKB	Route/ Config.	1	IN	Negative true write block select.
DI<0:8>	Route	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true.
WRB	Route	1	IN	Negative true write pulse.
FULL, EMPTY	Route	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read.
EQTH, GEQTH	Route	2	OUT	EQTH is true when the FIFO holds (LEVEL) words. GEQTH is true when the FIFO holds (LEVEL) words or more.
DO<0:8>	Route	9	OUT	Output data bits <0:8>
RPE	Route	1	OUT	Read parity error.
WPE	Route	1	OUT	Write parity error.
LGDEP <0:2>	Config.	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	Config.	1	IN	Selects odd parity generation/detect when high, even when low.

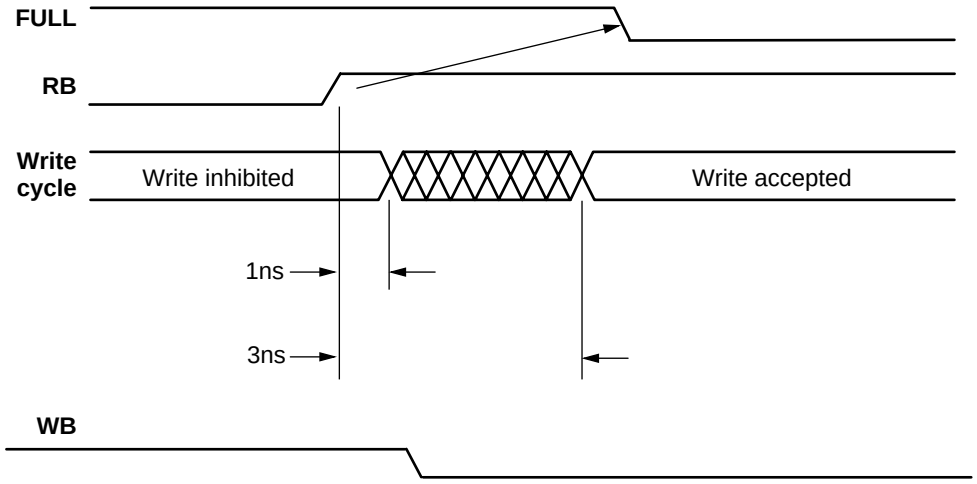


Figure 18 • *Write Timing Diagram*

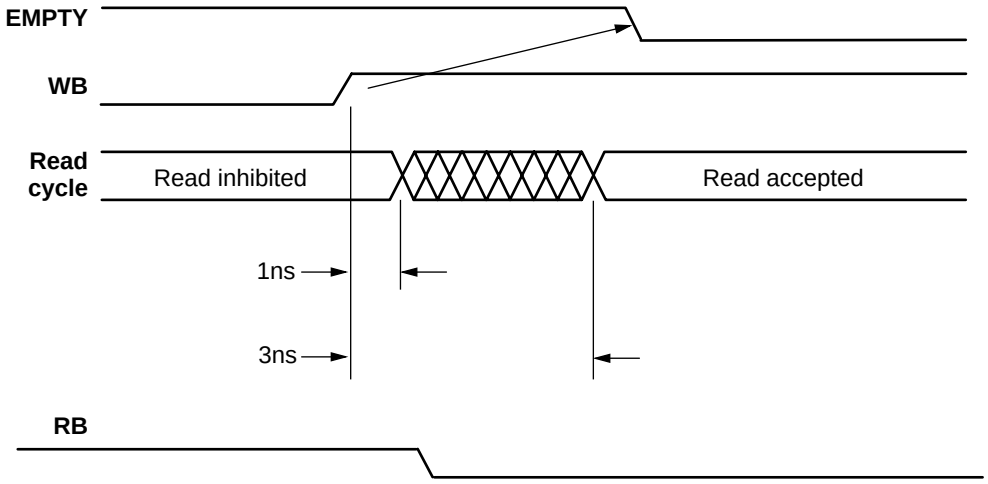
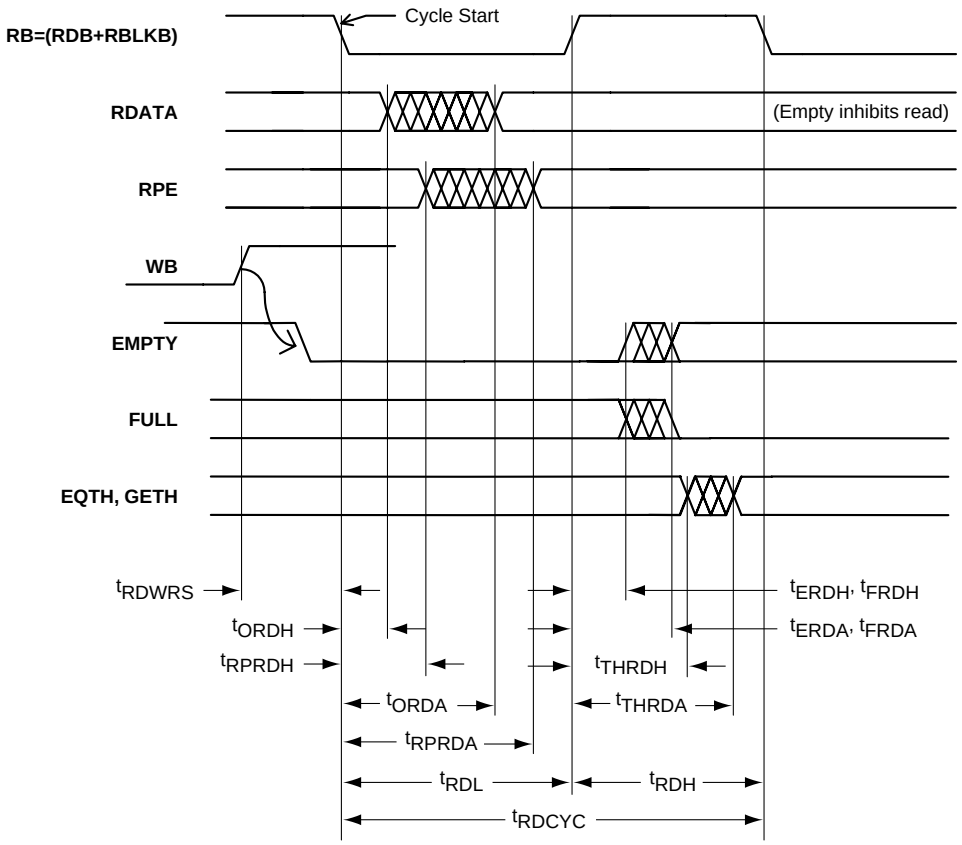


Figure 19 • *Read Timing Diagram*

Asynchronous FIFO Read

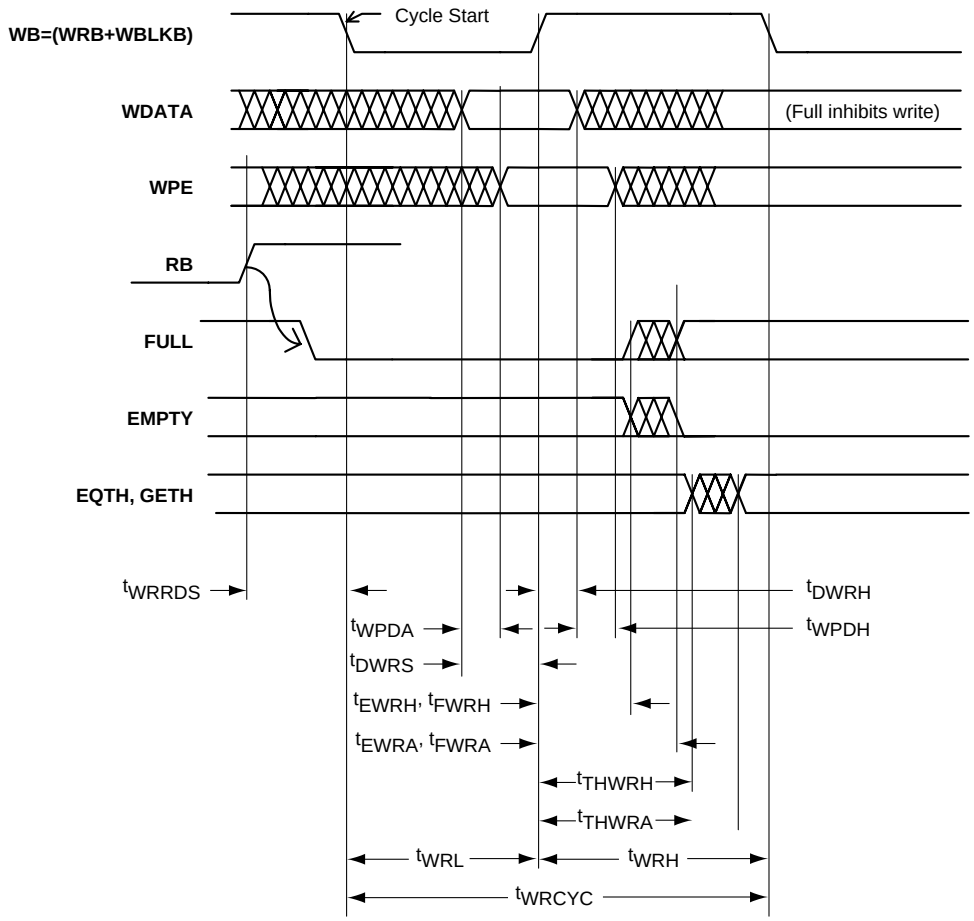


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
ERDA	New EMPTY access from RB ↑	3.0*		ns	
FRDA	FULL↓ access from RB ↑	3.0*		ns	
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0**		ns	Enabling the read operation.
			1.0	ns	Inhibiting the read operation.
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes: ** At fast cycles, ERDA & FRDA*
***At fast cycles, RDWRS (for enabling read) = MAX (7.5ns–WRL), 3.0ns*

Asynchronous FIFO Write

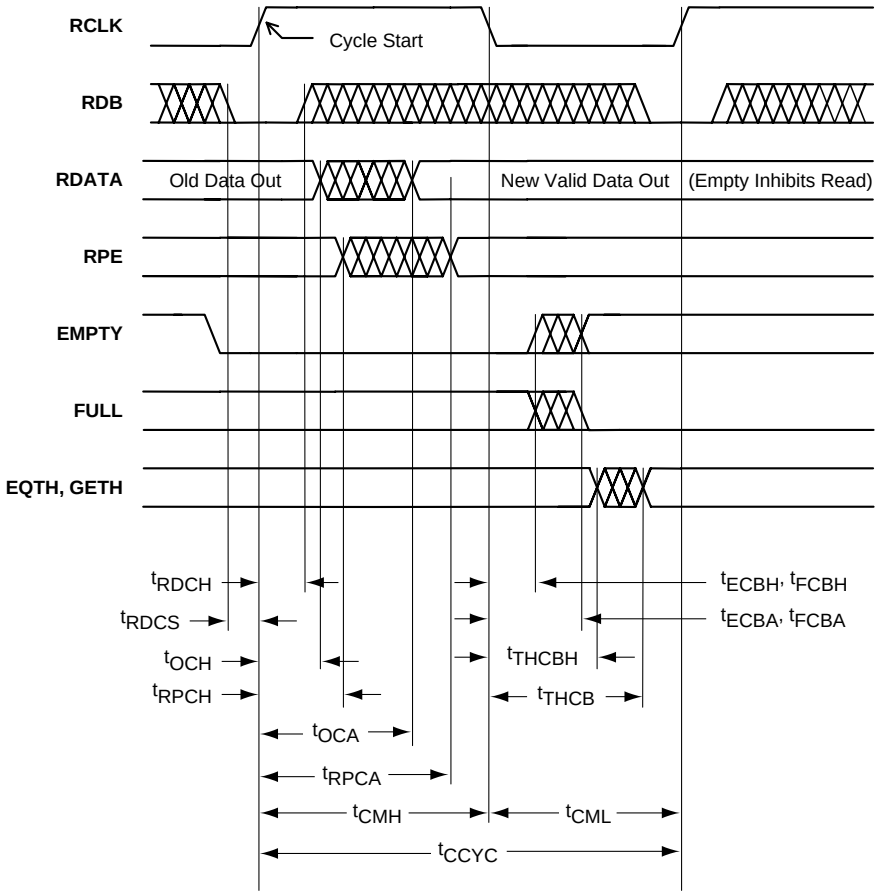


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	WDATA hold from WB ↑	1.5		ns	
DWRS	WDATA setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	WDATA setup to WB ↑	2.5		ns	PARGEN is active.
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
EWRA	EMPTY ↓ access from WB ↑	3.0*		ns	
FWRA	New FULL access from WB ↑	3.0*		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from WDATA	3.0		ns	WPE is invalid while PARGEN is active.
WPDH	WPE hold from WDATA		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0**		ns	Enabling the write operation.
			1.0		Inhibiting the write operation.
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes: ** At fast cycles, EWRA, FWRA = MAX((7.5ns-WRL), 3.0ns)*
***At fast cycles, WWRDS (for enabling write) = MAX (7.5ns–RDL), 3.0ns*

Synchronous FIFO Read, Access Timed Output Strobe

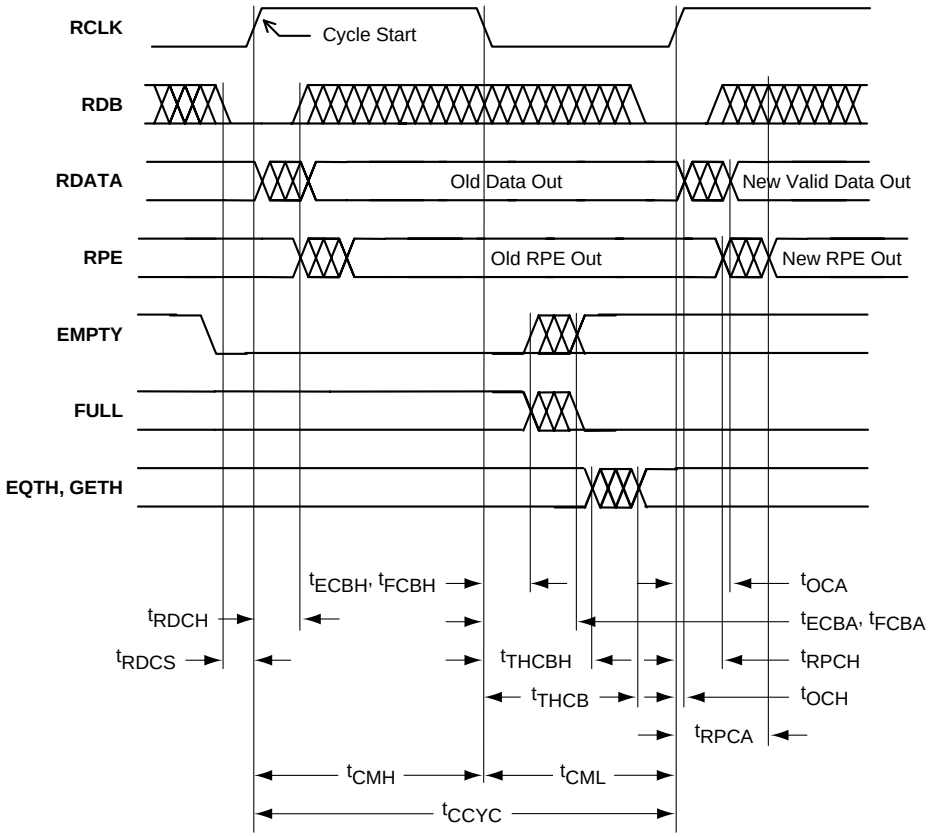


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from CLK ↓	3.0*		ns	
FCBA	FULL ↓ access from CLK ↓	3.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
OCA	New RDATA access from CLK ↑	7.5		ns	
OCH	Old RDATA valid from CLK ↑		3.0	ns	
RDCH	RDB hold from CLK ↑	0.5		ns	
RDCS	RDB setup to CLK ↑	1.0		ns	
RPCA	New RPE access from CLK ↑	9.5		ns	
RPCH	Old RPE valid from CLK ↑		3.0	ns	
THCBA	EQTH or GETH access from CLK ↓	4.5		ns	

Note: ** At fast cycles, ECBA & FCBA = MAX((7.5ns-CMH), 3.0ns)*

Synchronous FIFO Read, Pipeline Mode Outputs

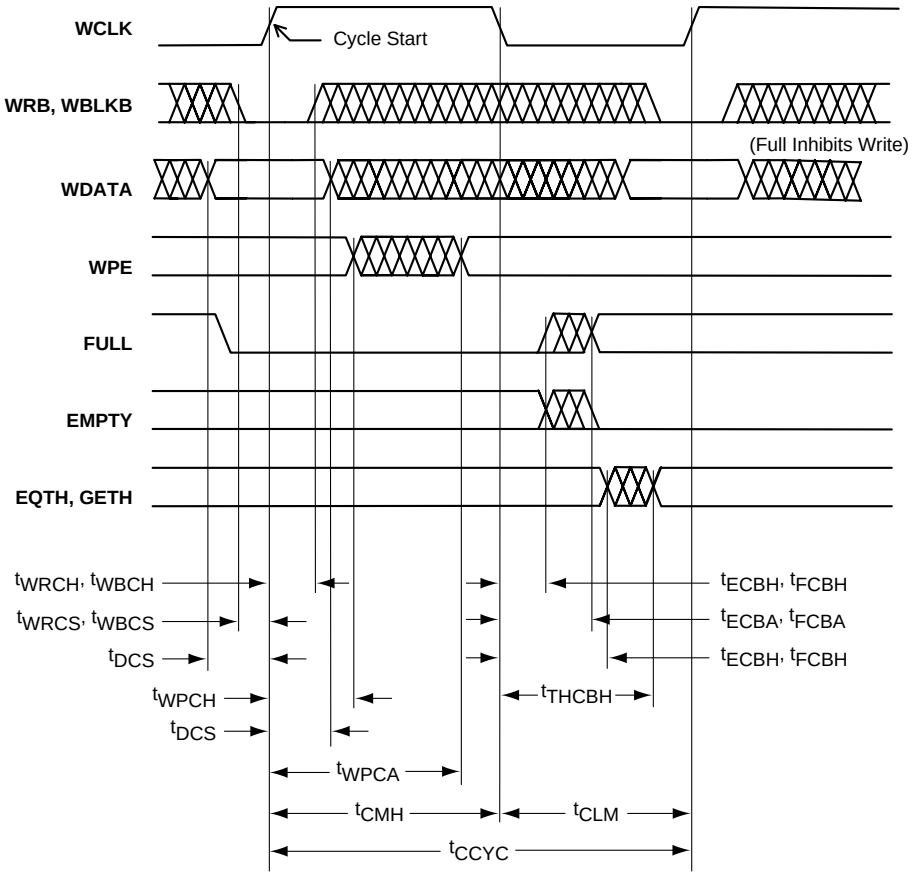


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from CLK ↓	3.0*		ns	
FCBA	FULL ↓ access from CLK ↓	3.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
OCA	New RDATA access from CLK ↑	2.0		ns	
OCH	Old RDATA valid from CLK ↑		0.75	ns	
RDCH	RDB hold from CLK ↑	0.5		ns	
RDCS	RDB setup to CLK ↑	1.0		ns	
RPCA	New RPE access from CLK ↑	4.0		ns	
RPCH	Old RPE valid from CLK ↑		1.0	ns	
THCBA	EQTH or GETH access from CLK ↓	4.5		ns	

Note: ** At fast cycles, ECBA & FCBA = MAX ((7.5ns-CMS), 3.0ns)*

Synchronous FIFO Write

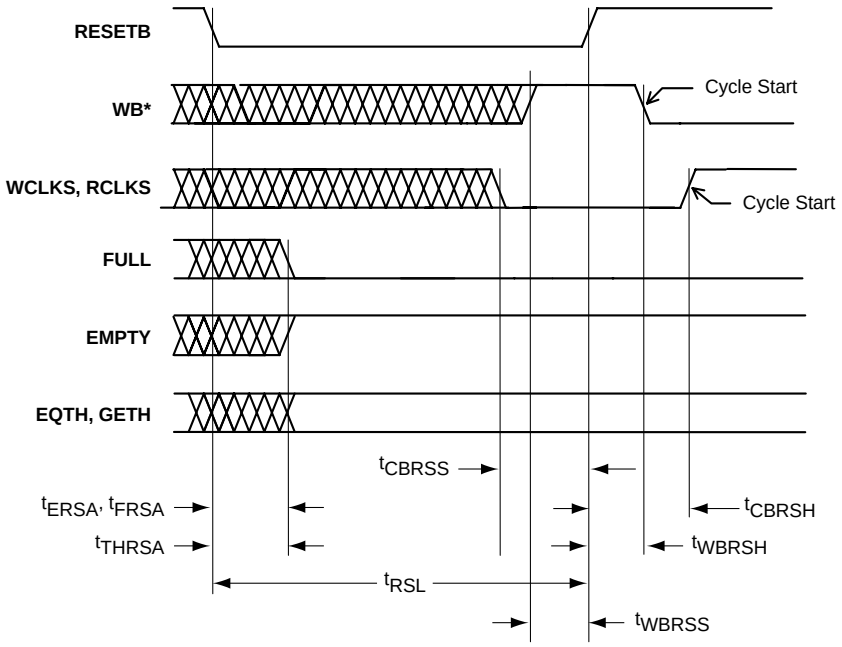


T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	WDATA hold from CLK ↑	0.5		ns	
DCS	WDATA setup to CLK ↑	1.0		ns	
FCBA	New FULL access from CLK ↓	3.0*		ns	
ECBA	EMPTY↓ access from CLK ↓	3.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
THCBA	EQTH or GETH access from CLK ↓	4.5		ns	
WPCA	New WPE access from CLK ↑	3.0		ns	WPE is invalid while PARGEN is active.
WPCH	Old WPE valid from CLK ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from CLK ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to CLK ↑	1.0		ns	

Note: ** At fast cycles, ECBA & FCBA = MAX((7.5ns-CMH), 3.0ns)*

FIFO Reset



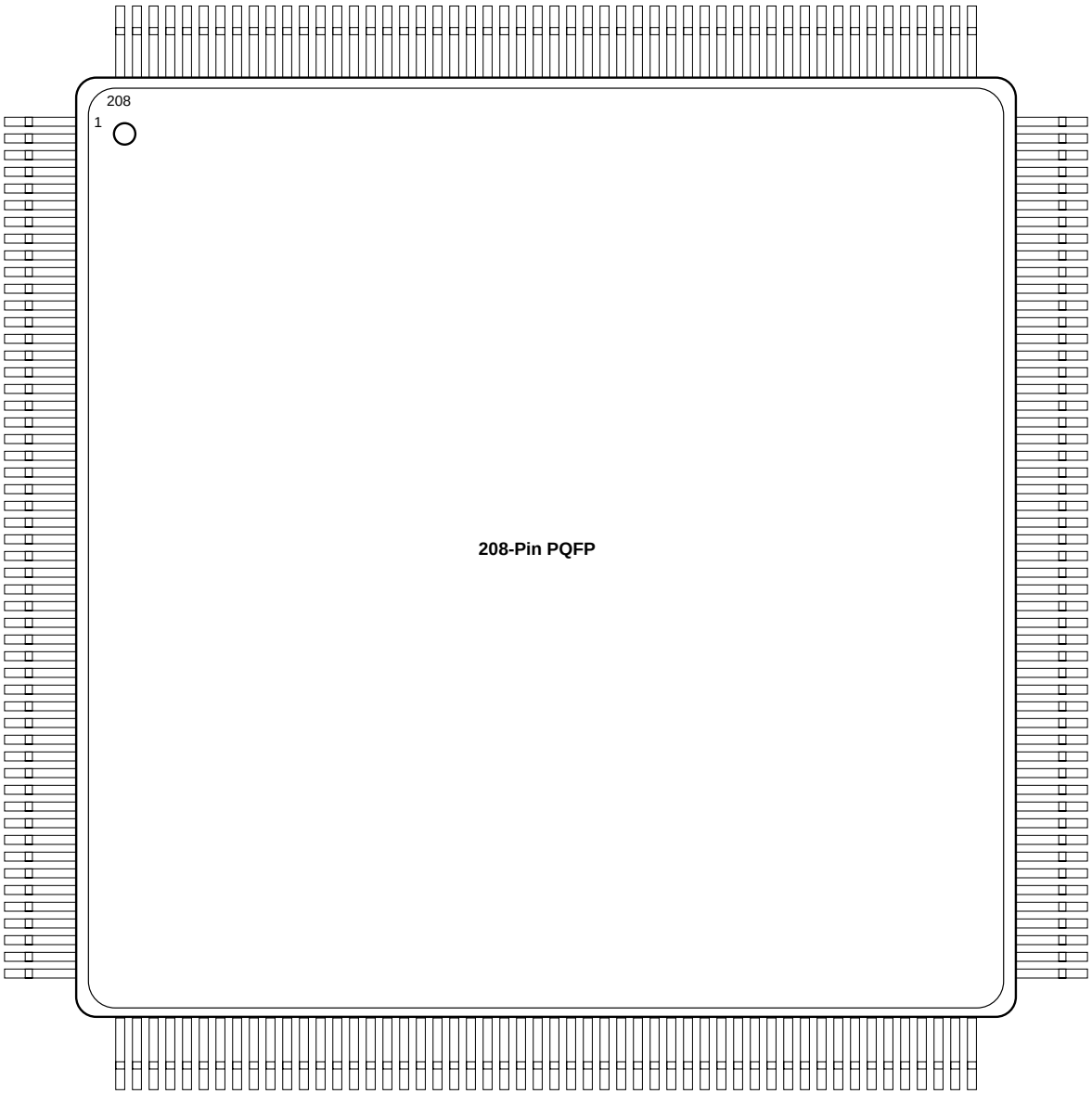
*WB = WRB + WBLRB

T_J= 0°C to 110°C; V_{DDL} = 2.30V to 2.70V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only.
CBRSS	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only.
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only.
WBRSS	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only.

Package Pin Assignments

208-Pin PQFP



208-Pin PQFP

Pin No.	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
1	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
17	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	G1	G1	G1	G1
26	G0	G0	G0	G0
27	I/O	I/O	I/O	I/O
28	I/O	I/O	I/O	I/O
29	GND	GND	GND	GND
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O
36	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O
71	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
89	V_{DDP}	V_{DDP}	GND	V_{DDP}
90	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O/TCK	I/O/TCK	I/O/TCK	I/O/TCK
102	I/O/TDI	I/O/TDI	I/O/TDI	I/O/TDI
103	I/O/TMS	I/O/TMS	I/O/TMS	I/O/TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

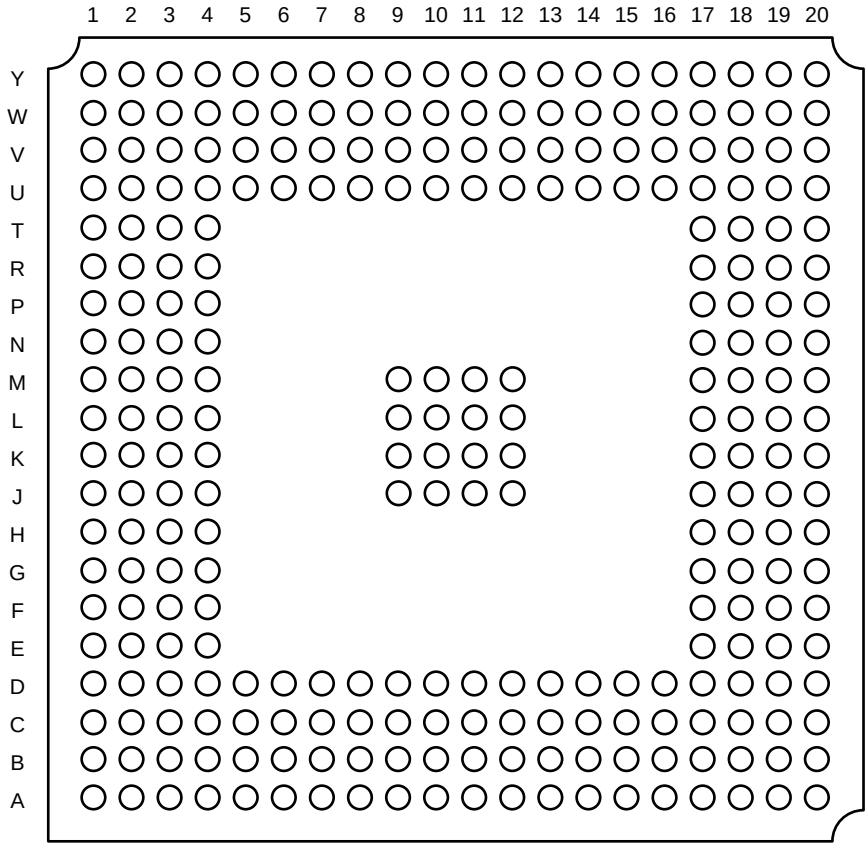
208-Pin PQFP (Continued)

Pin No.	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
105	GND	GND	GND	GND
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	I/O/TDO	I/O/TDO	I/O/TDO	I/O/TDO
109	I/O/TRSTB	I/OTRSTB	I/O/TRSTB	I/O/TRSTB
110	I/O/RCK	I/O/RCK	I/O/RCK	I/O/RCK
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O
126	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	I/O	I/O	I/O	I/O
130	GND	GND	GND	GND
131	I/O	I/O	I/O	I/O
132	I/O	I/O	I/O	I/O
133	G2	G2	G2	G2
134	G3	G3	G3	G3
135	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDL}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND
142	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
143	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND

Pin No.	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND
163	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
172	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O
184	I/O	I/O	I/O	I/O
185	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
188	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

Package Pin Assignments (continued)

272-Pin PBGA



272-Pin PBGA

Ext. Ball	A500K050 Function	A500K130 Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
B1	I/O	I/O
B2	I/O	I/O
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
C1	I/O	I/O
C2	I/O	I/O
C3	I/O	I/O
C4	I/O	I/O
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	I/O	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O	I/O
D4	V_{DDP}	V_{DDP}
D5	V_{DDP}	V_{DDP}
D6	V_{DDP}	V_{DDP}
D7	I/O	I/O
D8	V_{DDL}	V_{DDL}
D9	V_{DDL}	V_{DDL}
D10	V_{DDL}	V_{DDL}
D11	V_{DDL}	V_{DDL}
D12	V_{DDL}	V_{DDL}
D13	V_{DDL}	V_{DDL}
D14	I/O	I/O
D15	V_{DDP}	V_{DDP}
D16	V_{DDP}	V_{DDP}
D17	V_{DDP}	V_{DDP}
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O	I/O
E4	V_{DDP}	V_{DDP}
E17	V_{DDP}	V_{DDP}
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	V_{DDP}	V_{DDP}
F17	V_{DDP}	V_{DDP}
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	G3	G3
J1	I/O	I/O
J2	G0	G0
J3	G1	G1
J4	V_{DDL}	V_{DDL}
J9	GND	GND
J10	GND	GND
J11	GND	GND
J12	GND	GND
J17	V_{DDL}	V_{DDL}
J18	G2	G2
J19	I/O	I/O
J20	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	V_{DDL}	V_{DDL}
K9	GND	GND
K10	GND	GND
K11	GND	GND
K12	GND	GND
K17	V_{DDL}	V_{DDL}
K18	I/O	I/O
K19	I/O	I/O
K20	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O

272-Pin PBGA (Continued)

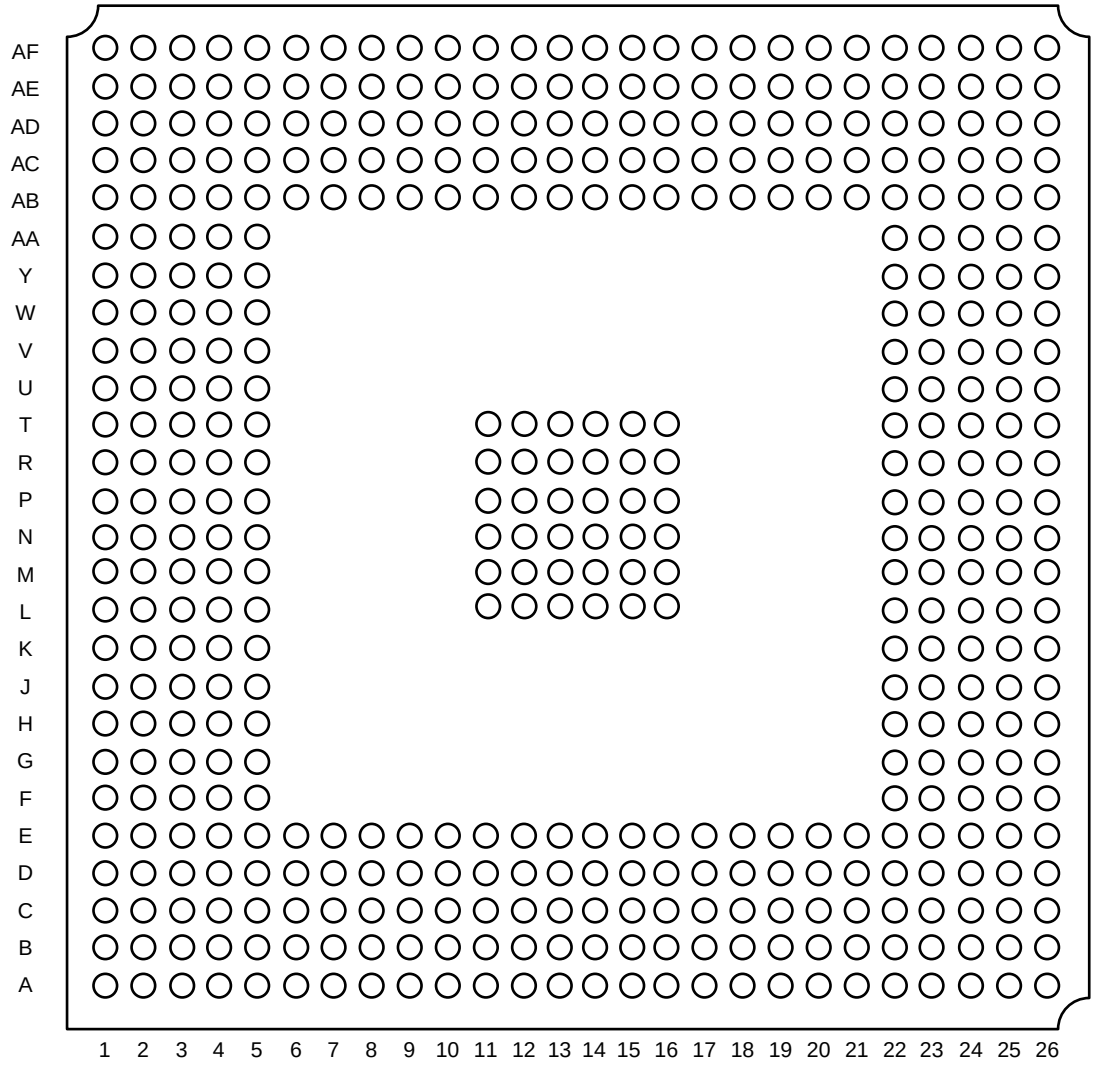
Ext. Ball	A500K050 Function	A500K130 Function
L3	I/O	I/O
L4	V_{DDL}	V_{DDL}
L9	GND	GND
L10	GND	GND
L11	GND	GND
L12	GND	GND
L17	V_{DDL}	V_{DDL}
L18	I/O	I/O
L19	I/O	I/O
L20	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	V_{DDL}	V_{DDL}
M9	GND	GND
M10	GND	GND
M11	GND	GND
M12	GND	GND
M17	V_{DDL}	V_{DDL}
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	V_{DDL}	V_{DDL}
N17	V_{DDL}	V_{DDL}
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	V_{DDP}	V_{DDP}
P17	V_{DDP}	V_{DDP}
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	V_{DDP}	V_{DDP}
R17	V_{DDP}	V_{DDP}
R18	I/O	I/O
R19	I/O	I/O
R20	I/O	I/O

Ext. Ball	A500K050 Function	A500K130 Function
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	V_{DDP}	V_{DDP}
T17	V_{DDP}	V_{DDP}
T18	I/O	I/O
T19	I/O	I/O
T20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	V_{DDP}	V_{DDP}
U5	V_{DDP}	V_{DDP}
U6	V_{DDP}	V_{DDP}
U7	I/O	I/O
U8	V_{DDL}	V_{DDL}
U9	V_{DDL}	V_{DDL}
U10	V_{DDL}	V_{DDL}
U11	V_{DDL}	V_{DDL}
U12	V_{DDL}	V_{DDL}
U13	V_{DDL}	V_{DDL}
U14	I/O	I/O
U15	V_{DDP}	V_{DDP}
U16	V_{DDP}	V_{DDP}
U17	V_{DDP}	V_{DDP}
U18	I/O/RCK	I/O/RCK
U19	I/O	I/O
U20	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O	I/O
V11	I/O	I/O
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	I/O/TMS	I/O/TMS
V18	I/O/TDO	I/O/TDO

Ext. Ball	A500K050 Function	A500K130 Function
V19	I/O	I/O
V20	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O
W9	I/O	I/O
W10	I/O	I/O
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O
W15	I/O	I/O
W16	I/O	I/O
W17	I/O/TCK	I/O/TCK
W18	V_{PP}	V_{PP}
W19	I/O/TRSTB	I/O/TRSTB
W20	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	I/O	I/O
Y9	I/O	I/O
Y10	I/O	I/O
Y11	I/O	I/O
Y12	I/O	I/O
Y13	I/O	I/O
Y14	I/O	I/O
Y15	I/O	I/O
Y16	I/O	I/O
Y17	I/O	I/O
Y18	I/O/TDI	I/O/TDI
Y19	V_{PN}	V_{PN}
Y20	I/O	I/O

Package Pin Assignments (continued)

456-Pin PBGA



456-Pin PBGA

Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
A1	V_{DDP}	V_{DDP}	V_{DDP}
A2	V_{DDP}	V_{DDP}	V_{DDP}
A3	NC	I/O	I/O
A4	IO	I/O	I/O
A5	IO	I/O	I/O
A6	NC	I/O	I/O
A7	IO	I/O	I/O
A8	NC	I/O	I/O
A9	NC	I/O	I/O
A10	IO	I/O	I/O
A11	NC	I/O	I/O
A12	NC	I/O	I/O
A13	IO	I/O	I/O
A14	NC	I/O	I/O
A15	NC	I/O	I/O
A16	IO	I/O	I/O
A17	NC	I/O	I/O
A18	NC	I/O	I/O
A19	IO	I/O	I/O
A20	NC	I/O	I/O
A21	NC	I/O	I/O
A22	IO	I/O	I/O
A23	NC	I/O	I/O
A24	NC	I/O	I/O
A25	V_{DDP}	V_{DDP}	V_{DDP}
A26	V_{DDP}	V_{DDP}	V_{DDP}
AA1	IO	I/O	I/O
AA2	IO	I/O	I/O
AA3	IO	I/O	I/O
AA4	IO	I/O	I/O
AA5	V_{DDL}	V_{DDL}	V_{DDL}
AA22	V_{DDL}	V_{DDL}	V_{DDL}
AA23	IO	I/O	I/O
AA24	IO	I/O	I/O
AA25	IO	I/O	I/O
AA26	NC	I/O	I/O
AB1	NC	I/O	I/O
AB2	IO	I/O	I/O
AB3	IO	I/O	I/O
AB4	IO	I/O	I/O
AB5	V_{DDL}	V_{DDL}	V_{DDL}
AB6	V_{DDL}	V_{DDL}	V_{DDL}
AB7	V_{DDL}	V_{DDL}	V_{DDL}
AB8	IO	I/O	I/O
AB9	IO	I/O	I/O
AB10	IO	I/O	I/O
AB11	IO	I/O	I/O
AB12	IO	I/O	I/O
AB13	IO	I/O	I/O
AB14	IO	I/O	I/O
AB15	IO	I/O	I/O
AB16	IO	I/O	I/O
AB17	IO	I/O	I/O
AB18	IO	I/O	I/O
AB19	IO	I/O	I/O
AB20	V_{DDL}	V_{DDL}	V_{DDL}
AB21	V_{DDL}	V_{DDL}	V_{DDL}
AB22	V_{DDL}	V_{DDL}	V_{DDL}
AB23	IO	I/O	I/O
AB24	IO	I/O	I/O
AB25	IO	I/O	I/O
AB26	IO	I/O	I/O
AC1	IO	I/O	I/O
AC2	IO	I/O	I/O
AC3	IO	I/O	I/O
AC4	V_{DDP}	V_{DDP}	V_{DDP}
AC5	IO	I/O	I/O
AC6	IO	I/O	I/O
AC7	IO	I/O	I/O
AC8	IO	I/O	I/O
AC9	IO	I/O	I/O
AC10	IO	I/O	I/O
AC11	IO	I/O	I/O
AC12	IO	I/O	I/O
AC13	IO	I/O	I/O
AC14	IO	I/O	I/O
AC15	IO	I/O	I/O
AC16	IO	I/O	I/O
AC17	IO	I/O	I/O
AC18	IO	I/O	I/O
AC19	IO	I/O	I/O
AC20	IO	I/O	I/O
AC21	IO/TMS	I/O/TMS	I/O/TMS
AC22	IO/TDO	I/O/TDO	I/O/TDO
AC23	V_{DDP}	V_{DDP}	V_{DDP}
AC24	IO/RCK	I/O/RCK	I/O/RCK
AC25	IO	I/O	I/O
AC26	NC	I/O	I/O
AD1	NC	I/O	I/O
AD2	IO	I/O	I/O
AD3	V_{DDP}	V_{DDP}	V_{DDP}
AD4	IO	I/O	I/O

Note: *NC = No Connection*

456-Pin PBGA (Continued)

Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
AD5	IO	I/O	I/O
AD6	IO	I/O	I/O
AD7	IO	I/O	I/O
AD8	IO	I/O	I/O
AD9	IO	I/O	I/O
AD10	IO	I/O	I/O
AD11	IO	I/O	I/O
AD12	IO	I/O	I/O
AD13	IO	I/O	I/O
AD14	IO	I/O	I/O
AD15	IO	I/O	I/O
AD16	IO	I/O	I/O
AD17	IO	I/O	I/O
AD18	IO	I/O	I/O
AD19	IO	I/O	I/O
AD20	IO	I/O	I/O
AD21	IO/TCK	I/O/TCK	I/O/TCK
AD22	V_{PP}	V_{PP}	V_{PP}
AD23	IO	I/O	I/O
AD24	V_{DDP}	V_{DDP}	V_{DDP}
AD25	IO	I/O	I/O
AD26	NC	I/O	I/O
AE1	V_{DDP}	V_{DDP}	V_{DDP}
AE2	V_{DDP}	V_{DDP}	V_{DDP}
AE3	IO	I/O	I/O
AE4	IO	I/O	I/O
AE5	IO	I/O	I/O
AE6	IO	I/O	I/O
AE7	IO	I/O	I/O
AE8	IO	I/O	I/O
AE9	IO	I/O	I/O
AE10	IO	I/O	I/O
AE11	IO	I/O	I/O
AE12	IO	I/O	I/O
AE13	IO	I/O	I/O
AE14	IO	I/O	I/O
AE15	IO	I/O	I/O
AE16	IO	I/O	I/O
AE17	IO	I/O	I/O
AE18	IO	I/O	I/O
AE19	IO	I/O	I/O
AE20	IO	I/O	I/O
AE21	IO	I/O	I/O
AE22	IO	I/O	I/O
AE23	V_{PN}	V_{PN}	V_{PN}
AE24	IO/TRSTB	I/O/TRSTB	I/O/TRSTB
AE25	V_{DDP}	V_{DDP}	V_{DDP}
AE26	V_{DDP}	V_{DDP}	V_{DDP}
AF1	V_{DDP}	V_{DDP}	V_{DDP}
AF2	V_{DDP}	V_{DDP}	V_{DDP}
AF3	NC	I/O	I/O
AF4	NC	I/O	I/O
AF5	IO	I/O	I/O
AF6	NC	I/O	I/O
AF7	NC	I/O	I/O
AF8	IO	I/O	I/O
AF9	NC	I/O	I/O
AF10	NC	I/O	I/O
AF11	IO	I/O	I/O
AF12	NC	I/O	I/O
AF13	NC	I/O	I/O
AF14	IO	I/O	I/O
AF15	NC	I/O	I/O
AF16	NC	I/O	I/O
AF17	IO	I/O	I/O
AF18	NC	I/O	I/O
AF19	NC	I/O	I/O
AF20	IO	I/O	I/O
AF21	NC	I/O	I/O
AF22	IO	I/O	I/O
AF23	IO/TDI	I/O/TDI	I/O/TDI
AF24	NC	I/O	I/O
AF25	V_{DDP}	V_{DDP}	V_{DDP}
AF26	V_{DDP}	V_{DDP}	V_{DDP}
B1	V_{DDP}	V_{DDP}	V_{DDP}
B2	V_{DDP}	V_{DDP}	V_{DDP}
B3	IO	I/O	I/O
B4	IO	I/O	I/O
B5	IO	I/O	I/O
B6	IO	I/O	I/O
B7	IO	I/O	I/O
B8	IO	I/O	I/O
B9	IO	I/O	I/O
B10	IO	I/O	I/O
B11	IO	I/O	I/O
B12	IO	I/O	I/O
B13	IO	I/O	I/O
B14	IO	I/O	I/O
B15	IO	I/O	I/O
B16	IO	I/O	I/O
B17	IO	I/O	I/O
B18	IO	I/O	I/O

Note: *NC = No Connection*

456-Pin PBGA (Continued)

Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
B19	IO	I/O	I/O
B20	IO	I/O	I/O
B21	IO	I/O	I/O
B22	IO	I/O	I/O
B23	IO	I/O	I/O
B24	IO	I/O	I/O
B25	V_{DDP}	V_{DDP}	V_{DDP}
B26	V_{DDP}	V_{DDP}	V_{DDP}
C1	V_{DDP}	V_{DDP}	V_{DDP}
C2	IO	I/O	I/O
C3	V_{DDP}	V_{DDP}	V_{DDP}
C4	IO	I/O	I/O
C5	IO	I/O	I/O
C6	IO	I/O	I/O
C7	IO	I/O	I/O
C8	IO	I/O	I/O
C9	IO	I/O	I/O
C10	IO	I/O	I/O
C11	IO	I/O	I/O
C12	IO	I/O	I/O
C13	IO	I/O	I/O
C14	IO	I/O	I/O
C15	IO	I/O	I/O
C16	IO	I/O	I/O
C17	IO	I/O	I/O
C18	IO	I/O	I/O
C19	IO	I/O	I/O
C20	IO	I/O	I/O
C21	IO	I/O	I/O
C22	IO	I/O	I/O
C23	IO	I/O	I/O
C24	V_{DDP}	V_{DDP}	V_{DDP}
C25	IO	I/O	I/O
C26	NC	I/O	I/O
D1	NC	I/O	I/O
D2	IO	I/O	I/O
D3	IO	I/O	I/O
D4	V_{DDP}	V_{DDP}	V_{DDP}
D5	IO	I/O	I/O
D6	IO	I/O	I/O
D7	IO	I/O	I/O
D8	IO	I/O	I/O
D9	IO	I/O	I/O
D10	IO	I/O	I/O
D11	IO	I/O	I/O
D12	IO	I/O	I/O

Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
D13	IO	I/O	I/O
D14	IO	I/O	I/O
D15	IO	I/O	I/O
D16	IO	I/O	I/O
D17	IO	I/O	I/O
D18	IO	I/O	I/O
D19	IO	I/O	I/O
D20	IO	I/O	I/O
D21	IO	I/O	I/O
D22	IO	I/O	I/O
D23	V_{DDP}	V_{DDP}	V_{DDP}
D24	IO	I/O	I/O
D25	IO	I/O	I/O
D26	IO	I/O	I/O
E1	NC	I/O	I/O
E2	IO	I/O	I/O
E3	IO	I/O	I/O
E4	IO	I/O	I/O
E5	V_{DDL}	V_{DDL}	V_{DDL}
E6	V_{DDL}	V_{DDL}	V_{DDL}
E7	V_{DDL}	V_{DDL}	V_{DDL}
E8	V_{DDL}	V_{DDL}	V_{DDL}
E9	IO	I/O	I/O
E10	IO	I/O	I/O
E11	IO	I/O	I/O
E12	IO	I/O	I/O
E13	IO	I/O	I/O
E14	IO	I/O	I/O
E15	IO	I/O	I/O
E16	IO	I/O	I/O
E17	IO	I/O	I/O
E18	IO	I/O	I/O
E19	IO	I/O	I/O
E20	V_{DDL}	V_{DDL}	V_{DDL}
E21	V_{DDL}	V_{DDL}	V_{DDL}
E22	V_{DDL}	V_{DDL}	V_{DDL}
E23	IO	I/O	I/O
E24	IO	I/O	I/O
E25	IO	I/O	I/O
E26	IO	I/O	I/O
F1	IO	I/O	I/O
F2	IO	I/O	I/O
F3	IO	I/O	I/O
F4	IO	I/O	I/O
F5	V_{DDL}	V_{DDL}	V_{DDL}
F22	V_{DDL}	V_{DDL}	V_{DDL}

Note: *NC = No Connection*

456-Pin PBGA (Continued)

Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
F23	IO	I/O	I/O
F24	IO	I/O	I/O
F25	IO	I/O	I/O
F26	NC	I/O	I/O
G1	NC	I/O	I/O
G2	IO	I/O	I/O
G3	IO	I/O	I/O
G4	IO	I/O	I/O
G5	V_{DDL}	V_{DDL}	V_{DDL}
G22	V_{DDL}	V_{DDL}	V_{DDL}
G23	IO	I/O	I/O
G24	IO	I/O	I/O
G25	IO	I/O	I/O
G26	IO	I/O	I/O
H1	NC	I/O	I/O
H2	IO	I/O	I/O
H3	IO	I/O	I/O
H4	IO	I/O	I/O
H5	V_{DDL}	V_{DDL}	V_{DDL}
H22	V_{DDL}	V_{DDL}	V_{DDL}
H23	IO	I/O	I/O
H24	IO	I/O	I/O
H25	IO	I/O	I/O
H26	NC	I/O	I/O
J1	IO	I/O	I/O
J2	IO	I/O	I/O
J3	IO	I/O	I/O
J4	IO	I/O	I/O
J5	IO	I/O	I/O
J22	IO	I/O	I/O
J23	IO	I/O	I/O
J24	IO	I/O	I/O
J25	IO	I/O	I/O
J26	NC	I/O	I/O
K1	NC	I/O	I/O
K2	IO	I/O	I/O
K3	IO	I/O	I/O
K4	IO	I/O	I/O
K5	IO	I/O	I/O
K22	IO	I/O	I/O
K23	IO	I/O	I/O
K24	IO	I/O	I/O
K25	IO	I/O	I/O
K26	IO	I/O	I/O
L1	NC	I/O	I/O
L2	IO	I/O	I/O
L3	IO	I/O	I/O
L4	IO	I/O	I/O
L5	IO	I/O	I/O
L11	GND	GND	GND
L12	GND	GND	GND
L13	GND	GND	GND
L14	GND	GND	GND
L15	GND	GND	GND
L16	GND	GND	GND
L22	IO	I/O	I/O
L23	IO	I/O	I/O
L24	IO	I/O	I/O
L25	IO	I/O	I/O
L26	NC	I/O	I/O
M1	G2	G1	G1
M2	G1	G0	G0
M3	IO	I/O	I/O
M4	IO	I/O	I/O
M5	IO	I/O	I/O
M11	GND	GND	GND
M12	GND	GND	GND
M13	GND	GND	GND
M14	GND	GND	GND
M15	GND	GND	GND
M16	GND	GND	GND
M22	G4	G3	G3
M23	IO	I/O	I/O
M24	IO	I/O	I/O
M25	IO	I/O	I/O
M26	NC	I/O	I/O
N1	NC	I/O	I/O
N2	IO	I/O	I/O
N3	IO	I/O	I/O
N4	IO	I/O	I/O
N5	IO	I/O	I/O
N11	GND	GND	GND
N12	GND	GND	GND
N13	GND	GND	GND
N14	GND	GND	GND
N15	GND	GND	GND
N16	GND	GND	GND
N22	IO	I/O	I/O
N23	G3	G2	G2
N24	IO	I/O	I/O
N25	IO	I/O	I/O
N26	IO	I/O	I/O

Note: *NC = No Connection*

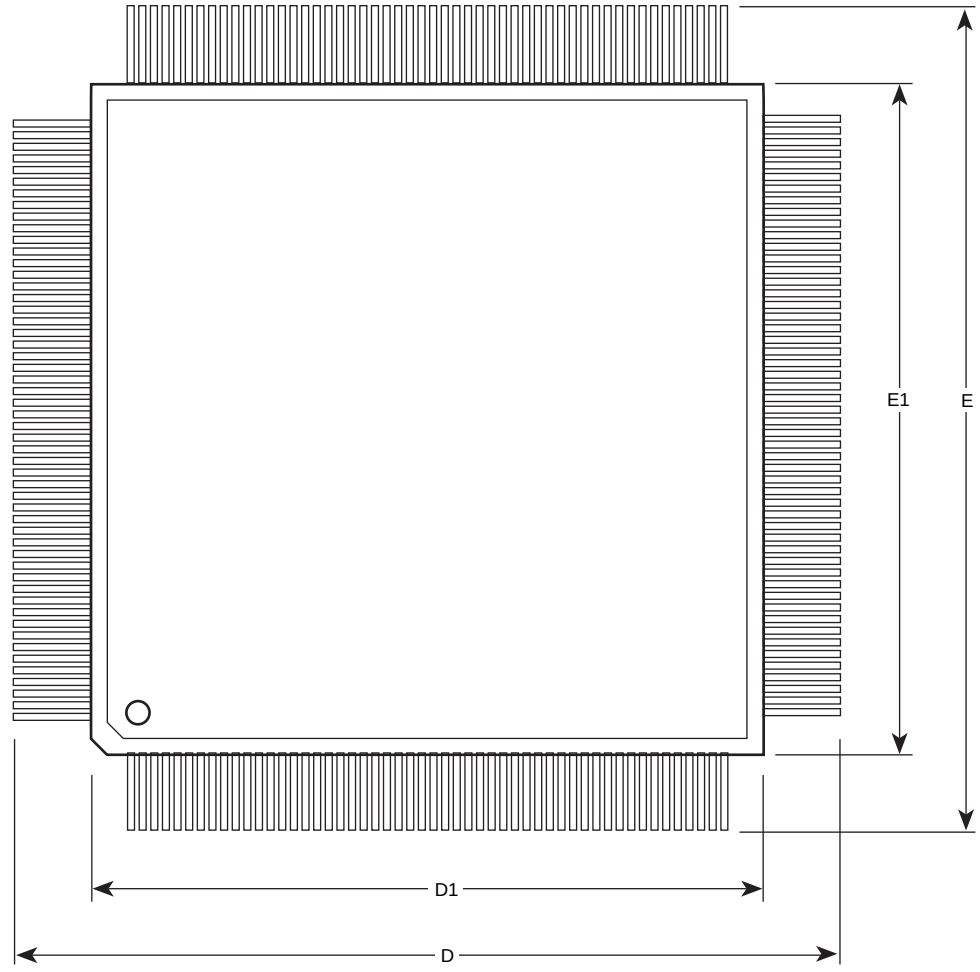
456-Pin PBGA (Continued)

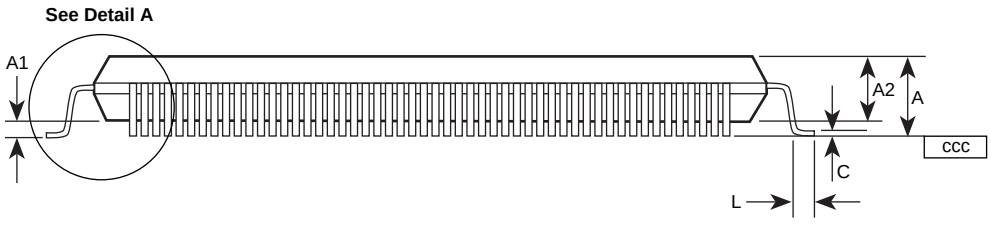
Ext. Ball	A500K130 Function	A500K180 Function	A500K270 Function
P1	NC	I/O	I/O
P2	IO	I/O	I/O
P3	IO	I/O	I/O
P4	IO	I/O	I/O
P5	IO	I/O	I/O
P11	GND	GND	GND
P12	GND	GND	GND
P13	GND	GND	GND
P14	GND	GND	GND
P15	GND	GND	GND
P16	GND	GND	GND
P22	IO	I/O	I/O
P23	IO	I/O	I/O
P24	IO	I/O	I/O
P25	IO	I/O	I/O
P26	NC	I/O	I/O
R1	IO	I/O	I/O
R2	IO	I/O	I/O
R3	IO	I/O	I/O
R4	IO	I/O	I/O
R5	IO	I/O	I/O
R11	GND	GND	GND
R12	GND	GND	GND
R13	GND	GND	GND
R14	GND	GND	GND
R15	GND	GND	GND
R16	GND	GND	GND
R22	IO	I/O	I/O
R23	IO	I/O	I/O
R24	IO	I/O	I/O
R25	IO	I/O	I/O
R26	NC	I/O	I/O
T1	NC	I/O	I/O
T2	IO	I/O	I/O
T3	IO	I/O	I/O
T4	IO	I/O	I/O
T5	IO	I/O	I/O
T11	GND	GND	GND
T12	GND	GND	GND
T13	GND	GND	GND
T14	GND	GND	GND
T15	GND	GND	GND
T16	GND	GND	GND
T22	IO	I/O	I/O
T23	IO	I/O	I/O
T24	IO	I/O	I/O
T25	IO	I/O	I/O
T26	IO	I/O	I/O
U1	NC	I/O	I/O
U2	IO	I/O	I/O
U3	IO	I/O	I/O
U4	IO	I/O	I/O
U5	IO	I/O	I/O
U22	IO	I/O	I/O
U23	IO	I/O	I/O
U24	IO	I/O	I/O
U25	IO	I/O	I/O
U26	NC	I/O	I/O
V1	IO	I/O	I/O
V2	IO	I/O	I/O
V3	IO	I/O	I/O
V4	IO	I/O	I/O
V5	IO	I/O	I/O
V22	IO	I/O	I/O
V23	IO	I/O	I/O
V24	IO	I/O	I/O
V25	IO	I/O	I/O
V26	NC	I/O	I/O
W1	NC	I/O	I/O
W2	IO	I/O	I/O
W3	IO	I/O	I/O
W4	IO	I/O	I/O
W5	V_{DDL}	V_{DDL}	V_{DDL}
W22	V_{DDL}	V_{DDL}	V_{DDL}
W23	IO	I/O	I/O
W24	IO	I/O	I/O
W25	IO	I/O	I/O
W26	IO	I/O	I/O
Y1	NC	I/O	I/O
Y2	IO	I/O	I/O
Y3	IO	I/O	I/O
Y4	IO	I/O	I/O
Y5	V_{DDL}	V_{DDL}	V_{DDL}
Y22	V_{DDL}	V_{DDL}	V_{DDL}
Y23	IO	I/O	I/O
Y24	IO	I/O	I/O
Y25	IO	I/O	I/O
Y26	NC	I/O	I/O

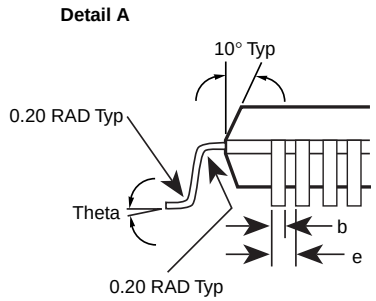
Note: *NC = No Connection*

Package Mechanical Drawings

208-Pin PQFP







Plastic Quad Flat Packages (PQFP)

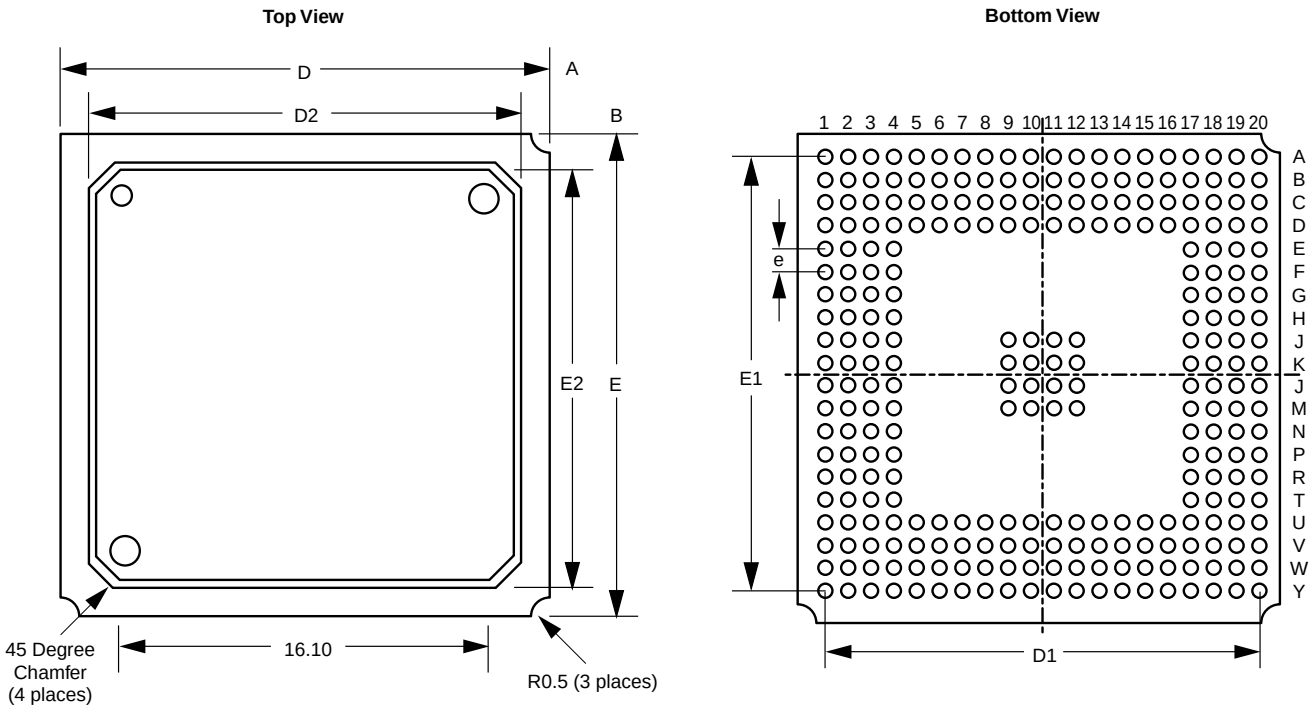
Jedec Equiv	PQFP 208 MO-143		
Dimension	**Min.**	**Nom.**	**Max.**
A		3.70	4.10
A1	0.25	0.38	
A2	3.20	3.40	3.60
b	0.17		0.27
c	0.09		0.20
ccc			0.10
D/E	30.25	30.60	30.85
D1/E1	27.90	28.00	28.10
e	0.50 BSC		
L	0.50	0.60	0.75
Theta	0		7 deg
Diameter	19.82	20.32	20.82

Notes:

1. *All dimensions are in millimeters.*
2. *BSC – Basic Spacing between Centers.*

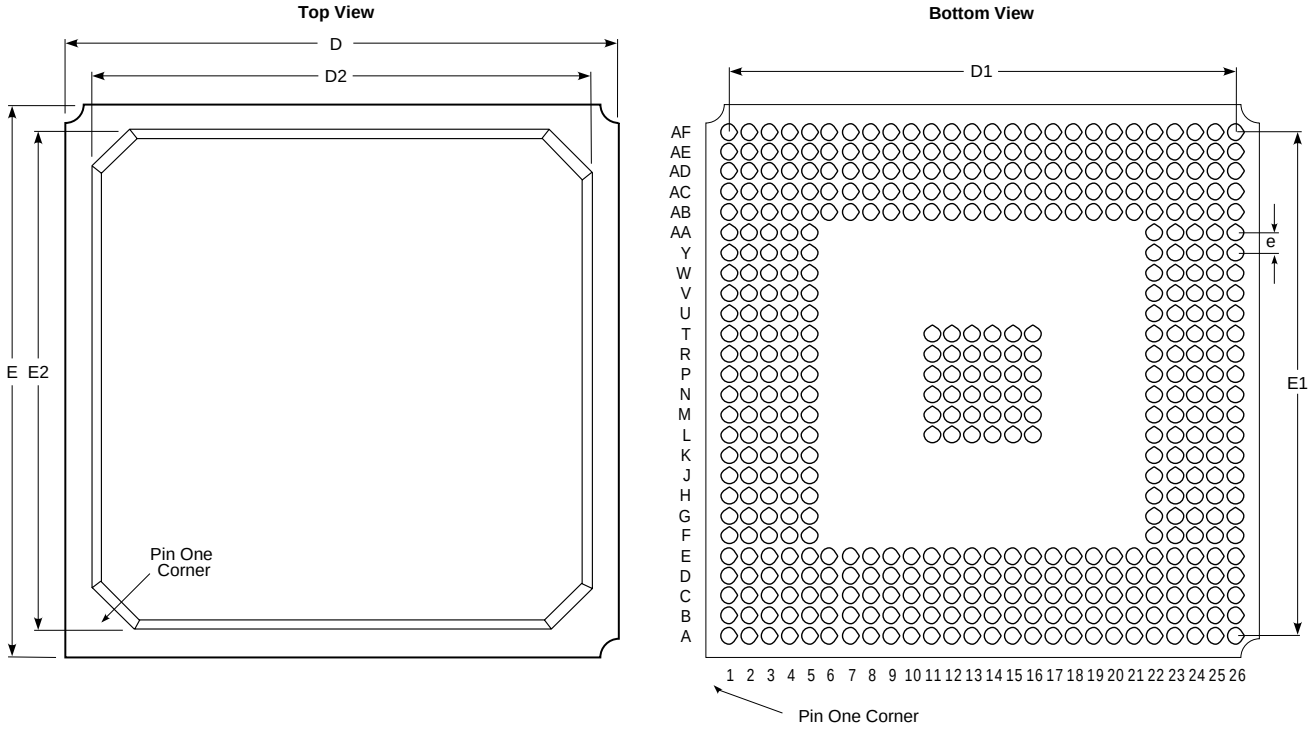
Package Mechanical Drawings (Continued)

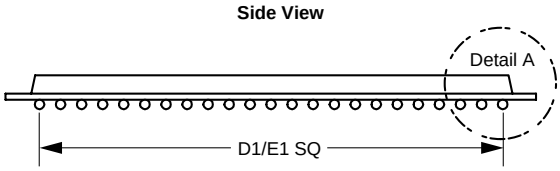
272-Pin PBGA

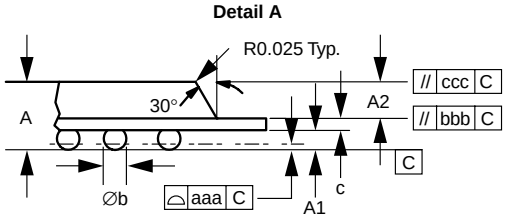


Package Mechanical Drawings (Continued)

456-Pin PBGA







Plastic Ball Grid Array (PBGA)

JEDEC Equivalent	PBGA272			PBGA456		
Dimension	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	2.18	2.33	2.50	2.20	2.33	2.50
A1	0.50	0.60	0.70	0.50	0.60	0.70
A2	1.15	1.17	1.19	1.12	1.17	1.19
aaa			0.15			0.15
bbb			0.20			0.20
b	0.60	0.75	0.90	0.60	0.75	0.90
c	0.53	0.56	0.61	0.51	0.56	0.61
ccc			0.25			0.25
D	26.80	27.00	27.20	34.80	35.00	35.20
D1	24.13 BSC			31.75 BSC		
D2	23.90	24.00	24.10	29.80	30.00	30.20
E	26.80	27.00	27.20	34.80	35.00	35.20
E1	24.13 BSC			31.075 BSC		
E2	23.90	24.00	24.10	29.80	30.00	30.20
e	1.27 typ.			1.27 typ.		
Theta	30° typ.			30° typ.		

Notes:

1. *All dimensions are in millimeters*
2. *BSC – Basic Spacing between Centers*

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