MultiView Navigator v6.1 User's Guide

NetlistViewer

PinEditor

I/O Attribute Editor

ChipPlanner

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Table of Contents

Welcome to MultiView Navigator (MVN)

MultiView Navigator is the physical design viewing and editing interface for the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families. With this interface, you can view, edit, and floorplan your design in many different views. Its four tools also include powerful find and undo/redo features as well as cross-probing features:

- NetlistViewer generates a schematic view of your design.
- PinEditor displays a view of the I/O macros assigned to the pins in your design.
- I/O Attribute Editor displays a table of the I/O attributes in your design.
- ChipPlanner displays a view of the I/O and logic macros in your design.

You can view your design in all of these tools at the same time. From within MultiView Navigator, simply select a tool from the Tools menu, or click its toolbar button.

Note: The MultiView Navigator tools also work with Timer and SmartPower.

Starting MultiView Navigator

You must compile your design before using NetlistViewer, ChipPlanner, PinEditor, or I/O Attribute Editor in MultiView Navigator.

To start MultiView Navigator from Designer:

1. Compile your design.
2. Click one of the following tools: **NetlistViewer**, **PinEditor**, **ChipPlanner**, or **I/O Attribute Editor**. If you have not compiled your design, Designer compiles it for you before opening your selected tool.

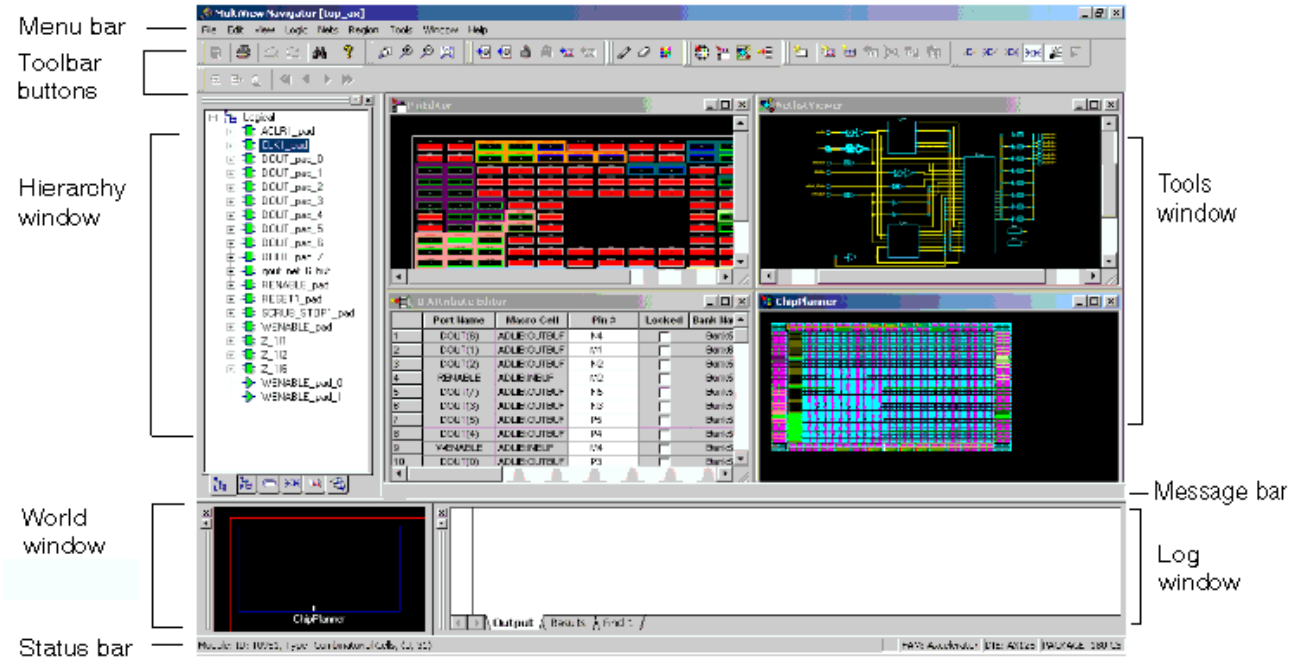
MultiView Navigator reads your design and opens it in the tool you selected.

Components of the MultiView Navigator Interface

The MultiView Navigator interface is divided into four windows:

- Hierarchy window
- Tools window
- World window
- Log window

In addition, this interface includes a menu bar, toolbar buttons, a message bar, and a status bar.



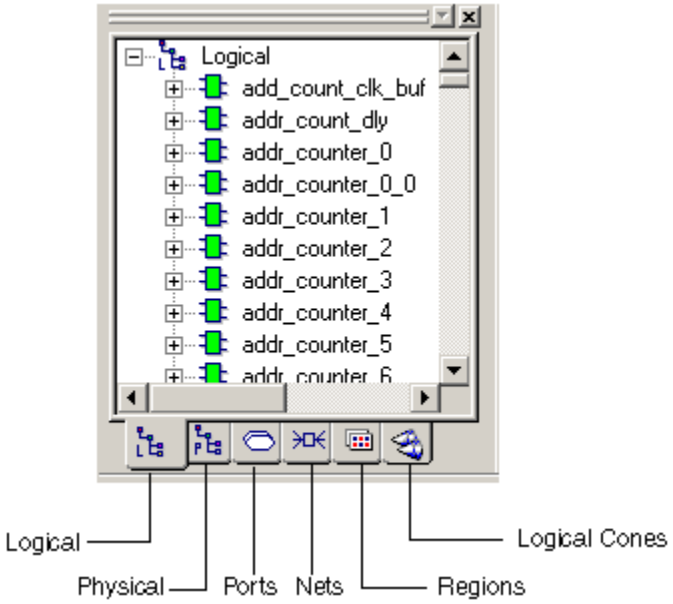
MultiView Navigator Interface

Use the menus or toolbar buttons to initiate commands.

Overview of Hierarchy Window

The leftmost window in MultiView Navigator is the Hierarchy window. The Logical tab in this window provides a hierarchical overview of the design.

Click the tabs at the bottom of this window to view macros, instances, ports, nets, regions, and logical cones in your design.



Hierarchy Window

Use these tabs to explore each level of the hierarchy and to trace signals. You use the Hierarchy window tabs with ChipPlanner, NetlistViewer, PinEditor, and I/O Attribute Editor to help identify critical paths.

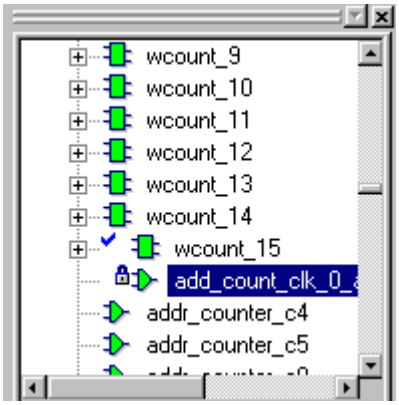
Tip: Right-click an object to use its context-sensitive menu.

In all Hierarchy views, you can right-click an object, and select **Properties** to display its properties.

Each view contains color-coded icons to indicate its logic type and state. These icons are explained in the following table:

Icon(s)	Color	What it Represents
	White	The logic or I/O is unassigned.
	Green	The logic or I/O is assigned.
	Hashed green	Some instances in the block of logic are assigned.
	Red and blue grid	The region is either inclusive or LocalClock.
	Blue grid	The region is exclusive.
	White	The region is empty.
	Cone icon	The object is a Logical Cone.
	Blue checkmark	The logic is assigned to a region.
	Gray checkmark	Some instances in the block of logic are assigned to a region.
	Blue lock	The entire block of assigned logic is locked to a location.
	Gray lock	Some instances in the block of assigned logic are locked to a location.

The Logical tab shown below illustrates that the selected logic is assigned to a region and locked. Only the Logical tab shows the logical design hierarchy. The Physical tab shows the physical hierarchy. The other tabs are not hierarchical.



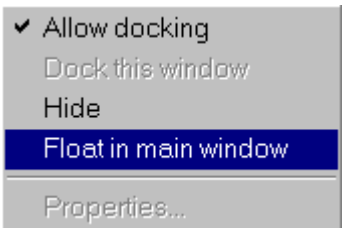
Logical Tab - Checkmark and Lock Icons

Floating and Docking Windows

You can rearrange or hide the Hierarchy window, World window, and Log window within MultiView Navigator. These windows are referred to as “floating” because you can move them within the Tools window. You can also “dock” or anchor them in place.

To move a window:

1. Select the window to move.
2. Right-click anywhere on the window except on a macro or within the display area of the Log window, and then choose **Float in main window** from the right-click menu.
3. Click and drag the title bar of the window to its new location.
4. Release the mouse button.



To return the floating window to its docked location:

1. Select the floating window to dock.
2. Right-click and choose **Dock this window** from the right-click menu. To dock the Log window, unselect **Float in main window** from the right-click menu.

The window returns to its original location in the MultiView Navigator interface.

Tip: You can also dock and undock a floating window by double-clicking the window frame.

To hide a window:

1. Select the window to hide.
2. Right-click and choose **Hide** from the right-click menu.

To show a hidden window:

1. From the **View** menu, choose **Windows.**
2. Select the name of the window to display (Hierarchy Window, Log Window, or World Window).

Selecting Objects

Before you can highlight, assign, unassign, configure, or otherwise manipulate an object, you must first select it by clicking it.

From the Hierarchy window, you can also select groups of objects. The procedure for selecting more than one object in the Tools window depends on which tool you are using. See the documentation for your tool.

To select a group of objects in the Hierarchy window:

- To select consecutive objects, click the first object, press and hold down **SHIFT**, and then click the last object.
- To select objects that are not consecutive, press and hold down **CTRL**, and then click each object.
- To select all objects in the design, from the **Edit** menu, choose **Select All**.

To unselect specific selected objects:

- To unselect one or more consecutive objects, press and hold down **SHIFT**, and then click the last object to include in the selection. The objects below it are unselected.
- To unselect objects that are not consecutive, press and hold down **CTRL**, and then click each object to unselect.

To unselect all selected objects:

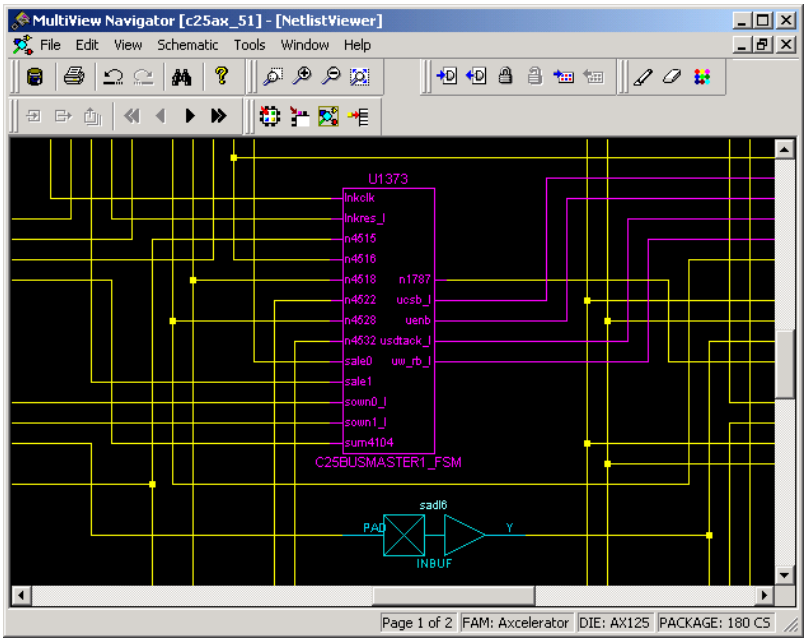
- Click on a clear spot in either the **Hierarchy** or **Tools** window.

Highlighting and Unhighlighting Objects

Highlight objects or groups of objects for easy reference. You can change the default highlight color.

To highlight an object:

1. Select the object to highlight in the **Tools** window.
2. From the **Edit** menu, choose **Highlight**, or click the **Highlight** toolbar button. The color of the object changes to the default highlight color. In the following illustration, the objects are highlighted in magenta.



Objects Highlighted in Magenta

To highlight a group of objects:

Highlighting a group of objects is useful for tracing a net.

1. From the **Edit** menu, choose **Highlight**, or click the **Highlight** toolbar button. The cursor turns into a pen icon.
2. Press and hold down the **CTRL** key, and then click each object to highlight.

To unhighlight a group of objects:

1. Select the highlighted group of objects.
2. From the **Edit** menu, choose **Unhighlight All**, or click its equivalent toolbar button.

Changing the Highlight Color

To change the highlight color:

1. From the **Edit** menu, choose **Highlight Color.**
2. Select the new highlight color from the **Color palette** that appears.
3. Click **OK**.

All objects that you choose to highlight will appear in the new highlight color. However, objects previously highlighted will not change to the new color.

Using the Prelayout Checker

The Prelayout Checker is a feature that checks your design for possible error conditions before you place and route it. Prelayout checks are a subset of the Design Rule Check (DRC). If the Prelayout Checker finds potential errors, it displays warning and error messages in MultiView Navigator's Log window.

To run the Prelayout Checker, from the **Tools** menu, choose **DRC**.

Selecting DRC performs the following checks:

- Validates common macros in overlapping regions against the overlap capacity
- Checks placement of I/O banks against the banks' voltage settings

When you choose **Commit** from the **File** menu in the MultiView Navigator, it automatically performs comprehensive checking in addition to committing the changes to your design.

Note: DRC stands for Design Rule Check. Use the DRC command to check for errors before you use the Layout command.

NetlistViewer in MultiView Navigator

The NetlistViewer tool displays the contents of the design as a schematic, making it easier for you to debug. Use NetlistViewer to view nets, ports, and instances in the schematic view. You can start NetlistViewer only after the design is compiled.

Note: This version of NetlistViewer supports only the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families. If you are designing for the MX, SX-A, eX, RTSX, or RTSX-S families, use the standalone version of NetlistViewer.

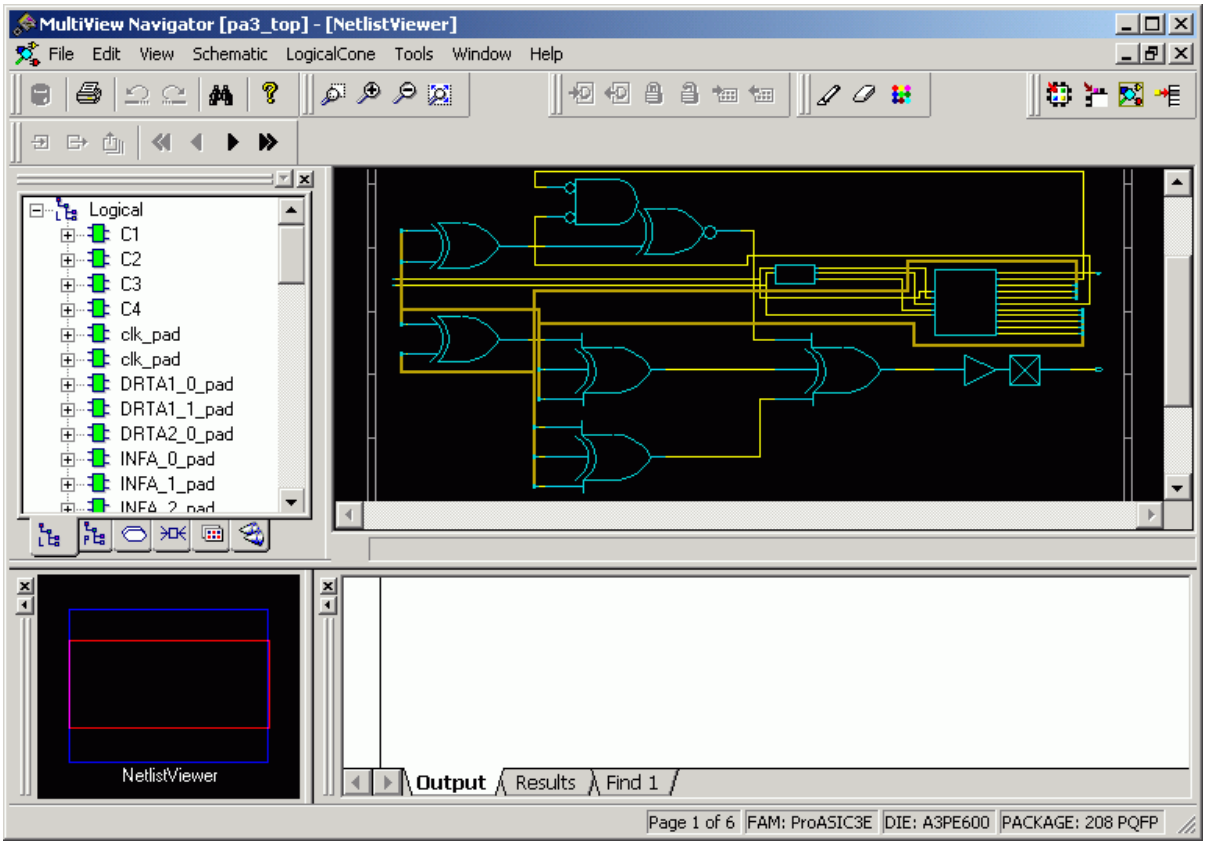
Starting NetlistViewer in MultiView Navigator

NetlistViewer requires a compiled design. If you start NetlistViewer before compiling your design, Designer guides you through the compile process before opening NetlistViewer.

To start NetlistViewer from Designer, either click the **NetlistViewer** icon in the Designer Design Flow window, or from the **Tools** menu, choose **NetlistViewer**.

To start NetlistViewer from within MVN, either click the **NetlistViewer** button in the MVN toolbar, or from the **Tools** menu, choose **NetlistViewer**.

NetlistViewer opens in the Tools window of MultiView Navigator. After reading your netlist design, NetlistViewer generates a clearly laid out schematic view, as shown here.



NetlistViewer in MultiView Navigator

Viewing Your Netlist

The NetlistViewer window displays your netlist in graphical format. When you open a ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, or ProASIC design, and click **NetlistViewer**, it automatically starts MultiView Navigator and displays your design in the NetlistViewer window.

To view your netlist using NetlistViewer:

- After NetlistViewer starts and displays your netlist in MultiView Navigator, you can view the optimized flattened netlist or the pre-optimized hierarchical netlist.
- The optimized flattened netlist is a non-hierarchical view. Use the optimized flattened netlist with Axcelerator when cross-probing with other tools, such as PinEditor or ChipPlanner.
- The pre-optimized netlist is your original netlist, as passed to the Designer software. The hierarchical structure is useful for navigating. The pre-optimized netlist is the default.

To switch between views, from the **Schematic** menu, click **Show Pre-optimized Netlist** or **Show Optimized Netlist**.

Bundling Nets

A netBundle is a group of nets with names that have the same pattern. For example, nets with names such as **N_357_0**, **N_357_1**, and **N_357** are bundled together as are **crc_100_**, **crc_200_**, and **crc_300_**.

A netBundle represents all nets in the group as a bus. In NetlistViewer, lines representing netBundles are brown and thicker than single nets. NetlistViewer automatically generates netBundles whenever possible. You cannot create, expand, or unbundle a netBundle.

Nets are bundled into a netBundle if the net names match one of the following patterns:

```
*(..)
*[..]
*{..}
*<..>
*_..._
*_..
```

where "*" stands for any character string and ". ." must consist of digits only.

Note: Pins are connected to the net, not the netBundle.

Navigating Through Your Netlist

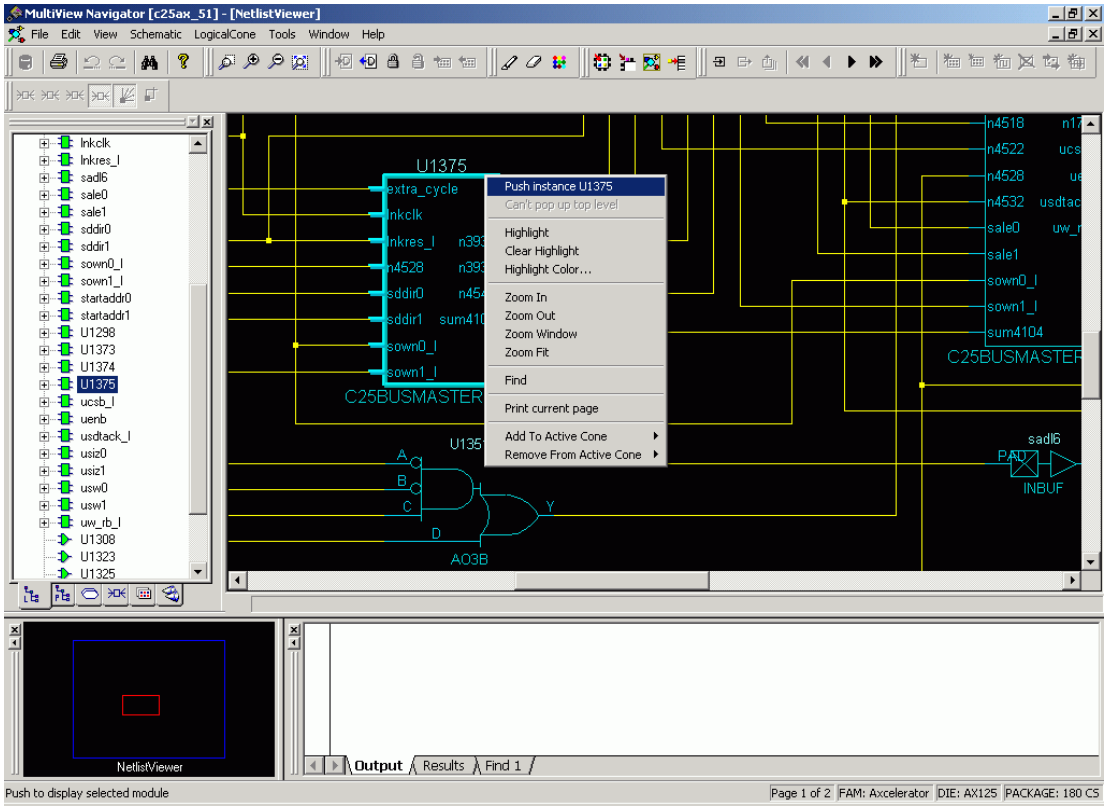
You can navigate in the logical view of the design vertically and horizontally.

Vertical Navigation

Navigate vertically through your hierarchical design using the **Push**, **Pop**, and **Top** commands. These commands are available from the **Schematic** menu, the right-click menu, and the toolbar.

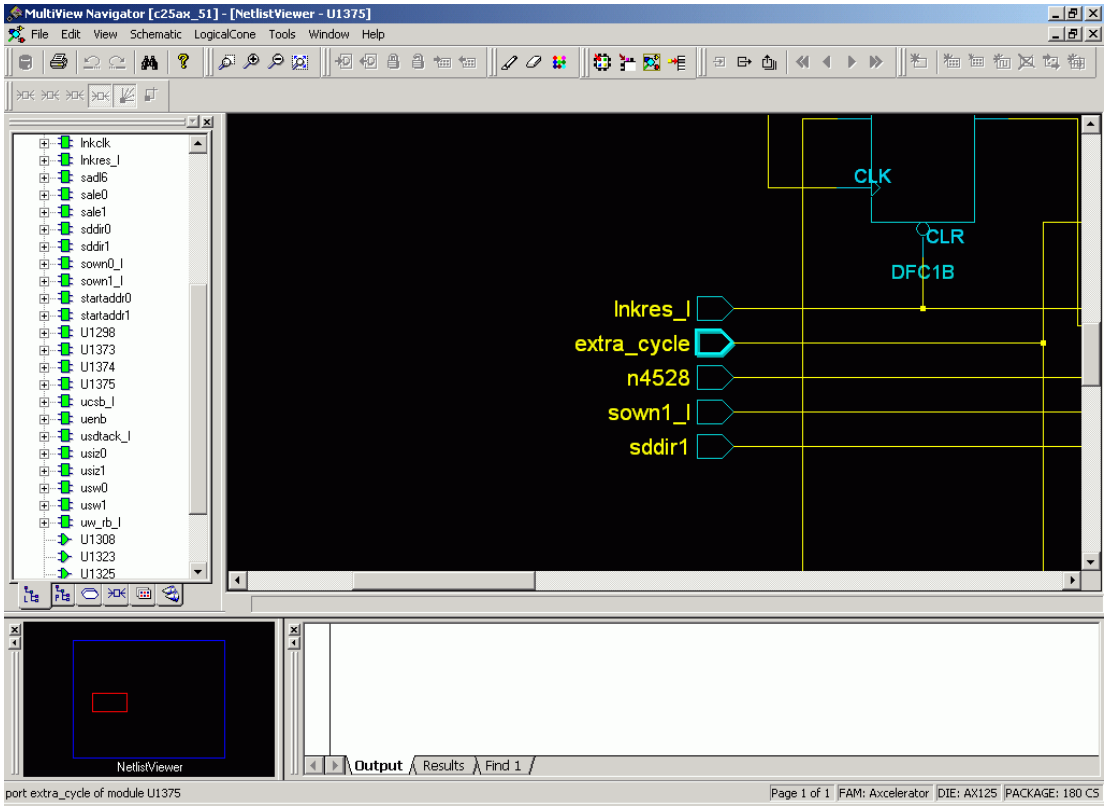
To go one level deeper in a design:

1. Select an instance.
2. From the **Schematic** menu, choose **Push**, or from the right-click menu, choose **Push instance <name of instance>.**



Pushing Instance U1375

You can also select one pin of an instance, and then choose **Push** to move the focus to that pin. NetlistViewer centers on the port corresponding to the pin you selected. In the following illustration, the focus is on the pin labeled "extra_cycle" because only that pin was selected when the **Push** command was executed.



Following the Net

To go one level higher in a design, either from the **Schematic** menu, choose **Pop**, or click the **Pop** toolbar button. You can also select a port and click **Pop** to go up one level and center on the pin of the port you selected.

To go to the top level, either from the **Schematic** menu, choose **Top**, or click the **Top** toolbar button.

Horizontal Navigation

When large designs do not fit in the Schematic View window, NetlistViewer splits the design into multiple pages. Page splitting enables you to quickly compute and display the schematic. You can also turn off page splitting to view your entire design on a single page. For larger designs, when this option is turned off, it may take NetlistViewer significantly longer to display the schematic. To turn page splitting on or off, from the **Schematic** menu, choose **Allow Page Splitting**.

To navigate to the next page in a design, from the **Schematic** Menu, choose **Go to Next Page**, or click the **Next Page** button in the toolbar.

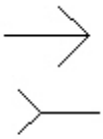
To navigate to the previous page, from the **Schematic** Menu, choose **Go to Previous Page**, or click the **Previous Page** button in the toolbar.

To navigate to the first page, from the **Schematic** menu, choose **Go to First Page**, or click the **First Page** toolbar button.

To navigate to the last page, from the **Schematic** menu, choose **Go to Last Page**, or click the **Last Page** toolbar button.

Following Nets

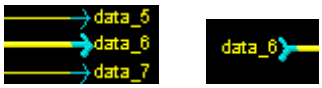
Following a net might take you to another page or another level in your design. Following nets is useful when your design is split into several pages or if it includes some hierarchical logic. Nets that continue on other pages are terminated by a page connector symbol (>). Note that a net can continue on many pages.



Indicates the net ends on another page

Indicates the net begins on another page

The illustrations below show two pages that include the pin labeled "net data_6." On both pages, the net ends with the page connector symbol (>), indicating the net continues on another page. As stated earlier, the net can continue on many pages.

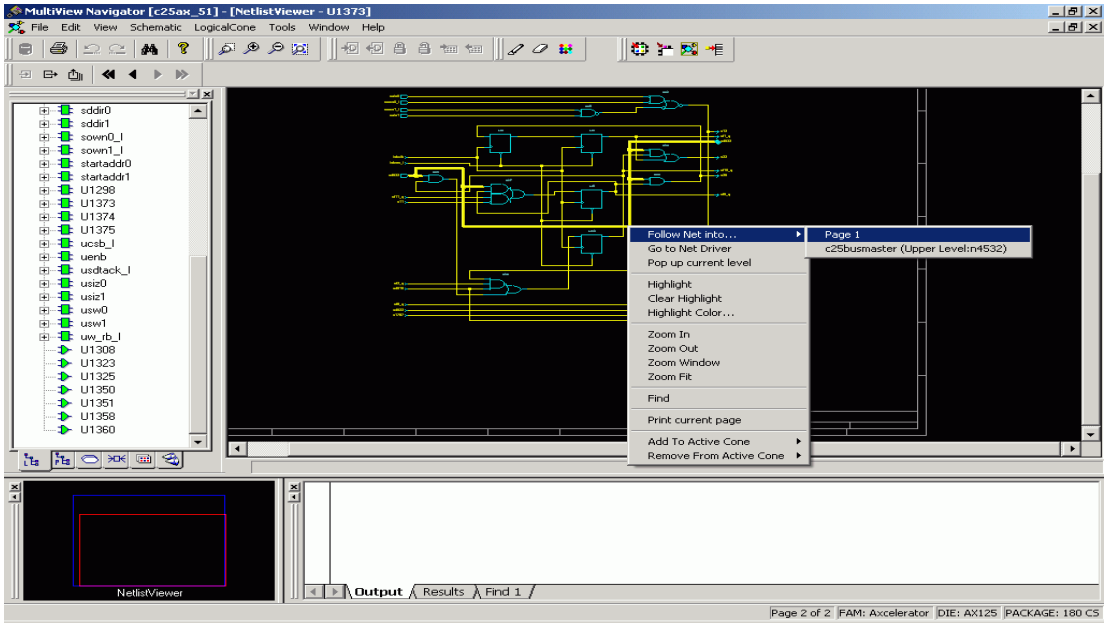


Symbols for a Continuing Net

Nets that cross a hierarchical boundary are inside a hierarchical instance and connected to a port of the instance or those connected to a pin of a hierarchical instance.

To follow a net:

1. Select a net in NetlistViewer.
2. From either the **Schematic menu** or right-click menu, choose **Follow Net Into**. NetlistViewer displays a list of all pages or modules to which your net is connected. Choose one item in the list. If the item you chose is a page, NetlistViewer displays the corresponding page and centers to the page connector (the -> or >- symbol ending a split net) ending the selected net. If you chose an instance, NetlistViewer does the corresponding Push or Pop operation to display it, and selects the net connected to the one initially selected.



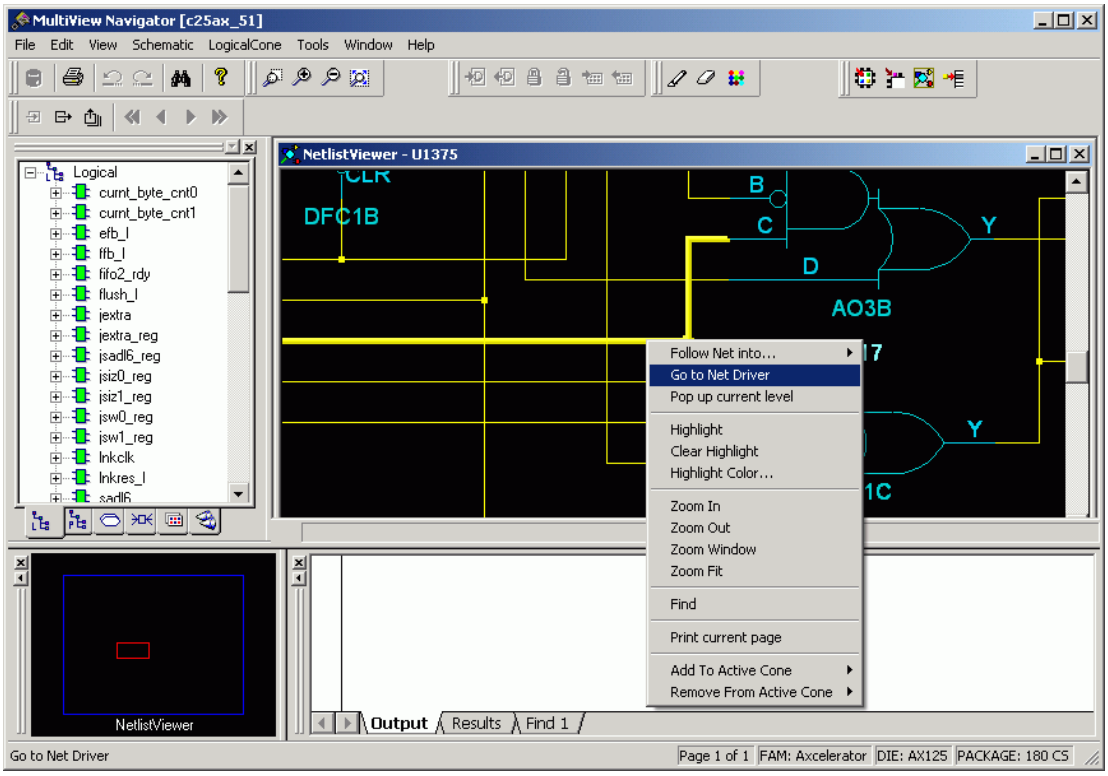
Page and Instance Option

Center to Net Driver

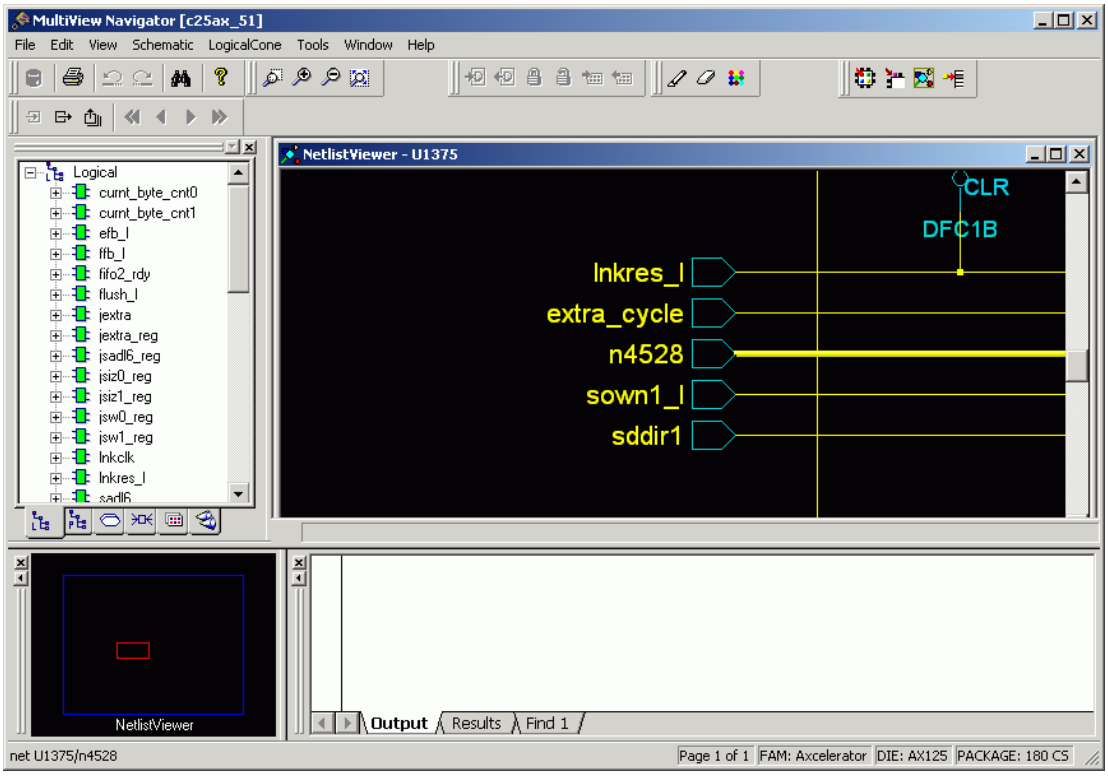
This feature allows you to easily retrieve the driver of a net.

To go to the net driver:

1. Select a net.
2. Right-click a net and choose **Go to Net Driver** from the right-click menu. NetlistViewer displays the pin or port centered in the appropriate page.



Go to Net Window



Net Driver

Selecting Objects in NetlistViewer

Before you can highlight an object, you must first select it. Selecting objects in NetlistViewer is similar to selecting objects in other MultiView Navigator tools. The main difference is that you use the **SHIFT** key instead of the **CTRL** key when selecting and unselecting more than one object in NetlistViewer.

To select a group of objects in the NetlistViewer window:

1. Click an object.
2. Press and hold down the **SHIFT** key while you click each object to select.

To unselect specific selected objects:

- Press and hold down the **SHIFT** key, and then click on a selected object to unselect it. You can also hold down the left mouse button and drag and draw a rectangle toward the bottom-right corner. Release the mouse button when all items you want to unselect are included in the rectangle.

To unselect all selected objects:

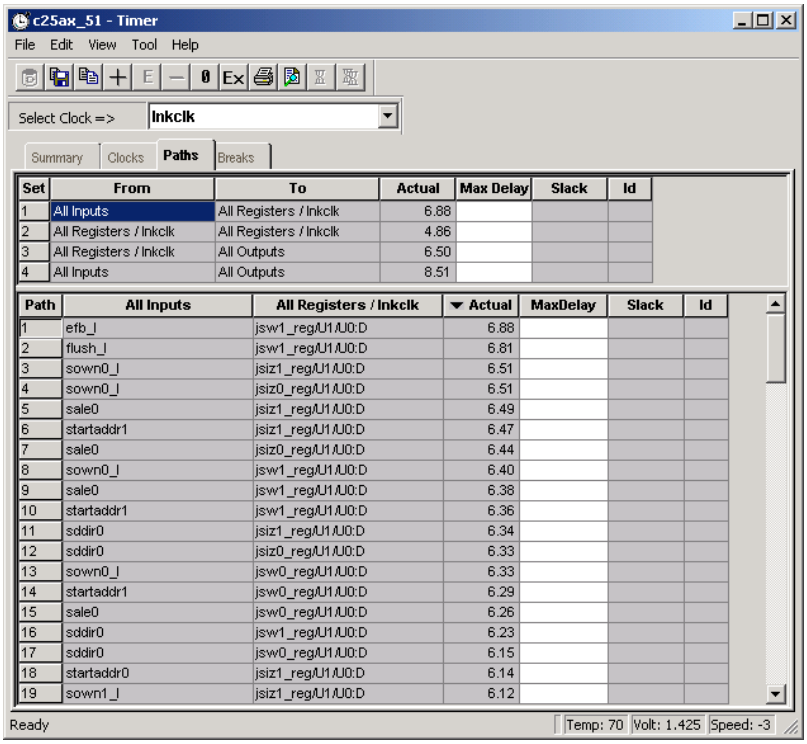
- Click a clear spot within NetlistViewer to unselect all objects.

Identifying Paths

You can use NetlistViewer with Timer to identify the inputs of combinational gates. For more information about Timer, see the *Timer User's Guide*.

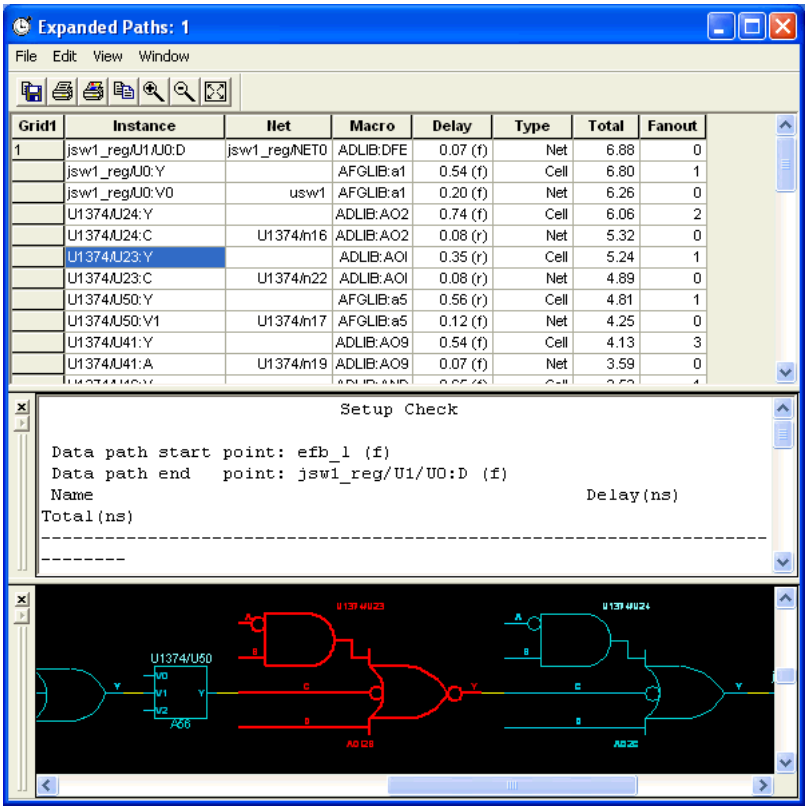
To identify paths:

1. In the **Design Flow** window, click **NetlistViewer** to display your netlist, and then click **Timer**.
2. In the **Timer** window, click the **Paths** tab. The **Paths** tab displays timing analysis information for several categories of paths, known as "sets," in the **Path Set** window. When you select a set in the **Path Set** window, the paths within that set are displayed in the lower table.



Timer's Paths Tab

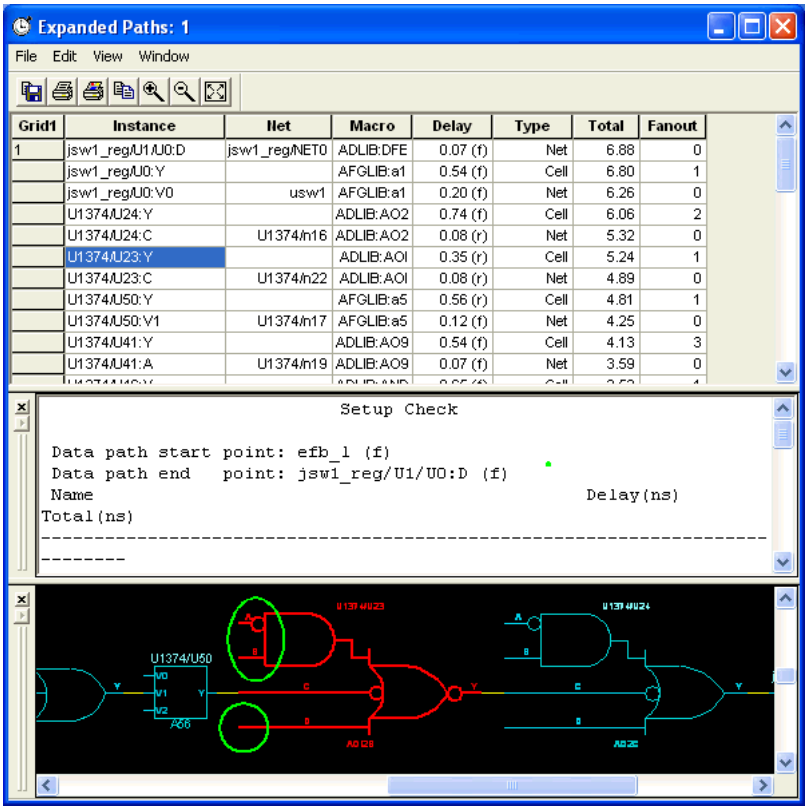
3. Select a path. Timer displays the paths within that set in the lower table.
4. Double-click a path (in the lower paths table) to see a graphical representation of it. The **Expanded Paths** window opens.



Expanding the Path

The **Expanded Paths** window displays a path in the **Expanded Paths** table and a graphical representation of the path in the **Graph** window. Notice that the inputs of combinational gates are not displayed in the **Graph** window.

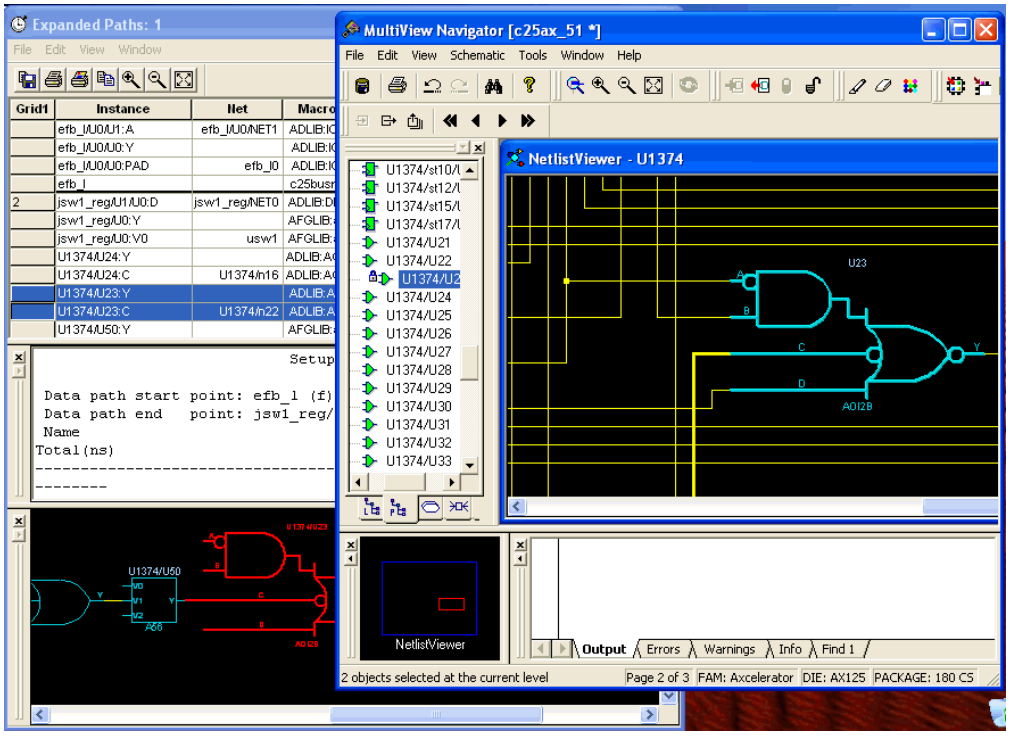
You can create a **Logical Cone** window to view a specific path. A logical cone is a view of a specific part of your design. See "Managing Logical Cones" and "Creating a Logical Cone" in this guide.



Combinational Gates in Timer's Expanded Paths Window

It is useful to know where these paths come from because they might indicate a false path that is never encountered and can affect the timing report. It is also important to know how other inputs to these macros interact with the indicated path, because this helps you define appropriate paths, which are essential for obtaining accurate timing reports.

5. Select the macro in the **Graph** window. The macro is located and selected in the NetlistViewer.



Selected Macro is Located and Selected in the NetlistViewer

Managing Logical Cones

A logical cone is a window that displays only a portion of a netlist. You create this window in NetlistViewer and simply select the objects that you want to appear in this separate view. You can add individual instances, blocks, and ports to a logical cone. You can also remove objects from this cone.

Logical cones help you navigate and analyze a specific part of the design. A Logical Cone view is very similar to the NetlistViewer view. The main differences between the Logical Cone and NetlistViewer views are:

- In a logical cone, you see only the pieces of the design that you want to focus on (for example, path analysis), whereas in NetlistViewer, you see the entire netlist.
- In a logical cone, a net appears as a dashed line unless all instances that are connected to that net in the netlist are also present in the Logical Cone view. These nets are designated as partially connected, as opposed to fully connected nets.
- In a logical cone, all objects of the netlist appear on a single sheet, with hierarchical boundaries still visible. This is a trade-off between the classical hierarchical view, where you must use Push and Pop commands to navigate in the netlist, and the flattened view, where hierarchy is simply ignored.

Logical cones support cross-probing. Therefore, you highlight and select objects the same way you do in the NetlistViewer. See “Selecting Objects” and “Highlighting and Unhighlighting Objects” in this guide.

All Logical Cone commands are available from the LogicalCone menu in MultiView Navigator, and most Logical Cone commands are also available from the right-click menu in both the NetlistViewer and Logical Cone windows.

Creating a Logical Cone

Logical cones enable you to view, highlight, and cross-probe a selected subset of your netlist.

You can create as many logical cones as you want. A logical cone displays only the objects you add to it. Initially, the cone does not contain objects.

To create a logical cone:

1. In NetlistViewer, select one or more objects.
2. Right-click the selected object(s), and choose **Add To Active Cone>Add Selection**.

A Logical Cone window containing only the selected object(s) appears. You can add and delete objects from this window.

To create an empty Logical Cone window:

- In NetlistViewer, from the LogicalCone menu, choose Create New Cone. A new window appears in which you can add logic to the cone. The name of the new cone appears in the **Logical Cones** tab of the **Hierarchy** window.

Now you can add logic to your cone.

Changing the Name of a Cone

You can modify the name of any Logical Cone view. The new name appears in the title bar of the cone window as well as in the Logical Cones tab of the Hierarchy window.

To change the name of a cone:

1. Select a Logical Cone view.
2. From the **LogicalCone** menu, choose **Rename Cone**.
3. In the Rename Cone dialog box, type the new name over the existing one.
4. Click **OK**.

Note: The Rename Cone command is available only when the current window is a Logical Cone view.

Tip: You can also rename a cone from the **Logical Cones** tab in the **Hierarchy** window.

Click once on the cone name to select it, and click again to edit it. When you see an outline around the highlighted name, type the new name in place of the old one.

Deleting a Logical Cone

To delete a Logical Cone:

1. In the **Logical Cones** tab of the **Hierarchy** window, click the **plus sign (+)** to the left of Logical Cones to display the names of the cone views.
2. Right-click the cone to delete, and choose **Delete** from the right-click menu.

Setting the Active Cone

The active or current cone is the one in which you can add or remove logic. Before you can add or remove objects from a cone, you must select the cone you want to modify.

To set the active cone, right-click the cone in the **Logical Cones** tab of the **Hierarchy** window, and choose **Set Active**.

Hiding Logic in a Hierarchical Instance

To hide logic within a hierarchical instance in a cone view:

1. Click the Logical Cone containing the logic to hide.
2. Select the instance to hide from view.
3. From the **LogicalCone** menu, choose **Fold Selection**.

All the logic inside the selected hierarchical instance disappears from the cone. Hiding the logic inside an instance reduces the size of the logic, providing you with a better global view of the cone content.

Displaying Logic Hidden within a Hierarchical Instance

To display logic that was added to a hierarchical instance in a cone view:

1. Click the Cone view containing the logic to show.
2. Select the instance containing hidden logic.
3. From the **LogicalCone** menu, choose **Unfold Selection**.

All the logic previously hidden inside of the selected hierarchical instance reappears in the cone. If the selected instance does not contain logic, nothing happens.

Adding Selected Objects to a Cone

You can add only instances and pins to a cone. (Nets and ports, if required, are automatically added to the cone.)

To add objects to a cone:

1. Make sure the cone to which you want to add objects is the active cone.
2. In NetlistViewer or a Logical Cone view, select the instances and pins to add to the cone.
3. From the **LogicalCone** menu, choose **Add To Active Cone> Add Selection**.

All the objects appear in the active cone view. If the objects can be connected to other objects already present in the active cone, the command also connects those objects. If some of the selected objects are pins, the corresponding instances are added.

Adding a Group of Highlighted Objects to a Cone

You can add a group of highlighted instances and pins to the active cone. (Nets and ports, if required, are automatically added to the cone.)

To add a group of highlighted objects to a cone:

1. Highlight the objects you want to add to a cone.
2. Click the cone to which you want to add your highlighted objects.
3. From the **LogicalCone** menu, choose **Add To Active Cone>Add Highlighted Group**.
4. Click a highlighted object. All objects with the same highlight color are added to the active cone.

All the highlighted objects appear in the active cone view. If the highlighted objects can be connected to other objects already present in the active cone, the command also connects those objects. If some of the highlighted objects are pins, the corresponding instances are added.

Tip: Click outside a highlighted object, or press **Esc** to terminate the command.

Clearing All Objects from a Cone

You can clear the entire contents of a cone with one command.

To remove all objects from a cone:

1. Make sure the cone you want to remove all objects from is the active cone.
2. From the **LogicalCone** menu, choose **Remove From Active Cone>Clear**.

The active window is now empty.

Removing Selected Objects from a Cone

You can remove specific instances and pins from the active cone. You cannot remove nets and ports from a Logical Cone.

To remove only selected objects from a cone:

1. Make sure the cone you want to remove objects from is the active cone.
2. Select the object(s) you want to remove from the cone.
3. From the **LogicalCone** menu, choose **Remove From Active Cone>Remove Selection**.

The selected objects no longer appear in the active cone. If some of the selected objects are pins, their corresponding instances are removed as well.

Removing a Group of Highlighted Objects from a Cone

You can remove a group of highlighted instances and pins from the active cone. You cannot remove nets and ports from a Logical Cone.

To remove only highlighted objects from a cone:

1. Make sure the cone you want to remove objects from is the active cone.
2. From the **LogicalCone** menu, choose **Remove From Active Cone>Remove Group**. The cursor turns into a color picker pointer.
3. Click a highlighted object. All objects with the same highlight color are removed from the active cone.

The highlighted objects you selected no longer appear in the active cone view. If some of the highlighted objects are pins, their corresponding instances are removed.

Tip: Click outside a highlighted object, or press **Esc** to terminate the command.

Adding Drivers to a Cone

You can add the driving instance(s) for an instance, a net, or an input pin to a cone.

To add the driver of an instance to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select the instance, net, or input pin whose driver you want to add to the cone.
2. Right-click the selected instance, and choose **Add To Active Cone>Add Driver**.

The driver for the selected instance appears in the active cone. For input pins, this command adds the connected net and driving instance to the active cone. For nets, this command adds the driving instance to the active cone. For each instance, this command adds the driver for each of the instance's input pins to the active cone.

If the added objects can be connected to other objects already present in the active cone, this command also connects those objects.

Adding Driven Instances to a Cone

You can add all of the logic driven by an instance, a net, or an output pin to a cone at the same time.

To add a driven instance to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select the output pin, net, or instance for which you want to add the driven logic to the cone.
2. Right-click the instance, and choose **Add To Active Cone> Add All Driven Logic**.

All instances driven by the selected object(s) appear in the active cone. For each selected net, it adds all the driven instances to the active cone. For each selected output pin, this command adds the connected net and all the instances connected to it. For each selected instance, this command adds the driven logic for each output pin.

If the added objects can be connected to other objects already present in the active cone, the command also connects those objects.

Adding Adjacent Objects to a Cone

You can add some of the objects that are connected to a net, pin, or instance to the active cone. These objects include the ones that have a pin driven by the selected net, output pin, or instance.

To add an adjacent object to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select a pin, net, or instance connected to objects that you want to add to a cone.
2. Right-click the selected object, and choose **Add To Active Cone>Add Adjacent**. A dialog box displays all instances connected to your selection.
3. Select one or several instances from the list. Optionally, click **Select All** to select the entire list of instances.
4. Click **OK**.

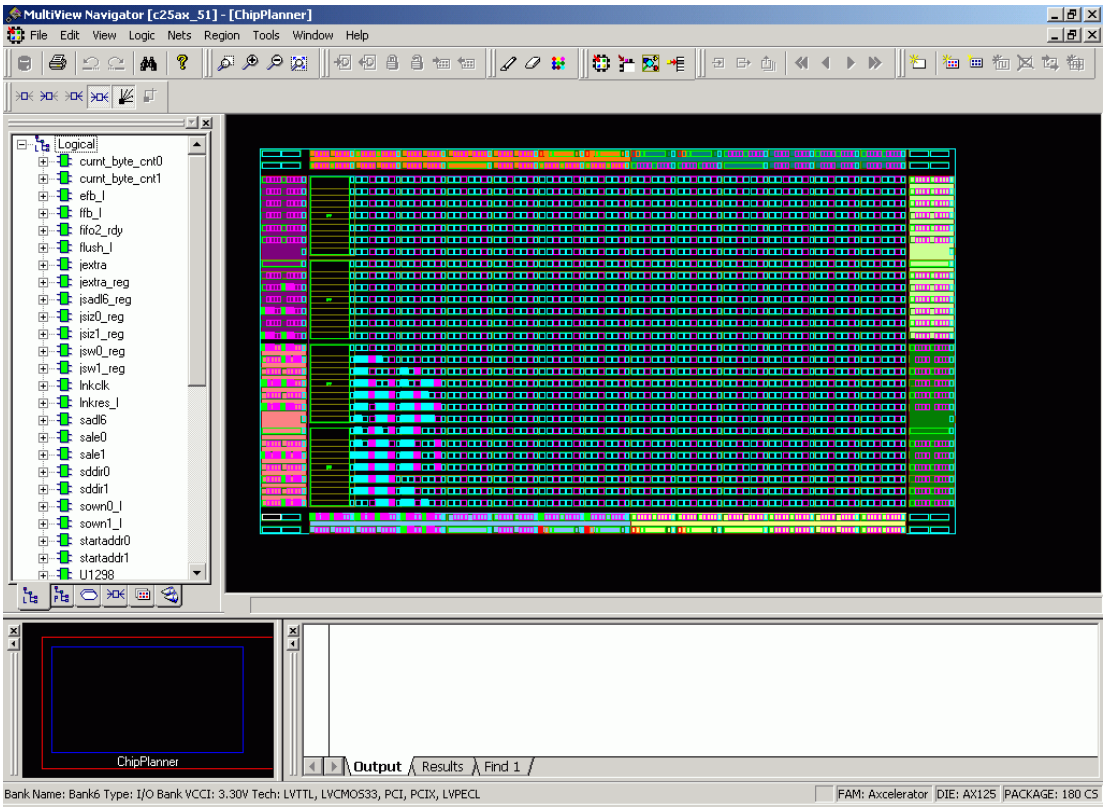
The selected instance(s) are added to the active cone. If the added instances can be connected to other objects already present in the active cone, this command also connects those objects.

Using NetlistViewer with ChipPlanner

If both NetlistViewer and ChipPlanner are open, items selected in either tool are selected and highlighted in the other. ChipPlanner is Actel's floorplanning tool, which you use to create and edit regions on your chip and assign logic to those regions.

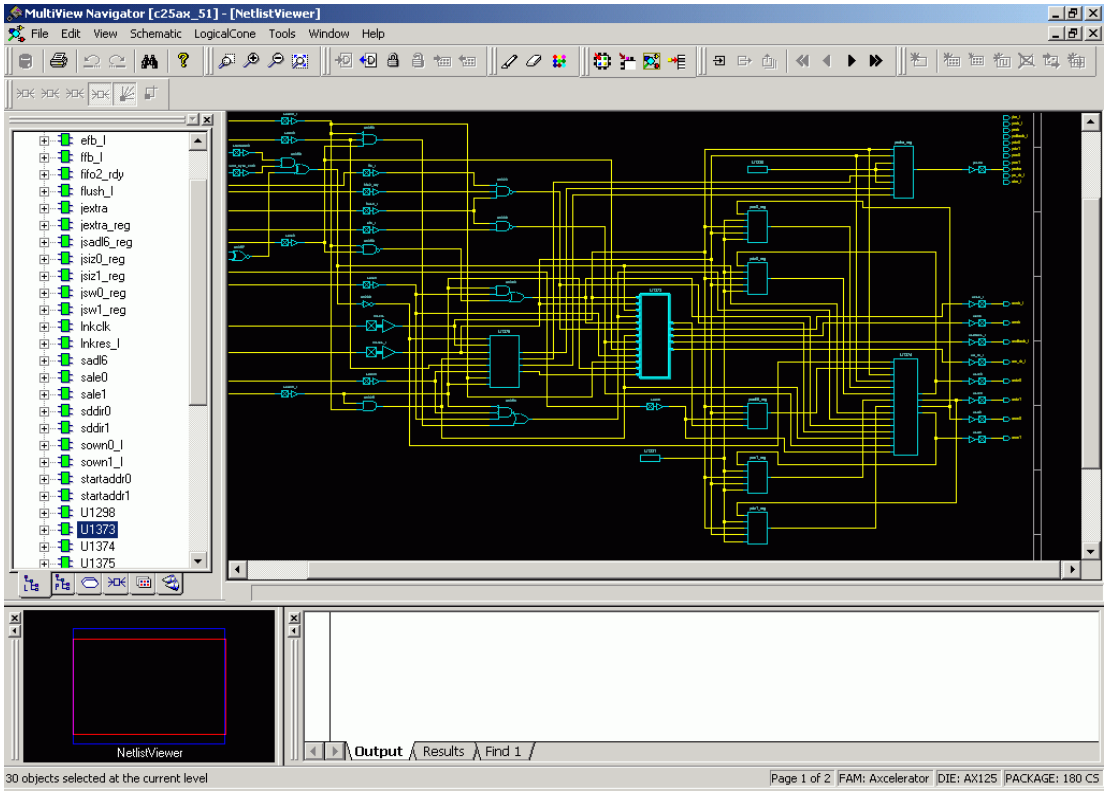
To use NetlistViewer with ChipPlanner:

1. Click **NetlistViewer** in the Designer Design Flow window. NetlistViewer starts and displays your netlist.
2. From the **Tools** menu, choose **ChipPlanner**. ChipPlanner opens in a separate window in the MultiView Navigator and displays the logic and I/O modules on the device.

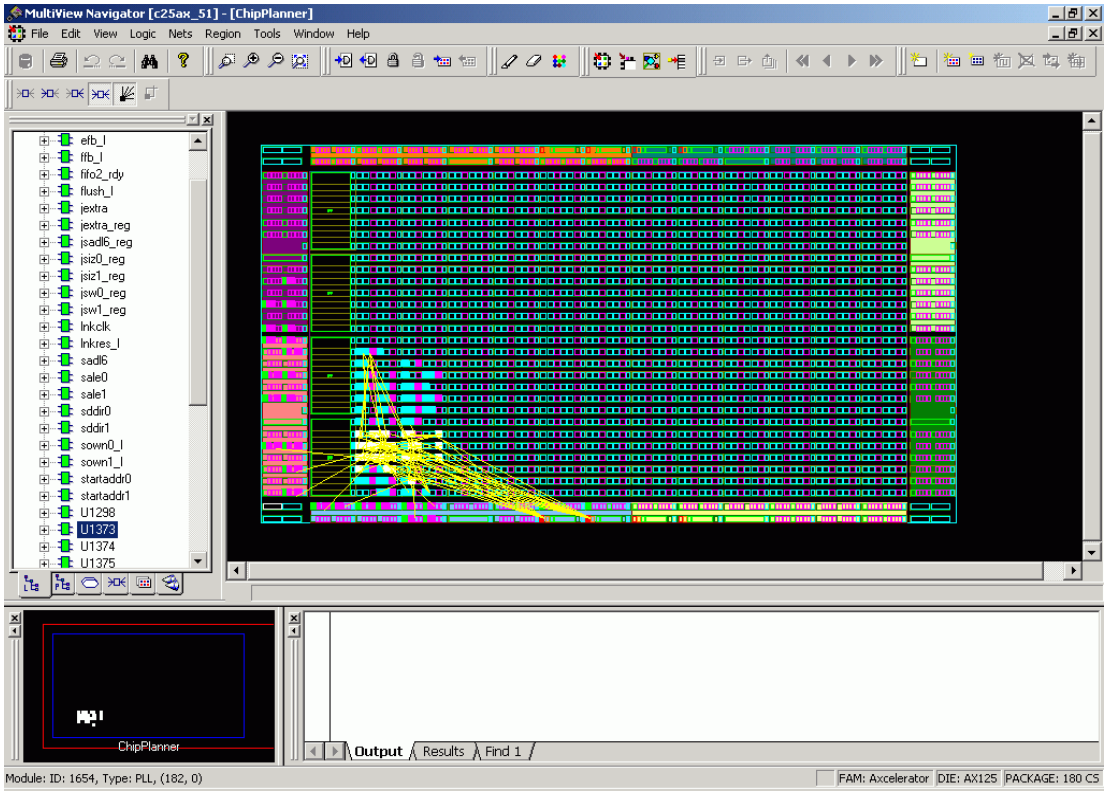


ChipPlanner Window

3. Select a macro or instance in either ChipPlanner or NetlistViewer. The selected item appears selected in both tools.



Item Selected in NetlistViewer



Same Item Selected in ChipPlanner

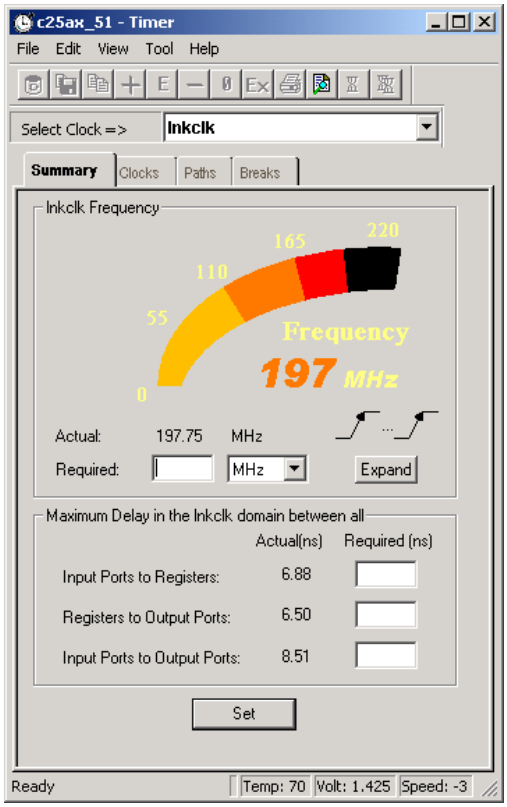
Using NetlistViewer with Timer

Use NetlistViewer with Timer to view and trace entire Timing paths.

Note: Your design must be compiled to start NetlistViewer. If it is not compiled, Designer prompts you to compile your design. After you compile it. NetlistViewer opens and displays the netlist.

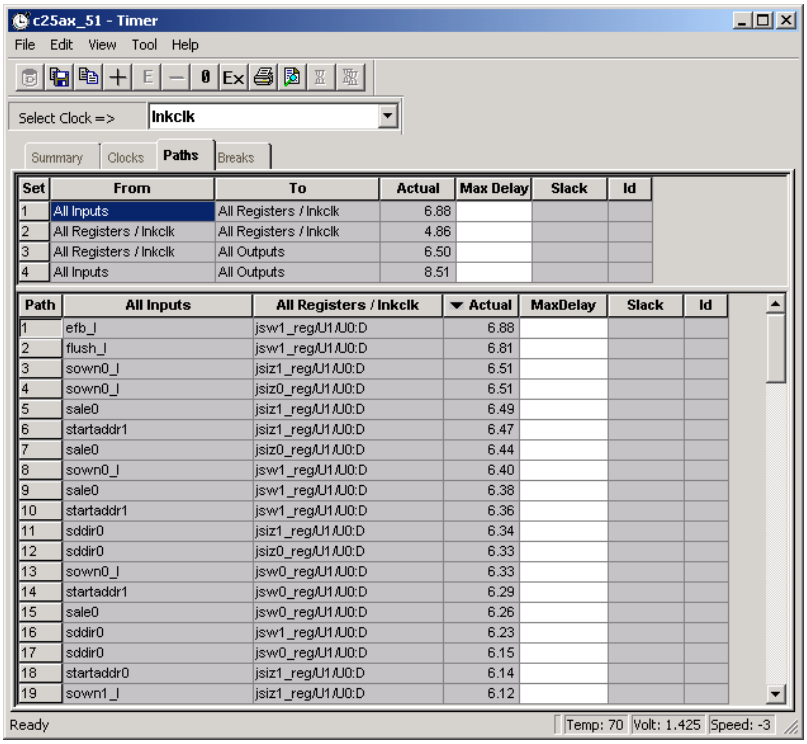
To trace paths using NetlistViewer and Timer:

1. Click **NetlistViewer** in the Designer **Design Flow** window to display the netlist.
2. Click **Timer** in the Designer **Design Flow** window to display the **Timer** window.



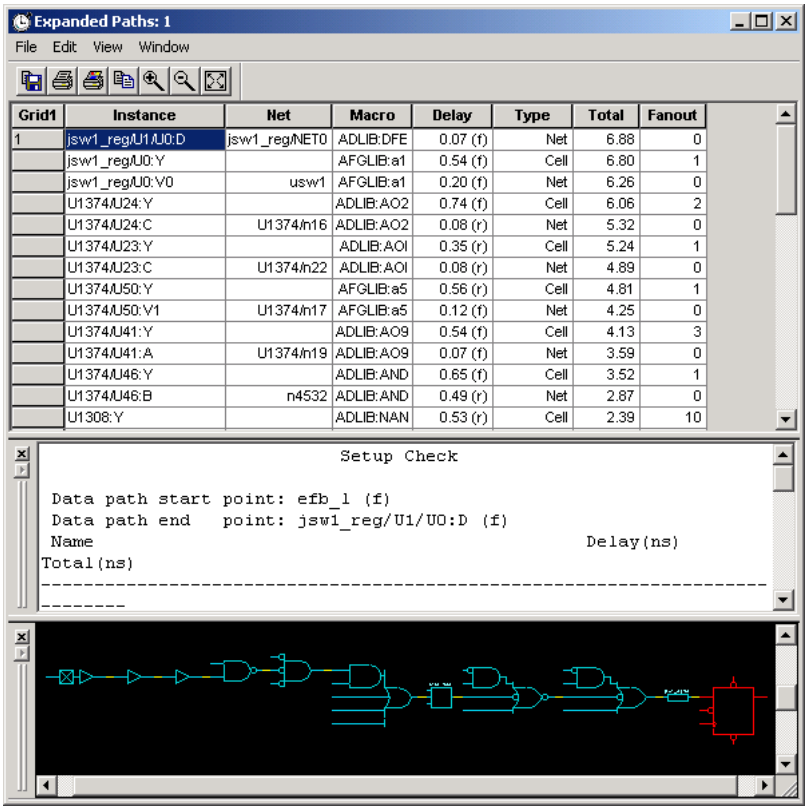
Timer Window

3. Click the Timer **Paths** tab.
4. Select a path set in the path set table. Paths within that set are displayed in the **Path Set** window.



Timer Paths Tab

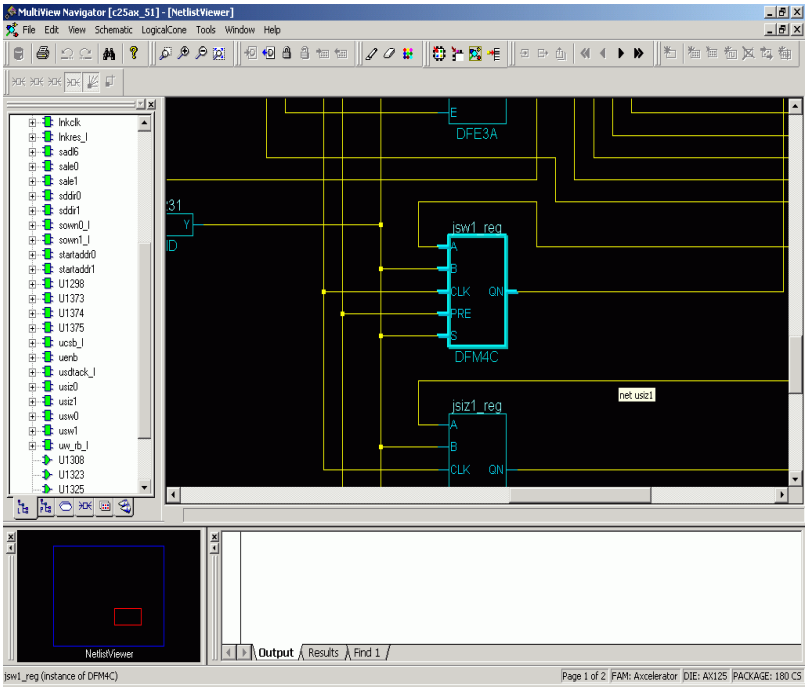
5. Double-click a path to expand it, or from the **Edit** menu, choose **Expand Paths**. The **Expanded Paths** window opens. The **Expanded Paths** window displays the path in the **Expanded Paths** grid and a graphical representation of the path in the **Graph** window.



Grid1	Instance	Net	Macro	Delay	Type	Total	Fanout
1	jsw1_reg/U1/U0:D	jsw1_reg/NET0	ADLIB:DFE	0.07 (f)	Net	6.88	0
	jsw1_reg/U0:Y		AFGLIB:a1	0.54 (f)	Cell	6.80	1
	jsw1_reg/U0:V0	usw1	AFGLIB:a1	0.20 (f)	Net	6.26	0
	U1374/U24:Y		ADLIB:AO2	0.74 (f)	Cell	6.06	2
	U1374/U24:C	U1374/n16	ADLIB:AO2	0.08 (r)	Net	5.32	0
	U1374/U23:Y		ADLIB:AOI	0.35 (r)	Cell	5.24	1
	U1374/U23:C	U1374/n22	ADLIB:AOI	0.08 (r)	Net	4.89	0
	U1374/U50:Y		AFGLIB:a5	0.56 (r)	Cell	4.81	1
	U1374/U50:V1	U1374/n17	AFGLIB:a5	0.12 (f)	Net	4.25	0
	U1374/U41:Y		ADLIB:AO9	0.54 (f)	Cell	4.13	3
	U1374/U41:A	U1374/n19	ADLIB:AO9	0.07 (f)	Net	3.59	0
	U1374/U46:Y		ADLIB:AND	0.65 (f)	Cell	3.52	1
	U1374/U46:B	n4532	ADLIB:AND	0.49 (r)	Net	2.87	0
	U1308:Y		ADLIB:NAN	0.53 (r)	Cell	2.39	10

Timer Expanded Paths Window

6. Select an instance in the **Expanded Paths** grid or in the **Graph** window. The instance appears highlighted in both Timer and NetlistViewer.



Selected Instance in Timer Appears Highlighted in NetlistViewer

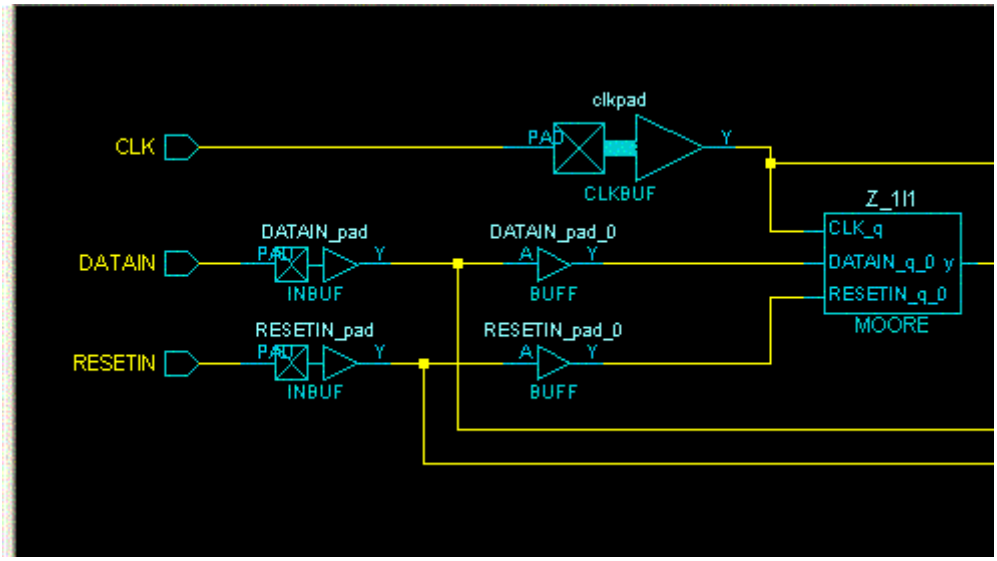
7. Select the first register in the **Timer** path and locate it in NetlistViewer. Follow the entire path in NetlistViewer.

Viewing Buffers

You can use NetlistViewer to see buffers inserted by your synthesis tool due to the high-fanout number of some signals.

To view inserted buffers, click **NetlistViewer** in the Design Flow window. NetlistViewer starts and displays your netlist.

In the following example, the fanout of the DATAIN and RESET inputs of the design exceeds the specified value in the Synplicity synthesis tool. To reduce the number of fanout for these signals, Synplicity inserts two buffers in their path. You can use NetlistViewer to see these inserted buffers.



Inserted Buffers

PinEditor in MultiView Navigator

PinEditor is the package layout interface you use to assign I/O ports to package pins.

Note: PinEditor supports the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families. If you are designing for the MX, eX, SX, or SX-A families, use PinEditor Standalone. See the PinEditor Standalone online help or the *PinEditor Standalone User's Guide* for more information.

Use PinEditor to:

- Assign I/O macros to pins
- Lock pin assignments that have automatically been assigned during layout
- View and print pin assignments
- Assign I/O standards to banks (for families that use I/O banks)
- Assign VREF pins (for I/O standards that require an input reference voltage)

Scripting Commands

You can make pin assignments, lock and unlock pins, commit pin assignments, and edit I/O attributes by running Tool Command Language (Tcl) scripts. You can run scripts from the Windows or UNIX command line or store and run a series of commands in a .tcl batch file.

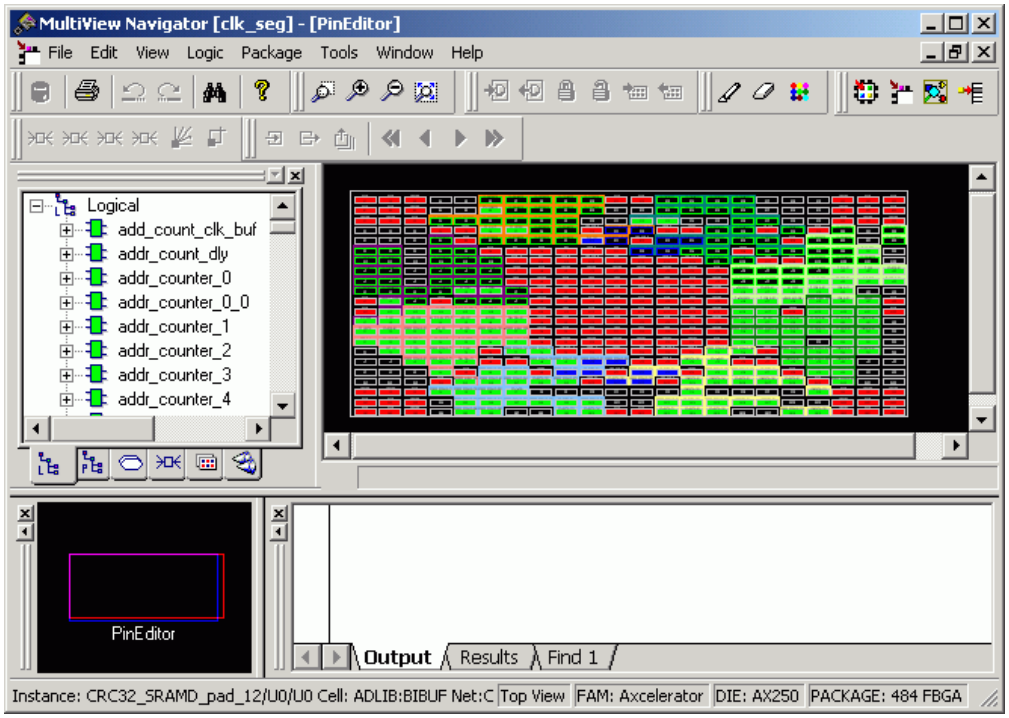
For more information on PinEditor Tcl extension commands, please refer to “Scripting” in the *Designer User’s Guide*.

Starting PinEditor in MultiView Navigator (MVN)

To start PinEditor from Designer, either click the **PinEditor** icon in the Designer Design Flow window, or from the **Tools** menu, choose **PinEditor**.

To start PinEditor from within MVN, either click the **PinEditor** button in the MVN toolbar, or from the **Tools** menu, choose **PinEditor**.

PinEditor opens in the Tools window of the MultiView Navigator interface and displays the pins and I/O macro assignments in your design. For ProASIC3E, ProASIC3, and Axcelerator families, it also displays I/O banks.



PinEditor in MultiView Navigator

When you select an assigned pin, the pin location appears selected in the World View window, and the I/O macro name is selected in the Logical and Physical hierarchy tabs.

You can display a top-down or bottom-up view of the package. To display a top-down view, from the **Package** menu, choose **View From Top**. To display a bottom-up view, from the **Package** menu, choose **View From Bottom**.

Colors and symbols

Colors and symbols differentiate the pin and logic I/O macro assignments in PinEditor. The following table indicates the default colors assigned to pins.

Color/Symbol	Definition
White border	A white border denotes a selected, assigned pin.
Green	A green border with a black center denotes a regular, unassigned pin. A pin with a grey or yellow border and a green center denotes a regular, assigned pin.
Blue	A blue border with a black center denotes a special, unassigned pin. A pin with a grey or yellow border and a blue center denotes a special, assigned pin. Special pins are pins that have some additional meaning to them. For example, pins used for JTAG are blue. When unassigned, special pins have additional descriptive text next to the pin number.
Grey with red center	Reserved pin. You use this pin for some specific purpose on the package, and you cannot assign it an I/O macro. Examples of such pins are ground and power.
Yellow	Yellow denotes *locked* assignments. If the assignment is selected, the symbol appears yellow. If the assignment is unselected, the border appears yellow.
Grey/black	A pin with a grey border and a black center denotes a pin that is not connected. You cannot use these pins, and they

	have no meaning.

Assigning Pins

Edits you make to pin assignments in PinEditor are permanent provided that they are locked and have been committed.

To assign an I/O macro to a pin:

1. Select the instance in the **Ports** tab of the **Hierarchy** window.
2. Drag the instance to the pin location. If the location is valid, the macro is assigned and automatically locked.

Note: If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned if it was not locked.

To assign multiple I/Os:

1. Select the I/Os from the **Ports** tab of the **Hierarchy** window.
2. From the **Logic** menu, choose **Assign to Location**.
3. In the **PinEditor** window, click each I/O location to which you want to assign the I/Os.

Unassigning pins

To unassign a macro from a pin:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Location**. This command is available only if the macro has been assigned to a location.

To unassign a macro from a region:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Region**. This command is available only if the macro has been assigned to a region.

Tip: You can also right-click the macro, and choose **Unassign From Region** or **Unassign From Location**.

Locking and Unlocking Pin Assignments

Designer does not alter locked pins during Layout. Designer recognizes pins as locked when they are assigned in one of the following ways:

- Manually using PinEditor in a design schematic
- Using a pin file (all Antifuse families except Axcelerator)
- Using a PDC file (ProASIC3E, ProASIC3, and Axcelerator family only)
- Using a GCF file (ProASIC and ProASIC PLUS families only)

Locked pins are permanent, provided you commit locked pins to your design before you exit PinEditor. To save changes to disk (in your .adb file), use the Save command in Designer before exiting PinEditor.

To lock pins:

1. Select the instance to lock in the **Ports** tab or in the **PinEditor** window. To select multiple pins, hold down the **CTRL** key and select multiple pins with your mouse. To select all pins, choose **Select All** from the **Edit** menu.
2. From the **Edit** menu, choose **Lock**.

Note: You can also lock pins in the I/O Attribute Editor by selecting the Locked check box.

To unlock a pin:

1. Select the instance(s) to unlock in the Ports tab of the **Hierarchy** window or in the **PinEditor** window. To select multiple pins, hold down the **CTRL** key and select multiple pins with your mouse. To select all pins, from the **Edit** menu, choose **Select All**.
2. From the **Edit** menu, choose **Unlock**.

Note: If you are using the I/O Attribute editor, clear the Locked check box to unlock a pin.

Closing and Committing Pin Assignments

The changes you make to your pin assignments and I/O attributes in PinEditor are temporary until you commit them.

- To commit your pin assignments at any time, from the **File** menu, choose **Commit.**
- To commit your pin assignments when closing PinEditor, click **Yes** when prompted.

Committing your changes saves them to the "working" design for this Designer session only.

To save changes made in PinEditor to disk, you must save your design by choosing **Save** from the **File** menu in Designer.

Setting PinEditor Properties

You can bring the selected macro into view in PinEditor by setting the **Move the display to show Selected Macro or Module** property.

This property brings the selected macro or module into view in the PinEditor window. By default, this property is selected. If you don't want to change your viewing area each time you select a macro or module, clear this check box.

To set PinEditor properties:

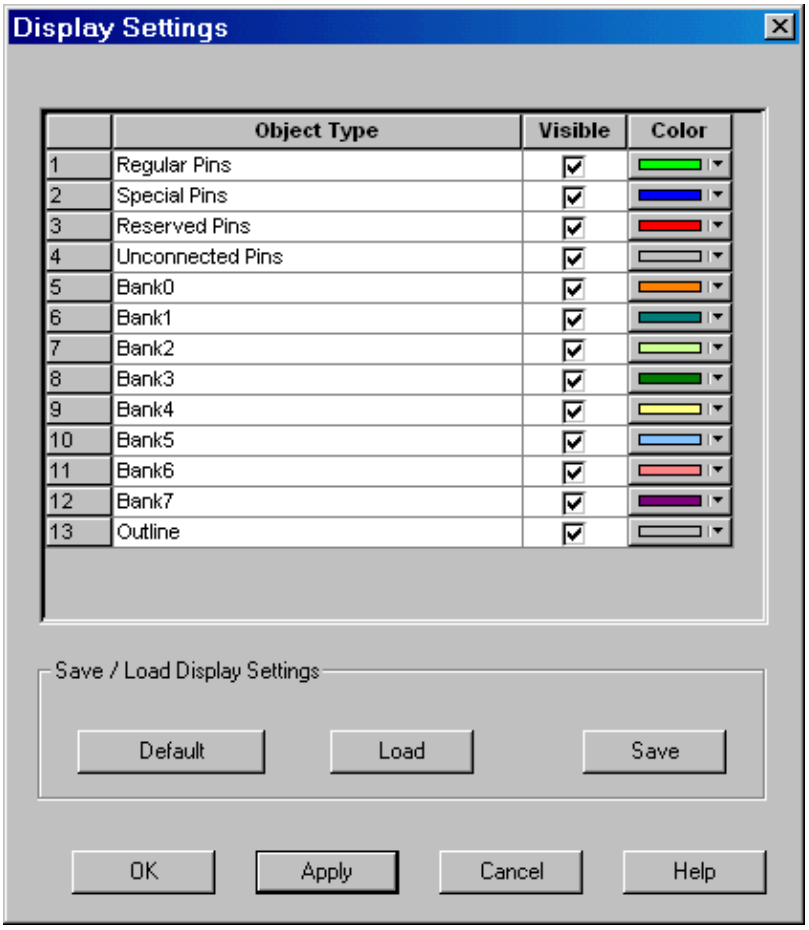
1. From the **View** menu, choose **Properties**.
2. In the PinEditor **Properties** dialog box, select the check box if you want to bring a macro or module into view when you select it, or clear the check box if you do not.
3. Click **OK**.

Changing an Object's Color

You can control the objects visible in your design and their displayed color.

To set display properties:

1. From the **View** menu, choose **Display Settings**. The **Display Settings** dialog box displays a list of all the architectural features you can turn on and off in PinEditor.



Display Settings Dialog Box in PinEditor

2. To make an object visible, select the **Visible** check box
3. To change the color used to display the object, click its color bar and select another color.
4. To save or open previously saved Display Settings, click:
   - **Save** to save your display settings to a file.
   - **Load** to open a saved display settings file.
   - **Default** to load the default display settings.
5. Click **Apply** to see your changes.
6. Click **OK** to dismiss the dialog box.

To change the color of an individual region:

1. Select the region.
2. Right-click the region, and choose **Properties.**
3. Select a different color from the **Color** drop-down list.

Editing I/O Attributes

You edit I/O attributes using the I/O Attribute Editor tool. This tool displays all assigned and unassigned I/O macros and their attributes in a tabular format.

Use the I/O Attribute Editor tool to view, sort, select, and edit common and device-specific I/O attributes.

From the **Tools** menu, choose **I/O Attribute Editor**.

For descriptions of individual I/O attributes and support by family, refer to the I/O Attributes Reference section of the *Designer User's Guide*.

Using I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip.

ProASIC3E and Axcelerator

ProASIC3E and Axcelerator devices have eight I/O banks surrounding the chip, two per side, numbered 0-7. The I/O banks are color-coded for quick identification. You can change the default colors through the Display Settings dialog box.

Each I/O bank has a common:

- VCCI, the supply voltage for its I/Os
- VREF, the reference voltage (for voltage-referenced I/O standards)

You can assign only one VREF pin to each I/O bank. Only I/O standards compatible with both the same VCCI and VREF standards can be assigned to the same bank. The following table shows the required voltage values and their compatible I/O standards for Axcelerator devices.

VCCI	Compatible I/O Standards
3.3V	LVTTL, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, LVPECL
2.5V	LVCMOS 2.5, GTL+ 2.5, SSTL2 (Class I & II), LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5, HSTL (Class I)

The following table shows the required voltage values and their compatible I/O standards for ProASIC3E devices.

VCCI	Compatible I/O Standards
3.3V	LVTTL, LVCMOS 3.3, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, GTL 3.3, LVPECL
2.5V	LVCMOS 2.5, LVCMOS 2.5/5.0, GTL+ 2.5, GTL 2.5, SSTL2 (Class I & II), LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5, HSTL (Class I), HSTL (Class II)

Note: The low-power mode and input delay attributes are not available in the I/O Bank Settings dialog box for ProASIC3E and ProASIC3 devices. Because these attributes are not available, the More Attributes button is also not available.

Banks are visible in both ChipPlanner and PinEditor. Information about banks appears in the MultiView Navigator's status bar.

ProASIC3

ProASIC3 devices have two, four, or eight I/O banks surrounding the chip, one per side, numbered 0-1, 0-3, or 0-7, respectively. Each I/O bank has dedicated resources for an input/output supply voltage (VCCI). Because of these dedicated resources, you can assign only I/Os with compatible standards to the same I/O bank. The following table shows the required voltage values and their compatible I/O standards.

VCCI	Compatible Standards
3.3V	LVTTL, PCI 3.3, LVPECL, LVCMOS
2.5V	LVCMOS 2.5/5.0, LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5

On some dies, the left and right side of the chip have a different selection of I/O standards (LVDS/LVPECL). Because the dies do not need an input referenced voltage (VREF), the **Use Pin for VREF** and **Highlight VREF Range** commands are unavailable from the right-click menu. Also, because the low-power mode and input delay attributes are not available, the **More Attributes** button is not available in the I/O Bank Settings dialog box.

Note: ProASIC3 devices do not support the Input Delay attribute.

Specifying Standards for an I/O Bank

You can specify standards for each I/O bank by doing one of the following:

- Using the I/O Bank Settings dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage
- Using the command `set_iobank` in a PDC file

You cannot change the I/O standard of an assigned I/O to an I/O standard that is incompatible with the bank. If you need to assign the I/O standard to a new technology, first unassign the I/O.

Assigning Technologies to I/O Banks

The procedure for assigning technologies to I/O banks differs depending on whether you are designing for ProASIC3E, ProASIC3, or Axcelerator devices.

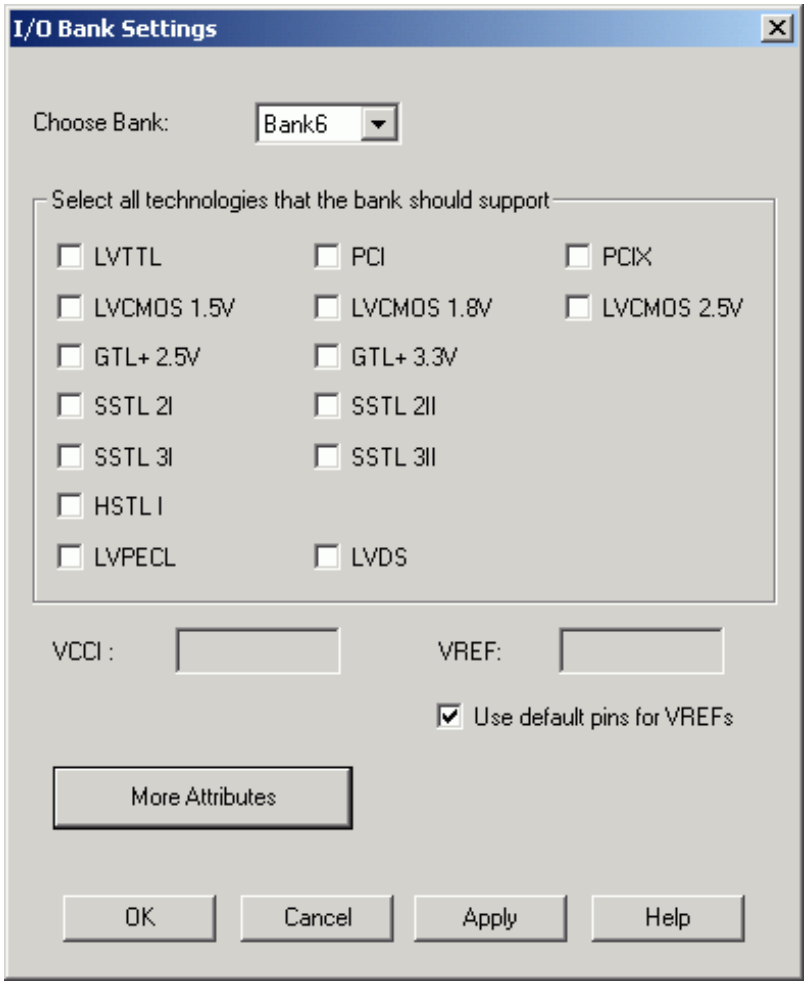
To assign technologies to I/O banks in Axcelerator and ProASIC3E devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further, selecting GTLP (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Click **More Attributes** to set the low-power mode and input delay. (These attributes are not supported in RTAXS, ProASIC3, and ProASIC3E devices.)
5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.

6. Leave the **Use default pins for VREFs** option selected to set default VREF pins and unset non-default VREF pins. If you unselect this option when setting a new VREF technology, no VREF pins are set. If you unselect this option when default VREF pins are already set, it unsets them.

   If the **Use default pins for VREFs** option is selected when you click **OK** or **Apply**, the software: 1) determines if setting default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, 2) determines if unsetting non-default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, and 3) sets default VREF pins and unsets non-default VREF pins.

7. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.



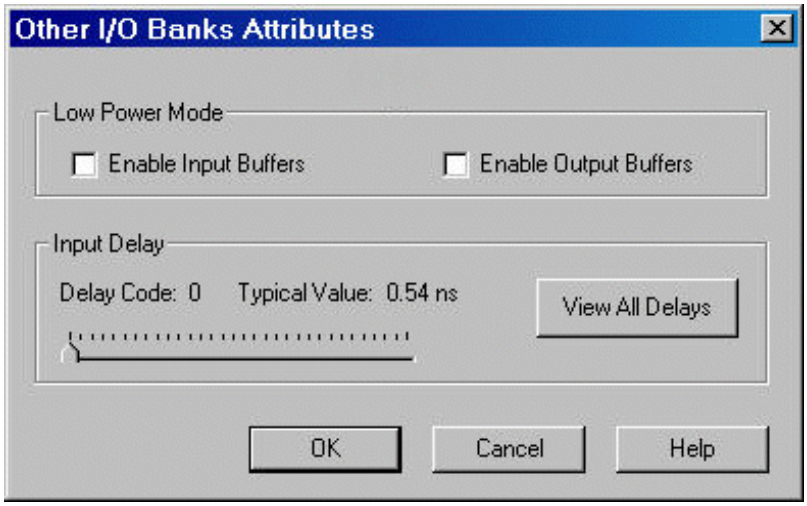
I/O Bank Settings Dialog Box for ProASIC3E and Axcelerator Devices

If VREF pins can be assigned, you must assign at least one VREF pin before running Layout. See "Assigning VREF Pins" in this guide for more information.

Note: If you use I/O standards that need reference voltage, make sure to assign VREF pins. Actel strongly recommends you use the defaults. VREF pins appear in red in ChipPlanner and are labeled VREF in PinEditor.

To set the low-power mode and input delay (for Axcelerator devices only):

1. Click **More Attributes** in the **I/O Bank Settings** dialog box.
2. Drag the slider bar to the desired delay. The delay is bank specific.
3. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. You must select a technology to see the input delays.
4. Click **OK**.

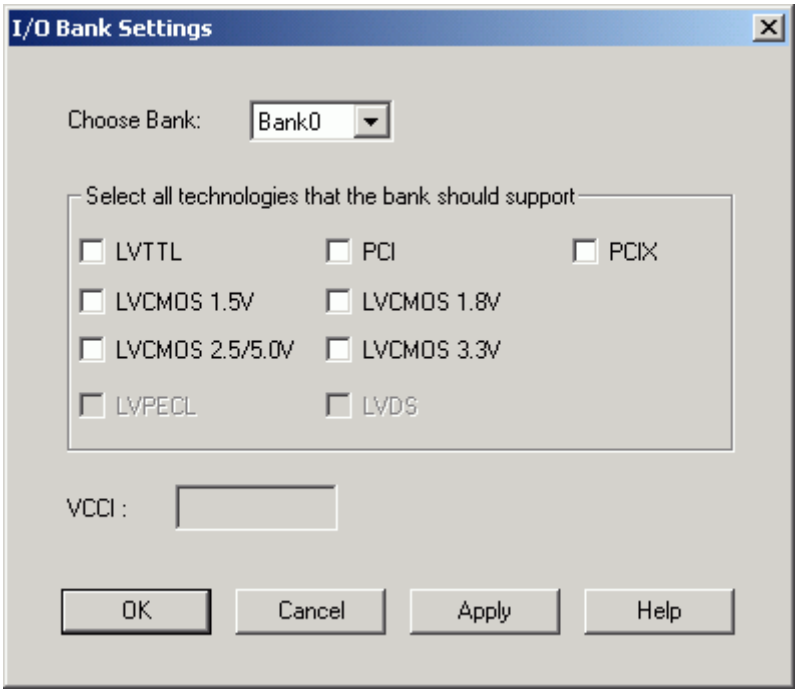


Other I/O Bank Attributes Dialog Box

Note: Low-Power Mode and Input Delay are not supported in RTAX-S, ProASIC3, and ProASIC3E devices.

To assign technologies to I/O banks in ProASIC3 devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Note that LVDS is available only for banks 1 and 3. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
5. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.



I/O Bank Settings Dialog Box for ProASIC3 Devices

Note: You cannot assign VREF pins in ProASIC3 devices.

Assigning Pins in ProASIC3E

To assign I/O in the ProASIC3E family:

1. From Designer's **Tools** menu, choose **Device Selection**. Select a die, package, speed, and die voltage, and click **Next**.
2. In the **Device Selection Wizard-Variations** dialog box, from the Default I/O Standard drop-down list, select the default I/O standard for all generic I/O macros. This action sets the same VCCI for each bank. You cannot choose LVDS or LVPECL as the default I/O standard. If your design has only one single-ended I/O and one VCCI requirement, go to step 8. Otherwise, in the next step you will specify the I/O standards for each I/O bank.
3. Start either **ChipPlanner** or **PinEditor**.
4. From the **Tools** menu, choose **I/O Bank Settings**.
5. In the **I/O Bank Settings** dialog box, choose an I/O standard for each I/O bank.
6. In ChipPlanner or PinEditor, assign VREF pins, if the standard requires VREF voltage. See Assigning VREF pins. In ProASIC3E, you can use any I/O as a VREF pin. The default VREFs setting may create more VREF pins than needed and may result in a loss of usable user I/Os. If that happens, you can choose the custom VREF setting. You must create enough VREF pins to allow a legal placement of the compatible user-voltage-referenced I/O macros. After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin.
7. After assigning VREF pins, from the **Tools** menu, choose **DRC** to check the I/O voltage assignment and to generate an I/O bank report. The I/O voltage Usage section in this report shows whether you have enough I/Os available for each voltage. Any

infeasible voltage requirements appear as an asterisk (*) in the I/O voltage Usage report. If asterisks appear in your report, you should resolve the problem before continuing.

8. Once you have completed the I/O Bank assignments, you can assign I/O macros to individual pad locations using either the MultiView Navigator or a PDC file.

Note: Choosing Commit from the File menu also performs the DRC check.

Assigning VREF Pins

Voltage referenced I/O inputs (VREF) require an input referenced voltage. You must assign VREF pins to **Axcelerator** and **ProASIC3E** devices before running Layout.

Before assigning a VREF pin, you must set a VREF technology for the bank to which the pin belongs.

To set a VREF technology for a bank:

1. Select a bank in ChipPlanner.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select a technology such as GTL+ 3.3V so the VREF field displays a non-zero value.
4. Click **OK**. Now when you right-click on pins in this I/O bank, the VREF commands on the menu are enabled.

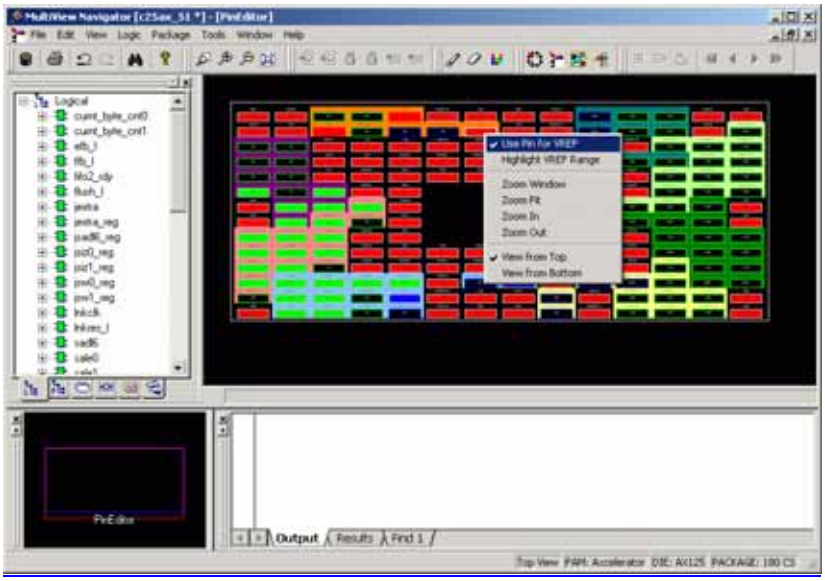
In either the PinEditor or ChipPlanner window, you can change a regular pin into a VREF pin from the right-click menu.

To assign a pin as a VREF pin:

1. In either PinEditor or ChipPlanner, select the pin to set as a VREF pin.
2. Right-click and choose **Use Pin for VREF**.

A check mark appears next to the **Use Pin for VREF** command in the right-click menu.

Note: The Use Pin for VREF command appears on the right-click menu only if you selected a pin in an I/O bank that supports VREF pins and for package pins or I/O modules that can become VREF pins.



Use Pin For VREF Command

Setting a pin as a VREF may result in I/O macros becoming unassigned, even if they are locked. In this case, a warning message appears so you can cancel this operation.

To unassign a VREF pin:

1. Select the pin to unassign.
2. Right-click and choose **Use Pin for VREF**. The check mark next to the command disappears. The VREF pin is now a regular pin.

Resetting the pin may result in unassigning I/O macros, even if they are locked. In this case, a warning message appears so you can cancel this operation.

Tip: You can also reset the **Use Pin for VREF** command by choosing **Undo** from the **Edit** menu.

After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin. To unhighlight the range, choose **Unhighlight All** from the **Edit** menu.

Displaying Pins in a VREF Range

You can see which pins in an I/O bank are serviced by a VREF pin. Use the right-click menu's **Highlight VREF Range** command while in PinEditor or ChipPlanner to see these pins.

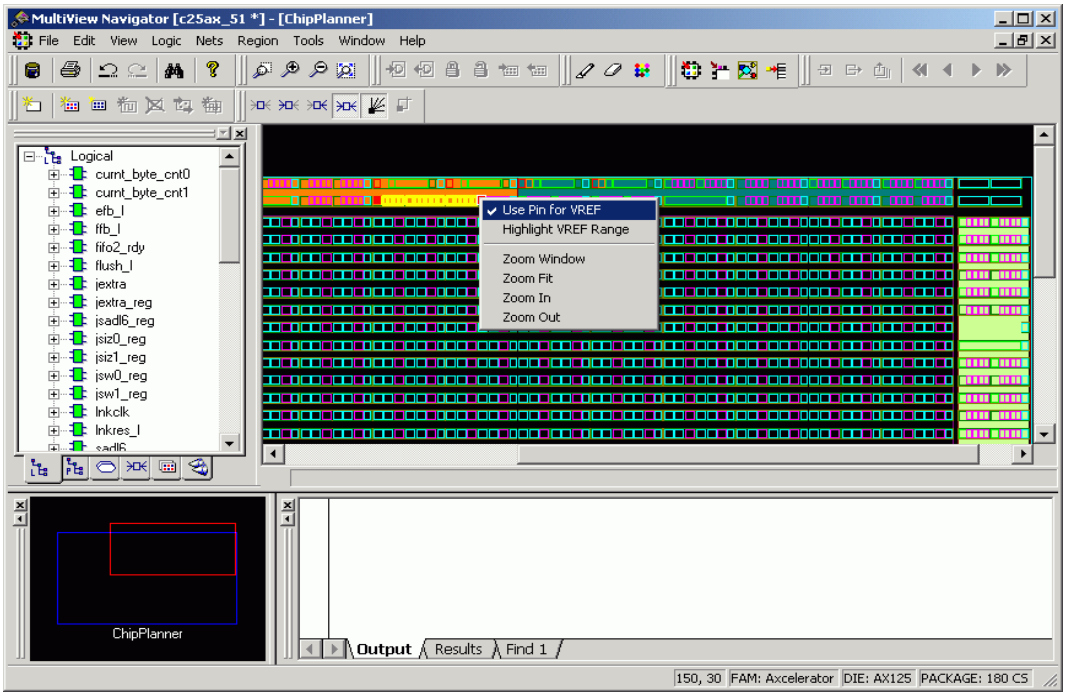
To display pins in a VREF range:

1. Right-click a VREF pin in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight VREF Range.**

When using PinEditor, all pins serviced by the selected VREF pin appear highlighted. In the following illustration, the pins serviced by the selected VREF pin are highlighted in orange.

Highlight VREF Range

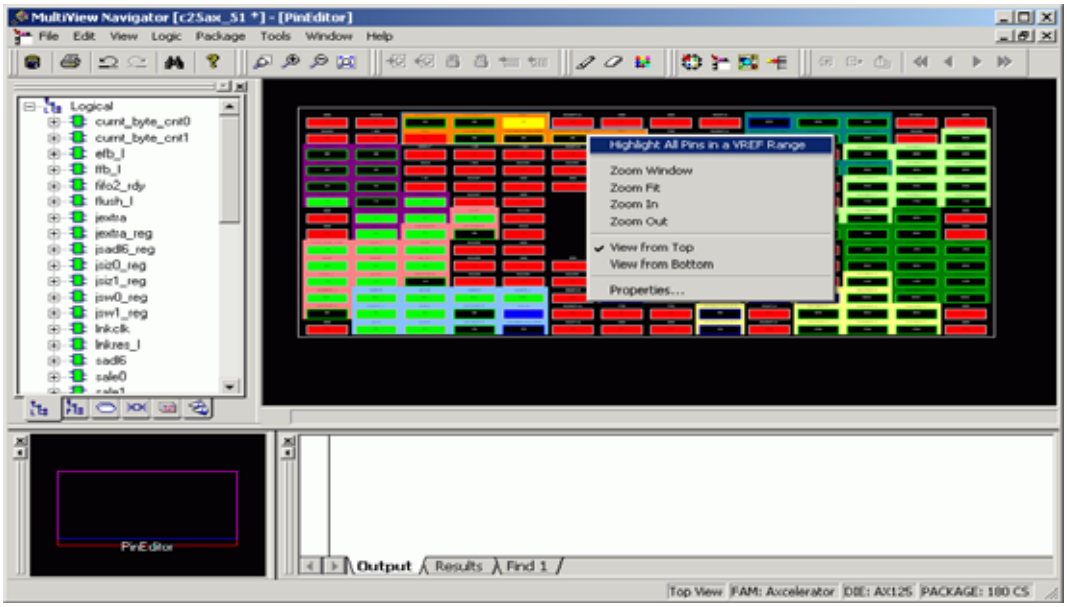
When using ChipPlanner, all I/O modules serviced by the selected VREF pin appear highlighted. The following illustration shows the right-click menu in ChipPlanner when a VREF pin is selected.



Right-click Menu in ChipPlanner

To highlight all pins in a VREF range:

1. Right-click an I/O bank in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight All Pins in a VREF Range.**



Highlight All Pins in a VREF Range

The **Highlight All Pins in a VREF Range** command appears in the right-click menu for all I/O banks that include a VREF pin.

All of the pins in the I/O bank that are serviced by a VREF appear highlighted. If the I/O bank does not contain a VREF pin, nothing is highlighted when you select this command.

To unhighlight all pins in a VREF range:

1. Select the highlighted range.
2. From the **Edit** menu, choose **Unhighlight All**.

I/O Attribute Editor

Note: The I/O Attribute Editor supports the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families. If you are designing for other families, use the standalone version of PinEditor, which includes an embedded I/O Attribute Editor.

The I/O Attribute Editor opens within the Tools window of the MultiView Navigator. It displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format.

Use I/O Attribute Editor to:

- View, sort, select, and edit common and device-specific I/O attributes
- Lock and unlock assigned attributes

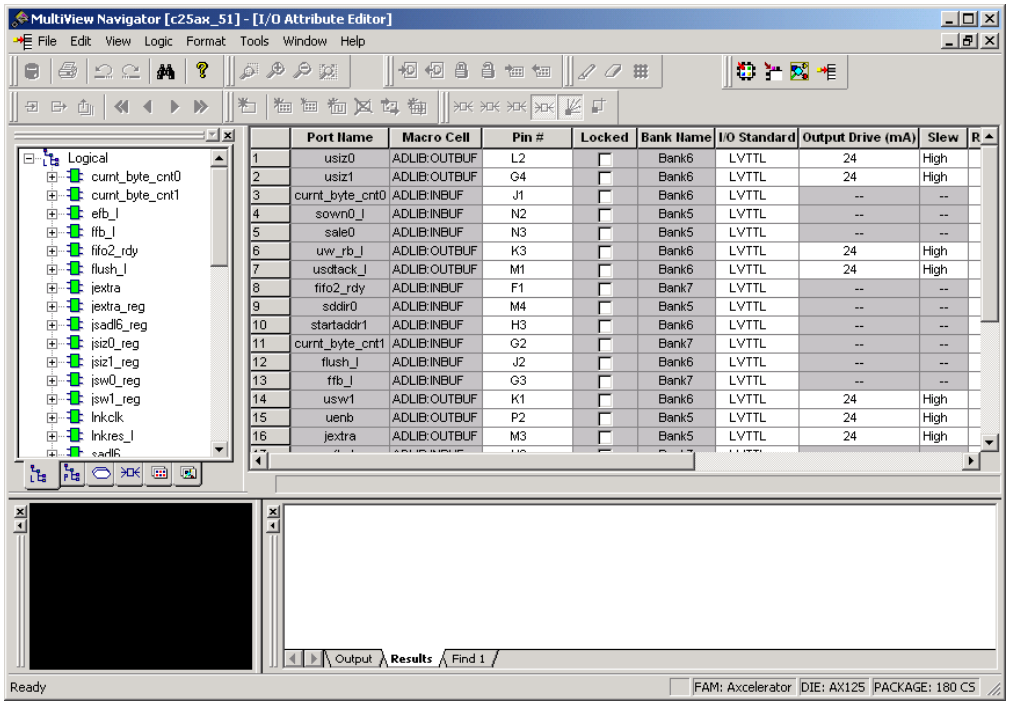
Starting I/O Attribute Editor

I/O Attribute Editor requires a compiled design. If you start I/O Attribute Editor before compiling your design, Designer compiles your design before opening I/O Attribute Editor.

To start I/O Attribute Editor from Designer, either click the **I/O Attribute Editor** icon in the Designer Design Flow window, or from the **Tools** menu, choose **I/O Attribute Editor**.

To start I/O Attribute Editor from within MVN, either click the **I/O Attribute Editor** button in the MVN toolbar, or from the **Tools** menu, choose **I/O Attribute Editor**.

The I/O Attribute Editor appears in the Tools window inside the MultiView Navigator and displays all assigned and unassigned I/O ports and their attributes in a tabular format. It functions much like a spreadsheet with sort, copy, and paste capabilities.



I/O Attribute Editor in MultiView Navigator

When you select a port name within the table, it also appears selected in the Logical, Physical, and Ports tabs of the Hierarchy window.

Editing I/O Attributes

You edit I/O attributes using the I/O Attribute Editor tool. This tool displays all assigned and unassigned I/O macros and their attributes in tabular format.

Use the I/O Attribute Editor tool to view, sort, select, and edit common and device-specific I/O attributes.

From the **Tools** menu, choose **I/O Attribute Editor**.

The column headings specify the names of the attributes in your design. The first four column headings are standard for all families so they will not change. However, the other column headings will change depending on the family you are designing for. For some I/O attributes, you will choose from a drop-down menu; for others, you might enter a value.

To edit I/O attributes:

1. Select an I/O standard for each I/O macro in your device.
2. Select I/O attributes that are available for your selected I/O standard.

For descriptions of individual I/O attributes and support by family, refer to the I/O Attributes Reference section of the *Designer User's Guide*.

Editing Multiple Rows

To edit multiple rows:

1. Select the rows to edit. To select consecutive rows, click the first row, press and hold down the **SHIFT** key, and then click the last row. To select rows that are not consecutive, press and hold down the **CTRL** key, and then click each row to select. Continue to hold down the **SHIFT** or **CTRL** key.
2. While still holding down the **SHIFT** or **CTRL** key, click in the cell containing the value you want to change. Release the **SHIFT** or **CTRL** key, and then release the mouse button. The change occurs in all selected rows.

Note: You can also select an entire column, which enables you to edit all rows.

Sorting Attributes

To sort I/O macros by attributes:

- Double-click a column heading to sort the table rows in ascending order.
- Double-click the column again to sort the table rows in descending order.

When sorted, an arrowhead appears in the column header to indicate the sort order.

Formatting Rows and Columns

When viewing and editing your input/output attributes, you can format the table to display only the attributes you want to see.

To hide one or more rows or columns:

1. Select the row(s) or column(s) you want to hide from view.
2. From the **Format** menu, choose **Row > Hide** or **Column > Hide**.

To show a hidden row or column:

1. Select the row(s) or column(s) on either side of the hidden row(s) or column(s).
2. From the **Format** menu, choose **Row > Unhide** or **Column > Unhide.**

You can “freeze” one or more columns so they remain visible on the screen as you scroll horizontally.

To freeze one or more columns:

1. Select the column(s) you want to freeze.
2. From the **Format** menu, choose **Column > Freeze Pane**.

To unfreeze one or more frozen columns, from the **Format** menu, choose **Column > Unfreeze Pane**. All frozen columns are unfrozen.

You can also resize all the columns and rows at once so their entire contents are visible.

To display a column's entire contents within it:

1. Select the column(s) you want to display.
2. From the **Format** menu, choose **Column >AutoFit**. The width of the column either expands or contracts to fit only the cell heading and cell contents.

Specifying an I/O Standard

Use the I/O Standard column to select an I/O specification for each pin.

If required to match the I/O standard, other I/O attributes, such as I/O threshold, slew, and loading, are automatically set to their default settings; you cannot edit these defaults.

You can change the I/O standards only for a generic I/O buffer to any of the legal I/O standards.

To specify an I/O standard:

1. Click the **I/O Standard** cell in the desired macro row.
2. Type or select a supported I/O standard from the drop-down list.

For devices that support I/O banks (for example, Axcelerator devices), the list is restricted to legal choices only. When an I/O is assigned, the I/O standards available for that I/O are limited to what the I/O bank location can support.

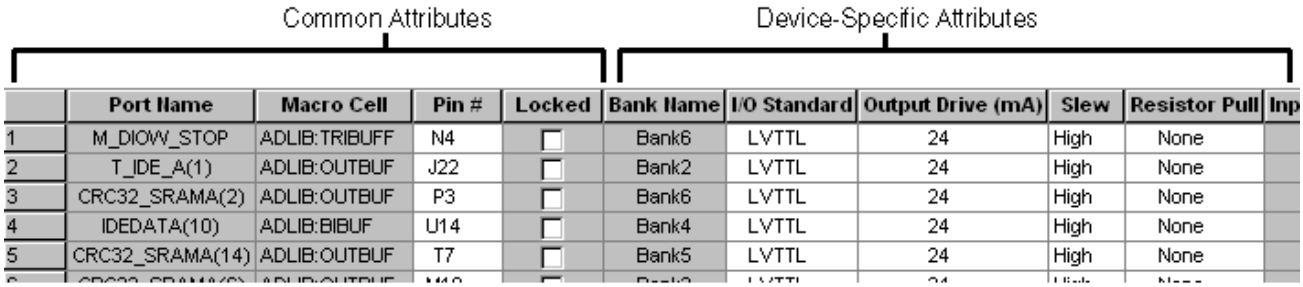
Note: Changing an I/O standard may also unassign existing I/Os. In addition, when a macro is assigned an I/O standard, the I/O bank is automatically assigned the voltages VCCI and VREF, if necessary. Unassigning this macro will undo these assignments as well.

Common I/O Attributes (All Families)

The I/O Attribute Editor displays four common attributes for all I/O macros:

- **Port Name** indicates the I/O macro name.
- **Macro Cell** indicates the type of I/O macro.
- **Pin #** indicates the current pin assignment.
- **Locked**, if checked, indicates that you cannot change the current pin assignment during layout.

Besides the common I/O attributes, the I/O Attribute Editor displays device-specific attributes. Only attributes applicable to a specific device appear in the I/O Attribute Editor table. The following example shows the I/O Attribute Editor for Axcelerator devices.



	Port Name	Macro Cell	Pin #	Locked	Bank Name	I/O Standard	Output Drive (mA)	Slew	Resistor Pull	Inp
1	M_DIOW_STOP	ADLIB:TRIBUFF	N4	☐	Bank6	LVTTL	24	High	None	
2	T_IDE_A(1)	ADLIB:OUTBUF	J22	☐	Bank2	LVTTL	24	High	None	
3	CRC32_SRAMA(2)	ADLIB:OUTBUF	P3	☐	Bank6	LVTTL	24	High	None	
4	IDEDATA(10)	ADLIB:BIBUF	U14	☐	Bank4	LVTTL	24	High	None	
5	CRC32_SRAMA(14)	ADLIB:OUTBUF	T7	☐	Bank5	LVTTL	24	High	None	

I/O Attributes by Family (in MVN)

The following table includes the attributes that each individual device family supports.

Attribute	Family				
	ProASIC3E	ProASIC3	ProASIC PLUS	Axcelerator	ProASIC
Bank Name	X	X		X	
I/O Standard	X	X	X	X	X
Output Drive	X	X		X	
Slew	X	X		X	
Resistor Pull	X	X		X	
Schmitt Trigger	X				
Input Delay	X			X	
Skew	X	X			
Output Load	X	X	X	X	X
Use Register	X	X			
Hot Swappable	X	X		X	

Refer to the appropriate datasheet for information about I/O standards for different families.

ChipPlanner in MultiView Navigator

ChipPlanner is the floorplanning tool you use to create and edit regions on your chip and assign logic to these regions. You can also use it to view routing information and influence place and route for more optimal results. This tool is particularly useful when you need maximum control over your design placement.

Note: ChipPlanner supports the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families. If you are designing for the MX, eX, SX, or SX-A families, use ChipEditor. For more information about ChipEditor, see the ChipEditor online help or *ChipEditor User's Guide*.

Use ChipPlanner to:

- View macro assignments made during layout
- Assign, unassign, or move macros
- Lock macro assignments
- View net connections using a ratsnest or route view
- View architectural boundaries
- View and edit silicon features, such as I/O banks
- Create regions and assign macros or nets to regions (floorplanning)
- View placement and routing of paths when used with Timer

Using PDC Files (ProASIC3E, ProASIC3, and Axcelerator only)

Any constraint that you can enter using ChipPlanner, you can also enter using a Physical Design Constraint (PDC) file. A PDC file is a Tool Command Language (Tcl) script file specifying physical constraints. This file can be imported and exported from Designer. PDC files replace the PIN file for the Axcelerator family.

Using GCF Files (ProASIC and ProASIC PLUS only)

Any constraint that you can enter using ChipPlanner, you can also enter using a GCF file. A GCF file is a constraint file specifying placement or timing constraints. This file can be imported and exported from Designer.

See the *Designer User's Guide* for more information about PDC and GCF files.

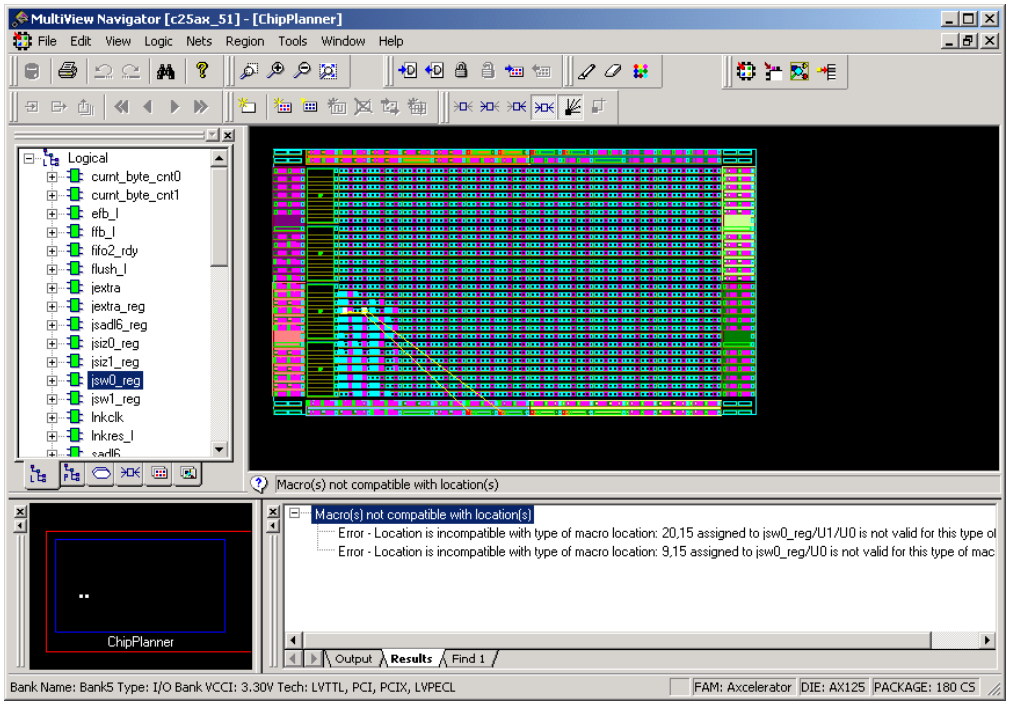
Starting ChipPlanner

ChipPlanner requires a compiled design. If you start ChipPlanner before compiling your design, Designer guides you through the compile process before opening ChipPlanner.

To start ChipPlanner from Designer, either click the **ChipPlanner** icon in the Designer Design Flow window, or from the **Tools** menu, choose **ChipPlanner**.

To start ChipPlanner from within MVN, either click the **ChipPlanner** button in the MVN toolbar, or from the **Tools** menu, choose **ChipPlanner**.

ChipPlanner opens in the Tools window of the MultiView Navigator interface and displays pins and I/O macro assignments. For ProASIC3E, ProASIC3, and Axcelerator families, it also displays I/O banks.

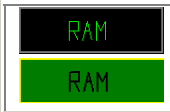
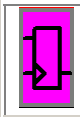


ChipPlanner in MultiView Navigator

When you select an assigned macro, the macro location appears selected in the World window, and the I/O macro name is selected in the Logical and Physical hierarchy tabs.

Colors and Symbols

Colors and symbols differentiate the I/O and logic macros in ChipPlanner. The following table defines the default colors assigned to symbols. You can change these colors per design.

Color/Symbol	Definition
White Border	A white border denotes a selected object.
Black Background	A black background denotes an unused or unassigned module.
Blue	Blue denotes a combinatorial module.
Yellow	Yellow denotes *locked* logic modules. If the module is selected, the symbol appears yellow. If the module is unselected, the border appears yellow.
Green	Green denotes I/O modules.
Red	Red denotes clock modules.
Magenta	Magenta denotes sequential modules.
	Reserved modules that are not user definable are gray, crossed-out symbols on a black background.
	Clock modules are red. Unused/unassigned modules are red symbols on a black background. Used/assigned modules are black symbols on a red background.
	Input/Output modules are green. Unused/unassigned modules are green symbols on a black background. Used/assigned modules are black symbols on a green background.
	Combinatorial modules are blue. Unused/unassigned modules are blue symbols on a black background. Used/assigned modules are black symbols on a blue background.
	Sequential modules are magenta. Unused/unassigned modules are magenta symbols on a black background. Used/assigned modules are black symbols on a magenta background.
	Buffer modules are blue.
	RAM modules are green. Unused/unassigned modules are green symbols (RAM) on a black background. Used/assigned modules are black on a green background.
	PLL modules are green. Unused/unassigned modules are green symbols (PLL) on a black background. Used/assigned modules are black on a green background.
	I/O Inbuff modules are pink on a black background. Used/assigned modules are black on a pink background.

Committing Changes

Changes you make are not permanent until you use the Commit command. The Commit command saves your changes to your design session. Changes are not reversible. To commit your changes, from the **File** menu, choose **Commit**.

Setting ChipPlanner Properties

You can bring the selected macro or net into view in ChipPlanner by setting the **Move the display to show Selected Macro** and **Center display around Selected Net** properties:

The first property brings the selected macro into view in the ChipPlanner window. Likewise, the second one brings the selected net into view and zooms into the selected net. By default, both properties are selected. If you do not want your viewing area to change when you select a macro or net, you can clear these check boxes.

To set ChipPlanner properties:

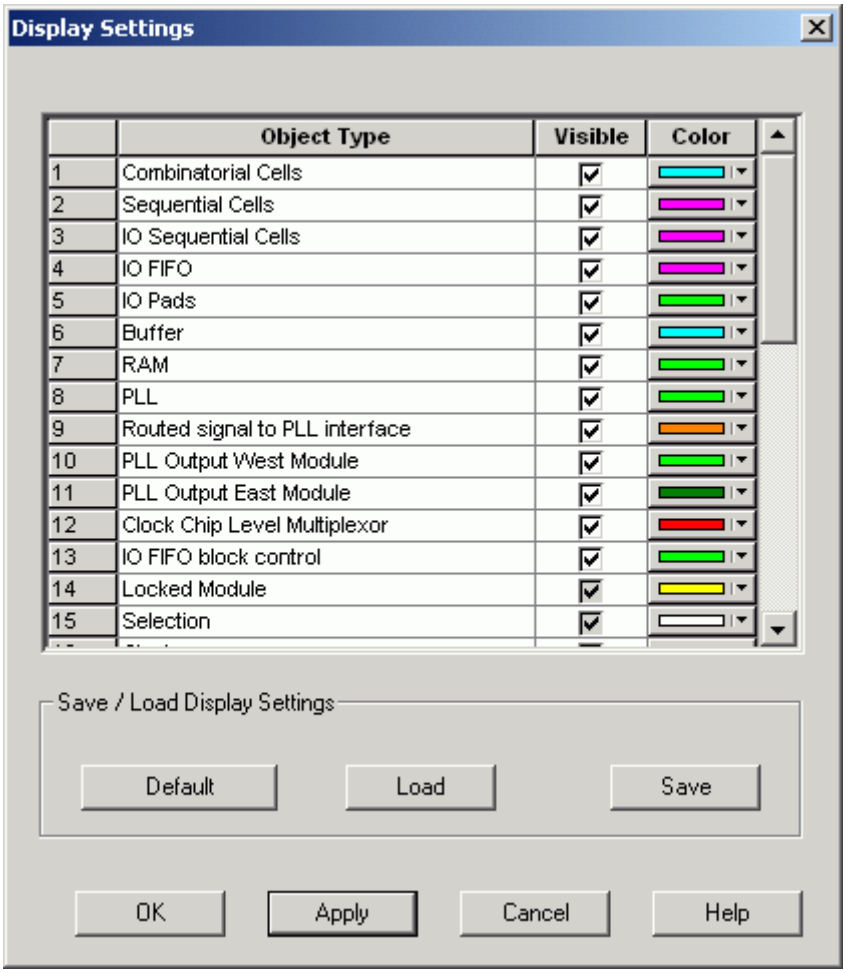
1. From the **View** menu, choose **Properties**.
   Note: You can also right-click anywhere in the ChipPlanner window, except on a region, and choose Properties from the right-click menu.
2. In the **ChipPlanner Properties** dialog box, clear one or both check boxes.
3. Click **OK**.

Changing Colors

You can control which objects are visible in your design and what color they are.

To set display properties:

1. From the **View** menu, choose **Display Settings**. The Display Settings dialog box displays a list of all the architectural features you can turn on and off in your tool.
2. To make an object visible, select the **Visible** check box.
3. To change the color used to display the object, click its color bar and select another color.
4. To save or open previously saved display settings, click:
   - **Save** to save your display settings to a file.
   - **Load** to open a saved display settings file.
   - **Default** to load the default display settings.
5. Click **Apply** to see your changes.
6. Click **OK** to dismiss the dialog box.



Display Settings Dialog Box in ChipPlanner

Floorplanning

Floorplanning includes creating regions and making logic assignments to those regions. It is an optional methodology you can use to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be clustered within regions. Clustering is especially helpful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try clustering the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing.

Use ChipPlanner before and after Layout to help you floorplan.

Regions

A region is a user-defined area on the device. When floorplanning, you can assign logic to regions to improve the design performance. You can use ChipPlanner to create regions or create them with PDC or GCF commands.

ChipPlanner supports the following types of regions:

Logic Region (Inclusive/Exclusive)

A Logic region is a region that has logic assigned to it. Logic may include core logic, memory, and I/O modules. The place-and-route tool will place all the logic assigned to a Logic region inside that region. The floorplanning process usually requires you to create several regions and assign logic to them.

Logic regions can either be inclusive or exclusive. If a Logic region is exclusive, it means that the placement tool cannot place any logic within the region other than what you have previously assigned to it. If a Logic region is inclusive, the place-and-route tool can place any logic within the region. Exclusive regions are not supported for ProASIC and ProASIC PLUS devices. However, exclusive regions are supported for ProASIC3 and ProASIC3E devices.

Empty Region

To prevent logic from being placed within a predefined area in the device, you can create an empty region. The place-and-route tool will not place any logic within an empty region; however, the routing resources within the region can be used.

LocalClock Regions

A LocalClock is a portion of the global clock network on the device. LocalClock regions are inclusive by default and cannot be changed. Each family has different LocalClock capabilities. For specific details, see the datasheet for your device.

QuadrantClock Regions

A QuadrantClock is a portion of the global clock network on the device. Each family has different QuadrantClock capabilities. For specific details, see the datasheet for your device. You create and delete a QuadrantClock in the same way that you create a LocalClock in ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC devices.

Overlapping Regions

If you create Logic regions whose areas intersect, the regions are defined to be overlapping. The place-and-route tool will detect the area where these regions intersect and try to place logic common to both of them within this area.

Creating Regions

With ChipPlanner, you can create empty, exclusive, inclusive, QuadrantClock, and LocalClock regions under certain conditions:

Region Type	Conditions
Empty	• Cannot assign macros to an empty region • Cannot create empty regions in areas that contain locked macros
Exclusive	• Only contains macros assigned to the region • Not supported in ProASIC and ProASIC PLUS • Cannot create exclusive regions in areas that contain locked macros
Inclusive	• Contains all macros, both assigned and unassigned to the region
LocalClock	• Can create LocalClock regions for ProASIC and ProASIC PLUS devices either in ChipPlanner or in a GCF file • Can create LocalClock regions for ProASIC3E, ProASIC3, and Axcelerator devices in a PDC file • Cannot resize or move a LocalClock region • Cannot assign logic to a LocalClock region
QuadrantClock	• Can assign CORE, RAM, and I/Os to QuadrantClock regions that are inclusive

To create an empty or logic region:

1. From the **Region** menu, choose **Create Empty, Create Exclusive,** or **Create Inclusive**.
2. While holding down the left mouse button, drag the mouse over the area where you want the region to be placed. As you drag out the region, a tooltip appears in its lower-right corner, showing you how many tiles, RAMs, and I/Os are in the region.

To create a LocalClock region:

1. In the **Net** tab of the Hierarchy window, select a clock net.
   Clock nets have a clock icon next to them in Net view.
2. From the **Region** menu, choose **Create LocalClock**, or click its icon in the toolbar.
3. Drag a rectangle from the top-left corner of the new LocalClock region to its bottom-right corner. As you drag out the region, a tooltip appears in its lower-right corner, showing you how many tiles, RAMs, and I/Os are in the region.

Note: See "Creating LocalClock regions" for more information.

To create a QuadrantClock region:

1. In the **Net** tab of the Hierarchy window, select a clock net.
   Clock nets have a clock icon next to them in the Net view.
2. From the **Region** menu, choose **Create QuadrantClock**, or click its icon in the toolbar. "Select a point in the Chip..." appears in the status bar.

3. Select a point in the chip that is driven by QCLK. ChipPlanner creates a QuadrantClock region for the given net. The region name is Qclock_<netname> and appears in the **Regions** tab of the Hierarchy View window. A tickmark appears next to the net in the Net tab and next to all the macros driven by it.

Note: See "Creating a Quadrant Clock," and "Creating QuadrantClock regions" in this guide for more information.

Using Empty Regions

Empty regions allow you to create exclusive areas on the device where no logic placement can occur. Empty regions help guide the placer to pack your logic closer together and thereby use more local routing resources to connect it. You cannot create empty or exclusive regions in areas that contain locked macros. Use the following guidelines for empty regions.

Use Empty Regions to Guide the Place-and-Route Process

If your design does not completely use up your target device (for example 60% utilization or lower), use empty regions to cluster your logic placement into specific subareas) of the chip. This helps when you have originally placed and routed the design into a smaller device but want to fit it to a larger part while still preserving the performance you have achieved in the smaller device.

Use Empty Regions to Reduce Routing Congestion

Creating empty regions next to the congested area(s) of your design helps reduce congestion. When you place an empty region next to congested logic blocks or regions, the placer cannot place any logic next to your region or logic block. Logic, which would normally be placed there, is forced to be placed somewhere else. Routing resources next to the congested area are, therefore, freed up and provide the router more options to route signals into the congested block.

Before deciding to place empty region(s), analyze your design for congestion areas. Use the **Ratsnest** view in ChipPlanner to see dense areas of connectivity into and out of your logic blocks or regions. Create empty regions in these congested areas and see it if improves the routability of your logic.

Use Empty Regions to Reserve Device Resources

If you want to preserve the placement of your existing design but plan additional modifications in the future, create empty regions in the areas of the chip where you plan to add additional logic. As you add new logic, remove or resize your empty regions accordingly to fit your new logic. Empty regions placed over I/O pins reserve them for future use as the I/O needs of your design changes. There are some restrictions for using empty regions in this manner. See the *Floorplanning ProASIC/ProASIC* ^{PLUS} *Devices for Increased Performance* application note for more details.

Using Logic regions

Use Logic regions to compact the placement of certain logic blocks in your design. This allows you to control logic placement at the region or block level. This may simplify your floorplanning task, since you might not have to place logic instances individually on the device. The following sections contain guidelines for using Logic regions.

Use Logic Regions to Localize Placement of Logic Blocks

If you partitioned your design into several modules, and some of these modules contain regular structures (such as arithmetic logic, register arrays, counters, or multiplexors), place these modules into Logic regions. These logic functions have a good amount of both local connectivity and regularity to their structure, which makes them good candidates for regions. Interconnects between your regions now become interconnects between hierarchical blocks in your design. Floorplan your regions so there is a smooth horizontal or vertical data flow between each Logic region.

For Pipelined Logic, Place Registers on Region Boundaries

If you assigned logic to a region so its inputs and outputs are bounded by a register array (pipeline registers), it is a good idea to place these pipeline registers close to the boundary of the region. If you plan to manually fix the placement of your pipeline registers, make sure you orient them in the correct direction to assure a smooth data flow between them and their interfacing logic.

Aligning RAM I/O with Placement

Before placing your memory blocks, review your design and understand how data is flowing into and out of them. Determine what logic blocks are driving the memory inputs (for example, address line, control signals) and what logic is driven by the memory outputs (for example, databus lines). Follow these guidelines:

- Place pins that drive or are driven by your memory blocks close to where your memory blocks are placed.
- Create an empty region next to your memory block to free up local routing resources that may need to be used to connect to the memory blocks.
- If you are driving high fan-in memory inputs such as read/write clocks or read/write enables, try using low-skew routing resources such as global nets or clock spines to connect them. Make sure your clock spine assignments are aligned with your RAM placement.

Using LocalClock and QuadrantClock Regions

Use a QuadrantClock when you want to drive all instances within one quadrant. Use a LocalClock when you want to drive instances within the entire chip.

Families	Create LocalClock Region in ChipPlanner?	Create LocalClock Region using PDC or GCF file?	Create QuadrantClock Region in ChipPlanner?	Create QuadrantClo Region usin PDC or GC file?
ProASIC3E	No	Yes, PDC file	Yes	Yes, PDC file
ProASIC3	No	Yes, PDC file	Yes	Yes, PDC file
ProASIC PLUS	Yes	Yes, GCF file	No	No
ProASIC	Yes	Yes, GCF file	No	No
Axcelerator	No	Yes, PDC file	No	No

See the *Floorplanning ProASIC/ProASIC PLUS Devices for Increased Performance* application note for more information about assigning LocalClocks.

Editing Regions

After creating regions, with the exception of LocalClock regions, you can rename, delete, move, and re-size them. LocalClock regions can only be renamed or deleted.

Regions must have unique names. Two regions cannot have the same name.

To change the name of a region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the region with the name you want to change.
3. From the **Region** menu, choose **Properties**.
4. In the **Properties** dialog box, type the new region name over the existing one.

Tip: You can also right-click a region, choose **Properties**, and type a new region name in the **Properties** dialog box.

To delete a region:

- Right-click the region, and chose **Delete**.

To move a region:

- Select the region and drag it to a new location.

Note: You cannot move the region if a macro assigned to the region is locked.

To re-size a region:

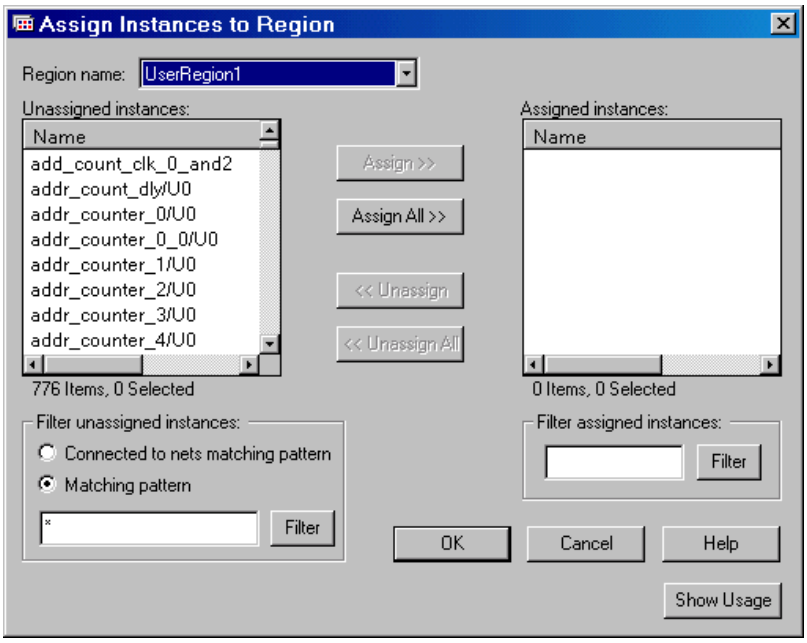
1. Select the region.
2. Grab and drag the sides and corners to re-size the region. You cannot resize a region smaller than the logic it already contains.

Assigning a Macro to a Region

During floorplanning, you can improve design performance by assigning macros to regions.

To assign a macro to a region:

1. Right-click a region and choose **Assign/Unassign**. The **Assign Instances to Region** dialog box appears with the name of the selected region in the **Region name** field. The dialog box displays all of the macros that you can assign to the selected region.



Assign Instances to Region Dialog Box

2. To display a subset of the unassigned instances, you can create and apply filters. To filter the unassigned instances list by a pattern, enter the pattern (string) in the text box to the left of the Filter button, select **Matching pattern**, and then click **Filter**. Only the instances that match the pattern appear in the **Unassigned Instances** list. For example, enter *U18* to display only unassigned instances containing the characters U18.

3. To assign specific instances to the region, select one or more instances in the **Unassigned Instances** list box, and then click **Assign**. To assign all instances to the region, click **Assign All.**
4. Click **OK**.

Note: The total number of instances that you can assign as well as the number of currently selected unassigned instances appears under the list box.

Tip: You can also assign logic to regions from the Hierarchy window. Just drag and drop the logic from the Hierarchy window to the region.

Assigning a Net to a Region

When assigning a net to a region, only the instances driven by the net are assigned to the region.

Assigning nets to a region allows you to control the net delays of logic connected to certain nets in the design. You can adjust the size of the region to pack logic more closely together, hence, improving its net delays.

To assign a net to a region:

1. Right-click a region and choose **Assign/Unassign**. The **Assign Instances to Region** dialog box appears with the name of the selected region in the **Region name** field. The dialog box displays all of the macros that you can assign to the selected region.
2. To display a subset of the unassigned instances, you can create and apply filters. To filter the unassigned instances list by a net name, enter it in the text box to the left of the Filter button, select **Connected to nets matching pattern**, and then click **Filter**. The **Unassigned Instances** list displays only macros assigned to the net name you specified. For example, enter add_count_clk to display only macros assigned to the net named add_count_clk.
3. To assign specific instances, select one or more instances in the **Unassigned Instances** list box, and click **Assign**. To select all instances, click **Assign All**.
4. Click **OK**.

Note: The total number of instances that you can assign, as well as the number of currently selected unassigned instances, appears under the list box.

Unassigning a Macro from a Region

To unassign a macro from a region:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Region**.

Tip: You can also right-click the macro, and choose **Unassign From Region**.

Creating LocalClock Regions

For **ProASIC3E**, **ProASIC3**, and **Axcelerator** devices, you can use a PDC file to create LocalClock regions. For **ProASIC PLUS** and **ProASIC** devices, you can create LocalClock regions in ChipPlanner or define them in a GCF file. See the *Floorplanning ProASIC/ProASIC PLUS Devices for Increased Performance* application note for more information.

When you create a LocalClock region, the selected net and all the macros driven by that net are assigned to the LocalClock region.

To create a LocalClock region from the MVN Hierarchy window:

1. In the **Net** tab of the **Hierarchy** window, select a clock net.
   Clock nets have a clock icon next to them in the **Net** view.
2. From the **Region** menu, choose **Create LocalClock**, or click its icon in the toolbar.
3. Drag a rectangle from the top-left corner of the new LocalClock region to its bottom-right corner. As you drag out the region, a tooltip appears in its lower-right corner showing how many tiles, RAMs, and I/Os are in the region.

Note: A net that is already assigned to a LocalClock region cannot be assigned to another non-overlapping region.

For ProASIC and ProASIC PLUS families, the RAMs and I/Os are assigned to the LocalClock region unless the Compile option "Include RAM and I/O in Spine and Net Regions" is cleared. See "Compile Options" in the online help for more information.

The default name of the LocalClock region is LocalClock_<netname> (for example, LocalClock_exl_d_0), and its type is inclusive.

Designer does not support exclusive LocalClock regions. LocalClock regions are inclusive by default, and you cannot change their type.

Note: To assign a signal to a spine, the spine itself and the entry MUX must be free. However, this does NOT necessarily require the corresponding global network to be unused. For example, you can assign non-global signals to spines when four global networks are used by other high-fanout nets. For more information, refer to the application note *Optimal Usage of Global Network Spines in ProASIC PLUS Devices*, which is available from the Actel web site.

Renaming a LocalClock Region

To change the name of a LocalClock region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the LocalClock region with the name you want to change.
3. From the **Region** menu, choose **Properties**.
4. In the **Properties** dialog box, type the new region name over the existing one.

Tip: You can also right-click on the region name, and choose **Properties** to display the region's properties. Type the new name over the old one in the **Properties** dialog box.

Creating QuadrantClock Regions

You can create QuadrantClock regions only for ProASIC3E and ProASIC3 devices.

To create a QuadrantClock region:

1. In the **Net** tab of the **Hierarchy** window, select a clock net.
   Clock nets have a clock icon next to them in the Net view.

2. From the **Region** menu, choose **Create QuadrantClock**, or click its icon in the toolbar. "Select a point in the Chip..." appears in the status bar.
3. Select a point in the chip that is driven by QCLK. ChipPlanner creates a QuadrantClock region for the given net. The region name is Qclock_<netname> and appears in the **Regions** tab of the Hierarchy window. A tickmark appears next to the net in the **Net** tab and next to all the macros driven by it.

Under the following conditions, ChipPlanner does not create a QuadrantClock region and displays an error message in the Log window:

- A net is not selected or more than one net is selected.
- The selected net is already assigned to a QuadrantClock region.
- Any macros connected to the selected net are locked outside of the region.
- Any macros connected to the selected net are assigned to a region that does not overlap the QuadrantClock region.
- The macros connected to the net exceed the capacity of the quadrant clock.

Note: You can also create a QuadrantClock using the assign_local_clock command in a PDC file.

Assigning a Clock to a QuadrantClock Region

You can assign a clock to a QuadrantClock region either using the ChipPlanner tool in the MultiView Navigator or using a PDC file.

In ChipPlanner, you can assign a clock to a quadrant clock in one of the following ways:

- Assign a clock macro (not hardwired to an I/O) to a QuadrantClock region using the ChipPlanner tool
- Assign a clock macro (hardwired to an I/O) to an I/O location using either the PinEditor or I/O Attribute Editor tool, or to an I/O module location that drives a QuadrantClock region using the ChipPlanner tool
- Assign a regular net to a QuadrantClock region

Using a PDC file, you can assign a clock to a QuadrantClock in one of the following ways:

- Assign a clock macro (not hardwired to an I/O) to a QuadrantClock region using the **`assign_local_clock`** command
- Assign a clock macro (hardwired to an I/O) to an I/O location (**`set_io`**) or to an I/O module location (**`set_location`**) that drives a QuadrantClock region
- Assign a net driven by a regular net or a clock net to a QuadrantClock region using the following command:

  `assign_local_clock -net <net name> -type quadrant <QuadranClock region>`

  where

  `<net name>` is the name of the net assigned to the LocalClock region

  `<quadrant clock region>` is the QuadrantClock region to which the net should be assigned. QuadrantClock regions are defined as UL (upper left), UR (upper right), LL (lower left), and LR (lower right)

Note: If the net assigned to the LocalClock is a regular net, Designer inserts a QCLKINT on the net.

See set_io and set_location in the *Designer User's Guide* for more information.

Assigning Logic to Locations

Manually assigning logic is an optional methodology to help you improve the performance and density of your design.

You do not need to manually assign logic to particular locations in your design. However, should you have specific design requirements, ChipPlanner allows you to have maximum control over your design.

To assign logic to specific locations:

1. Select the logic in the **Physical** tab of the **Hierarchy** window.
2. Drag the logic to the desired location. As you drag, valid assignment locations are highlighted. To remove the assignment, from the **Edit** menu, choose **Undo**.

   If the logic assignment is valid, the logic is assigned and locked. To save changes for this design session, commit your changes when exiting the MultiView Navigator.

To assign logic to multiple locations:

1. While holding down the **CTRL** or **SHIFT** key, select the logic in the order you want it placed.
2. From the **Logic** menu, choose **Assign To Location**.
3. One by one, select the desired locations. The macros are placed in the order selected.

To unassign logic from a location:

1. Select the logic.
2. From the **Logic** menu, choose **Unassign From Location.**

To unassign logic from multiple locations:

1. While holding down the **CTRL** or **SHIFT** key, select the logic you want to unassign. To select all logic, from the **Edit** menu, choose **Select All**.
2. From the **Logic** menu, choose **Unassign From Location**.

Moving Logic to Other Locations

You can move logic that was assigned manually or automatically during Layout.

To move logic:

1. Select the logic to move.
2. Drag the logic to the new location.

Tip: To remove the assigned macro, from the **Edit** menu, choose **Undo.**

Locking Logic to Locations

Locked logic is not moved during Layout. Locked logic only becomes permanent if you commit the changes to your design before exiting.

To lock macros:

1. Select the macro to lock. To select multiple macros, hold down the **CTRL** key and select multiple macros with your mouse. To select all macros, from the **Edit** menu, choose **Select All**.
2. From the **Logic** menu, choose **Lock**.
3. From the **File** menu, choose **Commit** to save your changes in this session. To save your changes in the design file (.adb), you must save your design in Designer as well.

To unlock a macro:

1. Select the macro. To select multiple macros, hold down the **CTRL** key and select multiple macros. To select all macros, from the **Edit** menu, choose **Select All**.
2. From the **Logic** menu, choose **Unlock**.

Ratsnest View

The Ratsnest view displays net connectivity between assigned logic macros by connecting lines from all output pins to all input pins. Use the Ratsnest view to understand how logic macros are connected to each other. The Ratsnest view is activated by default, showing all input and output nets for the selected macro.

To display the Ratsnest view:

1. From the **Nets** menu, choose **Show Input Only**, **Show Output Only**, or **Show Input & Output**, or click the corresponding Net toolbar button, to indicate which nets you want to see.
2. From the **Nets** menu, choose **Show Ratsnest**, or click the **Ratsnest** button in the toolbar.
3. Select the assigned macro in the ChipPlanner window. ChipPlanner displays all nets connected to the assigned macro. See nets assigned to multiple macros by holding down the **CTRL** key while you click on each assigned macro.

Route View

Note: This feature is available only for ProASIC3/E, ProASIC PLUS, and ProASIC devices.

The Route view displays a representation of the routes. This feature shows the general location of routing segments used by the design.

To activate the route view in ChipPlanner:

1. Complete **Layout**. To display routes, Layout must be completed before running ChipPlanner.
2. Select the assigned macro in either the **ChipPlanner** window or the **Physical** tab of the **Hierarchy** window. Select multiple macros by holding down the **CTRL** key.
3. From the **Nets** menu, choose **Show Routes**, or click the **Show Routes** toolbar button.

Clusters and SuperClusters

Note: This feature is only available for the Axcelerator family.

A cluster is a group of logic elements. The type of elements that make up the cluster is determined by the device type.

A SuperCluster is two clusters and a buffer. Modules in a cluster can be connected by fast or direct connects.

Use these areas as guides to ensure that specific nets can be implemented using fast or direct connects. Nets that connect within a rectangle can be implemented as fast or direct connects, depending on availability. For details about fast connects and direct connects, please see the FPGA datasheet for your device on the Actel web site.

To view clusters or SuperClusters:

1. From the **View** menu, choose **Display Settings**. The **Display Settings** dialog box appears.
2. Select the **Visible** check box for **Cluster** or **SuperCluster**.
3. Click the **color bar** and select a color to change its display color.
4. Click **OK**.

Using I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip.

ProASIC3E and Axcelerator

ProASIC3E and Axcelerator devices have eight I/O banks surrounding the chip, two per side, numbered 0-7. The I/O banks are color-coded for quick identification. You can change the default colors through the Display Settings dialog box.

Each I/O bank has a common:

- VCCI, the supply voltage for its I/Os
- VREF, the reference voltage (for voltage-referenced I/O standards)

You can assign only one VREF pin to each I/O bank. Only I/O standards compatible with both the same VCCI and VREF standards can be assigned to the same bank. The following table shows the required voltage values and their compatible I/O standards for Axcelerator devices.

VCCI	Compatible I/O Standards
3.3V	LVTTL, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, LVPECL
2.5V	LVCMOS 2.5, GTL+ 2.5, SSTL2 (Class I & II), LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5, HSTL (Class I)

The following table shows the required voltage values and their compatible I/O standards for ProASIC3E devices.

VCCI	Compatible I/O Standards
3.3V	LVTTL, LVCMOS 3.3, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, GTL 3.3, LVPECL
2.5V	LVCMOS 2.5, LVCMOS 2.5/5.0, GTL+ 2.5, GTL 2.5, SSTL2 (Class I & II), LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5, HSTL (Class I), HSTL (Class II)

Note: The low-power mode and input delay attributes are not available in the I/O Bank Settings dialog box for ProASIC3E and ProASIC3 devices. Because these attributes are not available, the More Attributes button is also not available.

Banks are visible in both ChipPlanner and PinEditor. Information about banks appears in the MultiView Navigator's status bar.

ProASIC3

ProASIC3 devices have two, four, or eight I/O banks surrounding the chip, one per side, numbered 0-1, 0-3, or 0-7, respectively. Each I/O bank has dedicated resources for an input/output supply voltage (VCCI). Because of these dedicated resources, you can assign only I/Os with compatible standards to the same I/O bank. The following table shows the required voltage values and their compatible I/O standards.

VCCI	Compatible Standards
3.3V	LVTTL, PCI 3.3, LVPECL, LVCMOS
2.5V	LVCMOS 2.5/5.0, LVDS
1.8V	LVCMOS 1.8
1.5V	LVCMOS 1.5

On some dies, the left and right side of the chip have a different selection of I/O standards (LVDS/LVPECL). Because the dies do not need an input referenced voltage (VREF), the **Use Pin for VREF** and **Highlight VREF Range** commands are unavailable from the right-click menu. Also, because the low-power mode and input delay attributes are not available, the **More Attributes** button is not available in the I/O Bank Settings dialog box.

Note: ProASIC3 devices do not support the Input Delay attribute.

Specifying Standards for an I/O Bank

You can specify standards for each I/O bank by doing one of the following:

- Using the I/O Bank Settings dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage
- Using the command `set_iobank` in a PDC file

You cannot change the I/O standard of an assigned I/O to an I/O standard that is incompatible with the bank. If you need to assign the I/O standard to a new technology, first unassign the I/O.

Assigning Technologies to I/O Banks

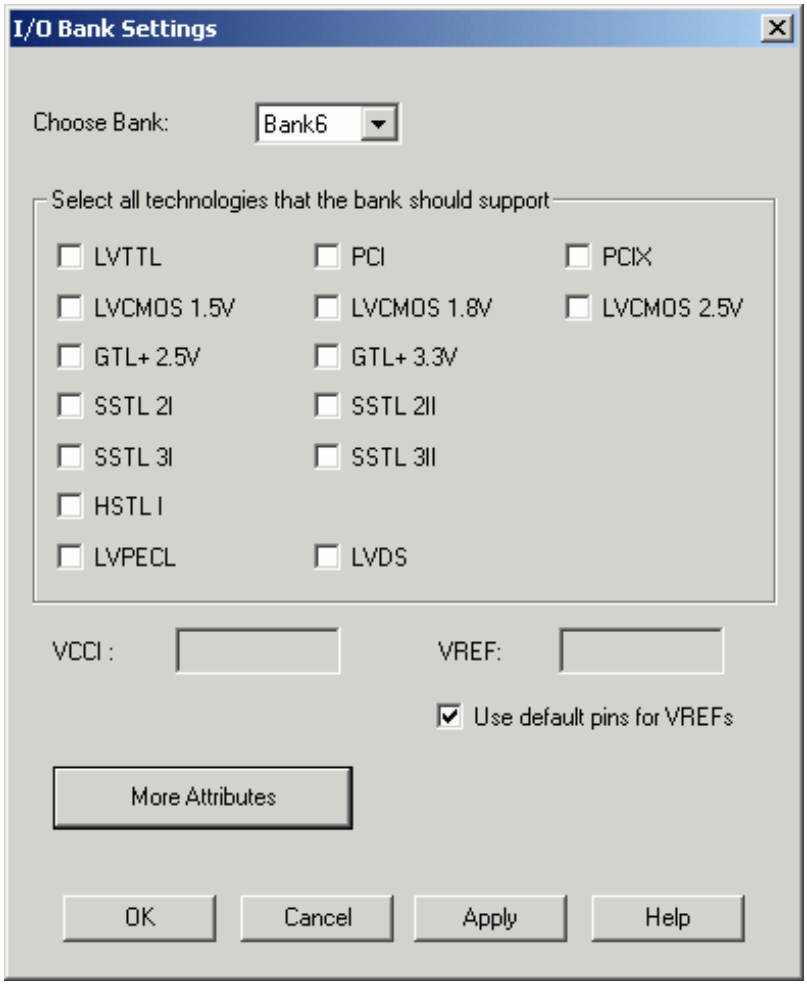
The procedure for assigning technologies to I/O banks differs depending on whether you are designing for ProASIC3E, ProASIC3, or Axcelerator devices.

To assign technologies to I/O banks in Axcelerator and ProASIC3E devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further, selecting GTLP (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Click **More Attributes** to set the low-power mode and input delay. (These attributes are not supported in RTAXS, ProASIC3, and ProASIC3E devices.)

5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
6. Leave the **Use default pins for VREFs** option selected to set default VREF pins and unset non-default VREF pins. If you unselect this option when setting a new VREF technology, no VREF pins are set. If you unselect this option when default VREF pins are already set, it unsets them.

   If the **Use default pins for VREFs** option is selected when you click **OK** or **Apply**, the software: 1) determines if setting default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, 2) determines if unsetting non-default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, and 3) sets default VREF pins and unsets non-default VREF pins.
7. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.



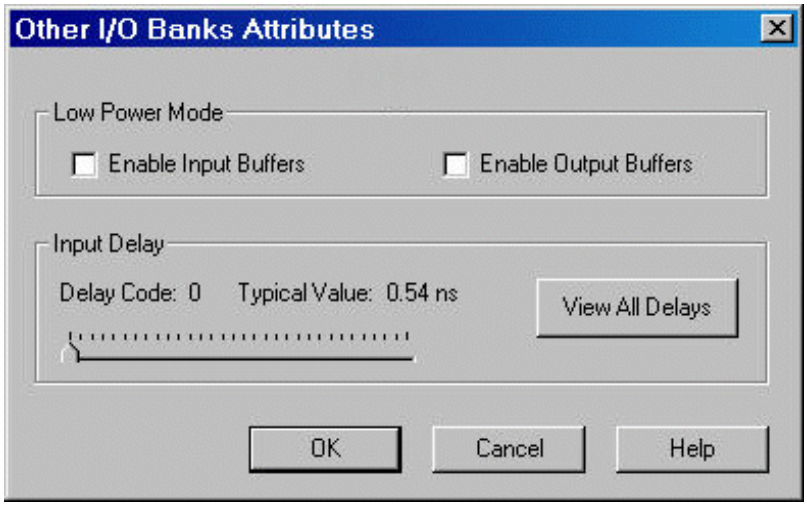
I/O Bank Settings Dialog Box for ProASIC3E and Axcelerator Devices

If VREF pins can be assigned, you must assign at least one VREF pin before running Layout. See "Assigning VREF Pins" in this guide for more information.

Note: If you use I/O standards that need reference voltage, make sure to assign VREF pins. Actel strongly recommends you use the defaults. VREF pins appear in red in ChipPlanner and are labeled VREF in PinEditor.

To set the low-power mode and input delay (for Axcelerator devices only):

1. Click **More Attributes** in the **I/O Bank Settings** dialog box.
2. Drag the slider bar to the desired delay. The delay is bank specific.
3. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. You must select a technology to see the input delays.
4. Click **OK**.

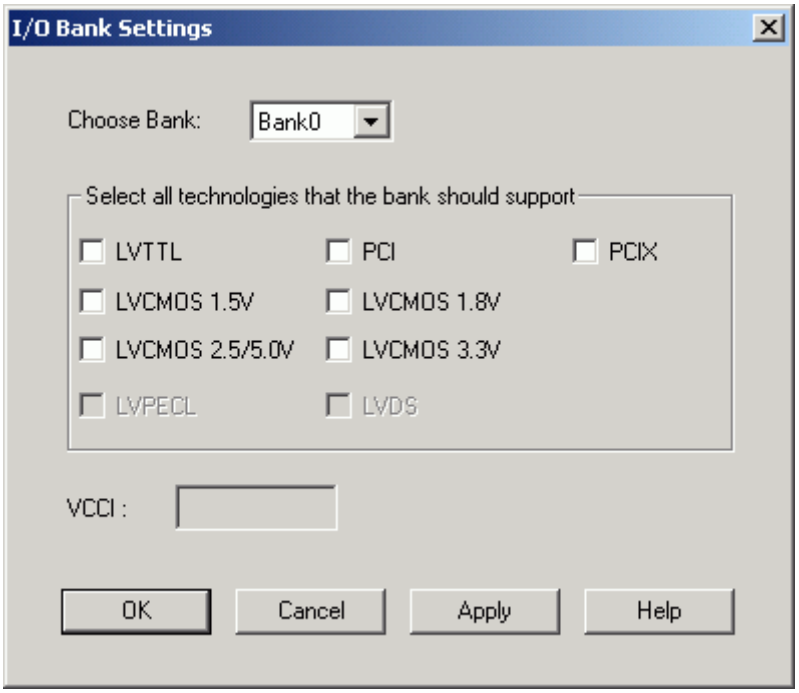


Other I/O Bank Attributes Dialog Box

Note: Low-Power Mode and Input Delay are not supported in RTAX-S, ProASIC3, and ProASIC3E devices.

To assign technologies to I/O banks in ProASIC3 devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Note that LVDS is available only for banks 1 and 3. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
5. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.



I/O Bank Settings Dialog Box for ProASIC3 Devices

Note: You cannot assign VREF pins in ProASIC3 devices.

Assigning Pins in ProASIC3E

To assign I/O in the ProASIC3E family:

1. From Designer's **Tools** menu, choose **Device Selection**. Select a die, package, speed, and die voltage, and click **Next**.
2. In the **Device Selection Wizard-Variations** dialog box, from the Default I/O Standard drop-down list, select the default I/O standard for all generic I/O macros. This action sets the same VCCI for each bank. You cannot choose LVDS or LVPECL as the default I/O standard. If your design has only one single-ended I/O and one VCCI requirement, go to step 8. Otherwise, in the next step you will specify the I/O standards for each I/O bank.
3. Start either **ChipPlanner** or **PinEditor**.
4. From the **Tools** menu, choose **I/O Bank Settings**.
5. In the **I/O Bank Settings** dialog box, choose an I/O standard for each I/O bank.
6. In ChipPlanner or PinEditor, assign VREF pins, if the standard requires VREF voltage. See Assigning VREF pins. In ProASIC3E, you can use any I/O as a VREF pin. The default VREFs setting may create more VREF pins than needed and may result in a loss of usable user I/Os. If that happens, you can choose the custom VREF setting. You must create enough VREF pins to allow a legal placement of the compatible user-voltage-referenced I/O macros. After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin.
7. After assigning VREF pins, from the **Tools** menu, choose **DRC** to check the I/O voltage assignment and to generate an I/O bank report. The I/O voltage Usage section in this report shows whether you have enough I/Os available for each voltage. Any infeasible voltage requirements appear as an asterisk (*) in the I/O voltage Usage report. If asterisks appear in your report, you should resolve the problem before continuing.

8. Once you have completed the I/O Bank assignments, you can assign I/O macros to individual pad locations using either the MultiView Navigator or a PDC file.

Note: Choosing Commit from the File menu also performs the DRC check.

Assigning VREF Pins

Voltage referenced I/O inputs (VREF) require an input referenced voltage. You must assign VREF pins to **Axcelerator** and **ProASIC3E** devices before running Layout.

Before assigning a VREF pin, you must set a VREF technology for the bank to which the pin belongs.

To set a VREF technology for a bank:

1. Select a bank in ChipPlanner.
2. From the **Tools** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select a technology such as GTL+ 3.3V so the VREF field displays a non-zero value.
4. Click **OK**. Now when you right-click on pins in this I/O bank, the VREF commands on the menu are enabled.

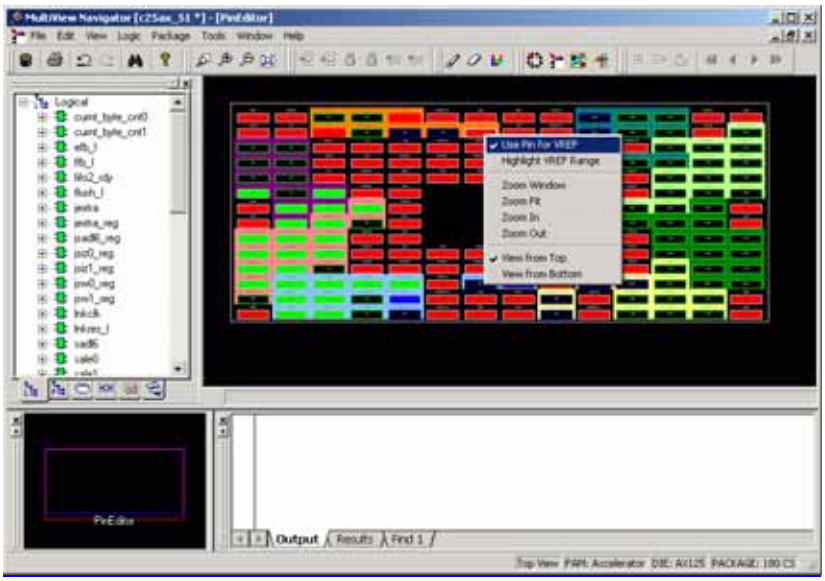
In either the PinEditor or ChipPlanner window, you can change a regular pin into a VREF pin from the right-click menu.

To assign a pin as a VREF pin:

1. In either PinEditor or ChipPlanner, select the pin to set as a VREF pin.
2. Right-click and choose **Use Pin for VREF**.

A check mark appears next to the **Use Pin for VREF** command in the right-click menu.

Note: The Use Pin for VREF command appears on the right-click menu only if you selected a pin in an I/O bank that supports VREF pins and for package pins or I/O modules that can become VREF pins.



Use Pin For VREF Command

Setting a pin as a VREF may result in I/O macros becoming unassigned, even if they are locked. In this case, a warning message appears so you can cancel this operation.

To unassign a VREF pin:

1. Select the pin to unassign.
2. Right-click and choose **Use Pin for VREF**. The check mark next to the command disappears. The VREF pin is now a regular pin.

Resetting the pin may result in unassigning I/O macros, even if they are locked. In this case, a warning message appears so you can cancel this operation.

Tip: You can also reset the **Use Pin for VREF** command by choosing **Undo** from the **Edit** menu.

After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin. To unhighlight the range, choose **Unhighlight All** from the **Edit** menu.

Displaying Pins in a VREF Range

You can see which pins in an I/O bank are serviced by a VREF pin. Use the right-click menu's **Highlight VREF Range** command while in PinEditor or ChipPlanner to see these pins.

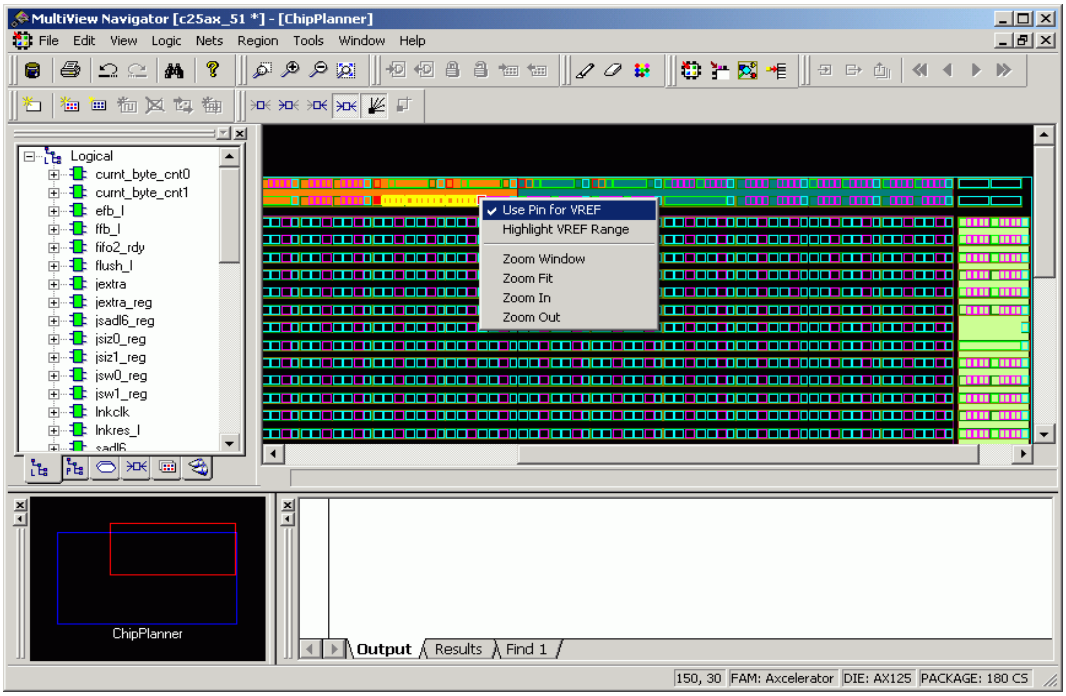
To display pins in a VREF range:

1. Right-click a VREF pin in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight VREF Range.**

When using PinEditor, all pins serviced by the selected VREF pin appear highlighted. In the following illustration, the pins serviced by the selected VREF pin are highlighted in orange.

Highlight VREF Range

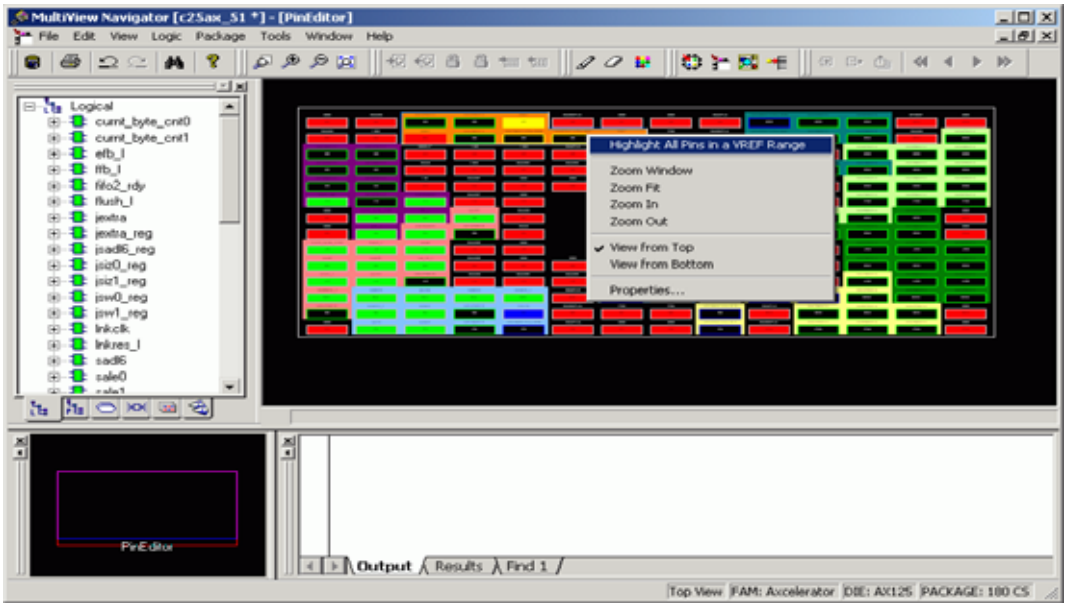
When using ChipPlanner, all I/O modules serviced by the selected VREF pin appear highlighted. The following illustration shows the right-click menu in ChipPlanner when a VREF pin is selected.



Right-click Menu in ChipPlanner

To highlight all pins in a VREF range:

1. Right-click an I/O bank in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight All Pins in a VREF Range.**



Highlight All Pins in a VREF Range

The **Highlight All Pins in a VREF Range** command appears in the right-click menu for all I/O banks that include a VREF pin.

All of the pins in the I/O bank that are serviced by a VREF appear highlighted. If the I/O bank does not contain a VREF pin, nothing is highlighted when you select this command.

To unhighlight all pins in a VREF range:

1. Select the highlighted range.
2. From the **Edit** menu, choose **Unhighlight All**.

Using ChipPlanner with Timer

Use ChipPlanner and Timer together to view place and route of paths in ChipPlanner.

To view paths:

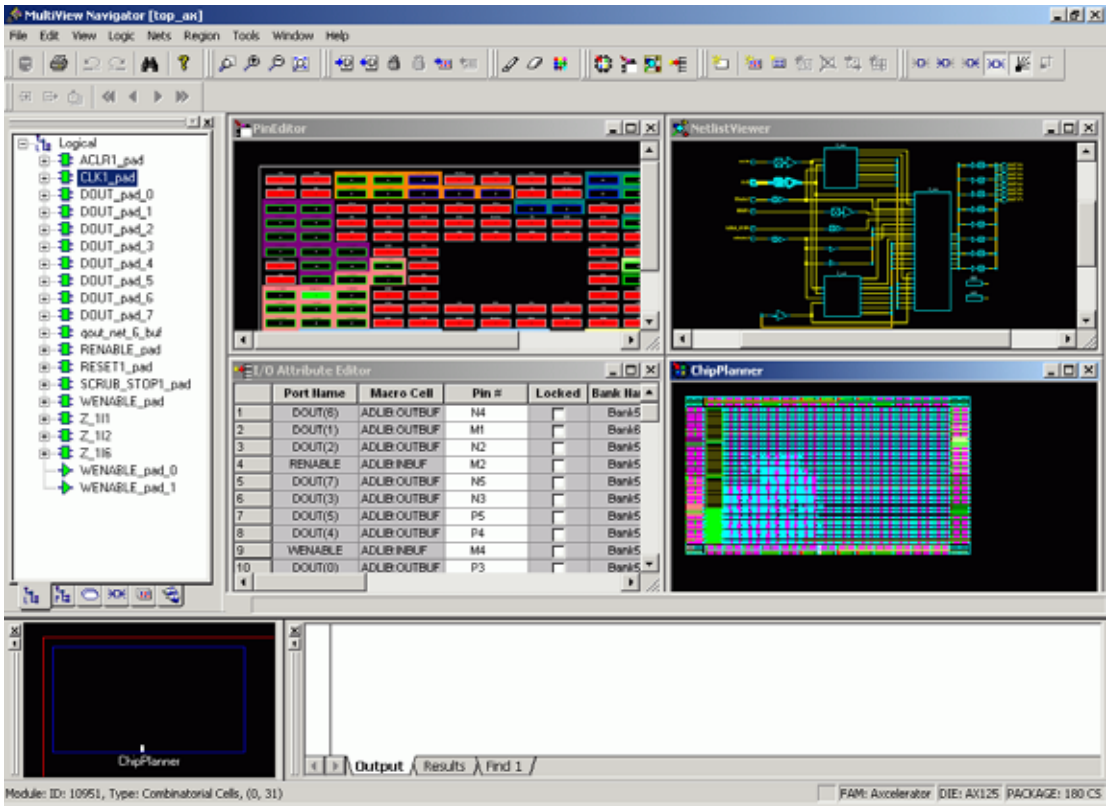
1. Open **Timer** and **ChipPlanner** from Designer.
2. In **Timer**, click the **Paths** tab.
3. Select a **Path** set in the path set grid. Paths within that set are displayed in the path grid.
4. Select the path you want to expand in the lower path grid.
5. Double-click the path to expand it, or from the **Edit** menu, choose **Expand Path**. The Expanded Paths window opens and displays a path in the **Expanded Paths** grid and a graphical representation of the path in the **Chart** window. The **Expanded Paths** grid shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge.
6. Anything selected in the **Expanded Paths** grid or **Graph** window is reflected in both windows.
   - Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
   - Selecting an instance, net, or macro in the Expanded Paths grid highlights that selection in the Chart window.
   - Selecting a logic macro in the Chart window highlights all instances of the macro in the Expanded Paths grid.
   - Toggle the **Graph window** on and off by choosing **Graph Window** from the **Window** menu. Use the commands on the **View** menu to zoom in and out. In the Graph window, dragging the mouse downward and to the left will make the selection fit within the window. Dragging down and to the right drags out a zoom in area.
   - In some cases, long instance names may overlap and be difficult to read in the Graph window. To resolve this, move the module. Select the module and while holding down the **SHIFT** key, click and drag the module to another location.
7. Select a module or net in the **Expanded Paths** dialog box. The module or net is shown in ChipPlanner.

Note: You can add and remove break points in Timer while using the ChipPlanner tool.

MVN Reference

Tools Window

In the MultiView Navigator interface, the Tools window is the area in which you view and edit your designs. Within this window, you can open a window for each tool: ChipPlanner, PinEditor, I/O Attribute Editor, and NetlistViewer. Logical Cone windows also appear in this window.



PinEditor, NetlistViewer, I/O Attribute, Editor, and ChipPlanner in the Tools Window

World Window

Use the World window to control which portion of the design appears in the active window of MultiView Navigator's Tools window. The blue rectangle represents the area of the chip. The red rectangle (known as the Viewing rectangle) represents the part of the design you see in a tool window.

To move the displayed area to another part of the design, click and drag the red rectangle to the area on the blue rectangle you want to see. To specify a new display area, right-click and drag out a new Viewing rectangle on the blue rectangle.

Log Window

The Log window displays information about your tool. This area also displays the results of any search that you perform. Click the tabs at the bottom of the window to view additional information. You can choose:

- **Output** (contains errors, warnings, and other information)
- **Results** (contains information about a message in the message bar)
- **Find1** (default, contains the results of a search)

Colors and Symbols

Messages are color-coded and represented by symbols. The default colors are:

Type	Color
Errors	Red
Warnings	Blue
Information	Black

You can change the colors in the Designer Preferences dialog box. However, you will not see your changes until you restart MultiView Navigator.

Output Tab

The Output tab displays all errors, warnings, and informational messages. It contains a complete history of your design session. Error and warning messages that are dark blue and underlined are linked to online help to provide details or helpful workarounds. Clicking an underlined message displays online help.

Results Tab

The Results tab displays the results of a command or other action. Clicking a message in the message bar displays more information in this tab. The view within this tab is reset when you execute a new command or open a new design. To see a complete history of your design session, click the **Output** tab.

Find Tab

The Find tab displays the results of a search performed with the **Find** command. You can create several Find tabs, one for each search (for example, Find1, Find2, or Find3). You can also drag and drop instances and ports from a **Find** output pane to the **ChipPlanner** window.

Tip: The right-click menu available from the **Hierarchy** window is also available from the Find tab.

Message Bar

The message bar displays errors, warnings, and other informational messages.

Clicking the icon to the left of the message in the message bar displays more information about the message in the **Results** tab of the **Log** window.

Tip: You can copy, show more information about, and clear a message from the right-click menu. Choosing **Copy** copies the message to the Clipboard, so you can paste it in another application. Choosing **Show More Info** displays more details about the message in the **Log** window. Choosing **Clear** erases the message from the Message bar.

Status Bar

Family, die, and package information appears in the right side of the status bar of the MultiView Navigator interface as shown in the example below:

To see other information in the status bar:

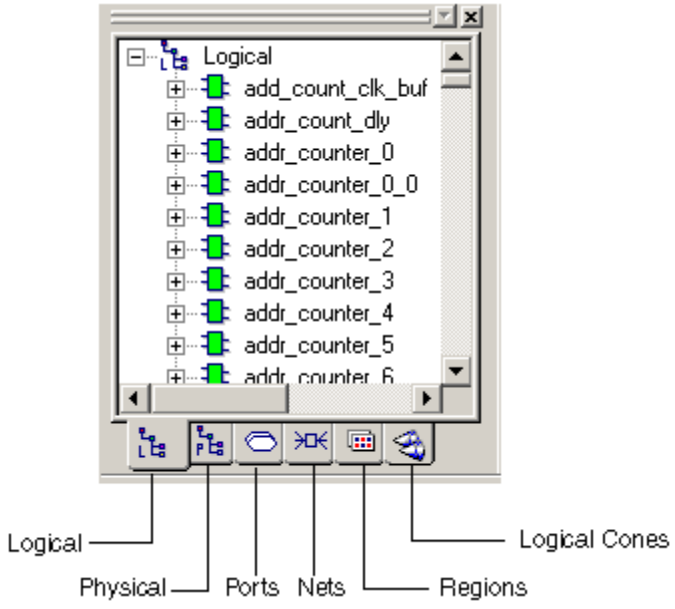
- Hold your mouse over an assigned macro to see the pin number, instance name, net name, macro cell, and locked or unlocked status bar.
- Hold your mouse over a module, instance, or bank in ChipPlanner to see information about it.
- Select a macro, zoom in, and click one of the ratsnest lines to see information about nets.
- Hold your mouse over a toolbar button or a menu command to see a short description of that command.

Note: For NetlistViewer, the current page number and the total number of pages also appear in the status bar.

Hierarchy Window

The leftmost window in MultiView Navigator is the Hierarchy window. The Logical tab in this window provides a hierarchical overview of the design.

Click the tabs at the bottom of this window to view macros, instances, ports, nets, regions, and logical cones in your design.



Hierarchy Window

Use these tabs to explore each level of the hierarchy and to trace signals. You use the Hierarchy window tabs with ChipPlanner, NetlistViewer, PinEditor, and I/O Attribute Editor to help identify critical paths.

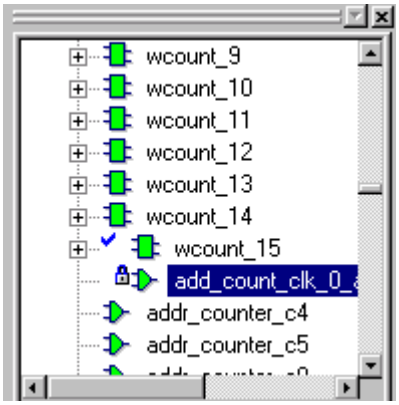
Tip: Right-click an object to use its context-sensitive menu.

In all Hierarchy views, you can right-click an object, and select **Properties** to display its properties.

Each view contains color-coded icons to indicate its logic type and state. These icons are explained in the following table:

Icon(s)	Color	What it Represents
	White	The logic or I/O is unassigned.
	Green	The logic or I/O is assigned.
	Hashed green	Some instances in the block of logic are assigned.
	Red and blue grid	The region is either inclusive or LocalClock.
	Blue grid	The region is exclusive.
	White	The region is empty.
	Cone icon	The object is a Logical Cone.
	Blue checkmark	The logic is assigned to a region.
	Gray checkmark	Some instances in the block of logic are assigned to a region.
	Blue lock	The entire block of assigned logic is locked to a location.
	Gray lock	Some instances in the block of assigned logic are locked to a location.

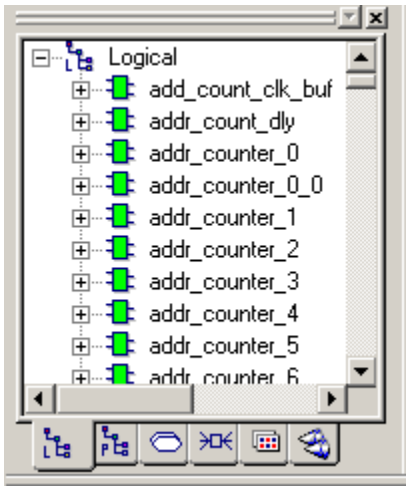
The Logical tab shown below illustrates that the selected logic is assigned to a region and locked. Only the Logical tab shows the logical design hierarchy. The Physical tab shows the physical hierarchy. The other tabs are not hierarchical.



Logical Tab - Checkmark and Lock Icons

Logical Tab

The Logical tab displays the logic in your design.



Hierarchy Window - Logical Tab

When you select a macro in this view, the macro and all of its instances are selected in all other views where it appears.

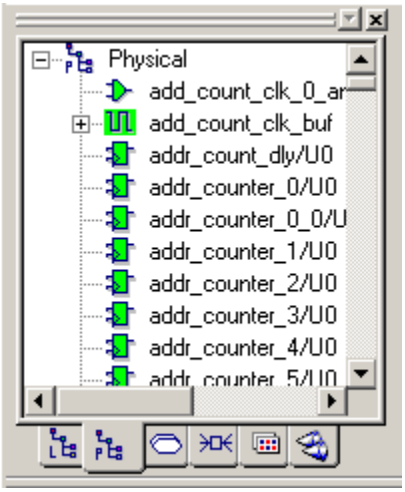
In this view, you can assign or unassign a macro to a region or location from the right-click menu or drag a macro from this view to the ChipPlanner or PinEditor window.

You can also lock an assigned macro or unlock a locked macro in this view.

Note: You can only lock macros that are currently assigned to a location.

Physical Tab

The Physical tab shows the hard macros and all of its instances in your design with their full hierarchical names. This tab provides you with more detail than the Logical tab.



Hierarchy Window - Physical Tab

When you select a macro in this tab, the macro and all of its instances are selected in all other views where it appears.

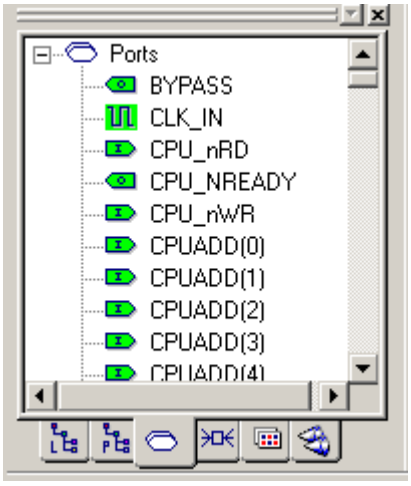
In this view, you can assign or unassign an instance to a region or location from the right-click menu or drag an instance from this view to the ChipPlanner or PinEditor window.

You can also lock an assigned instance or unlock a locked instance in this view.

Note: You can only lock macros or instances that are currently assigned to a location.

Ports Tab

The Ports tab shows all the input, output, and bidirectional ports in your design.



Hierarchy Window - Ports Tab

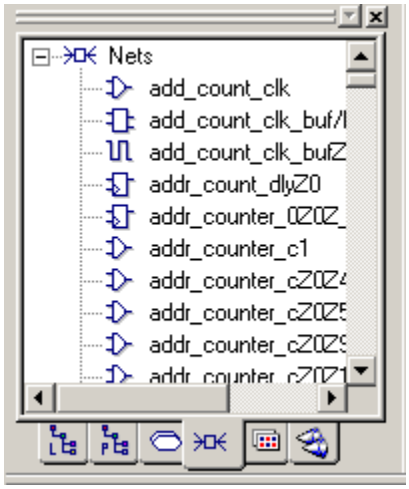
When you select a port in this view, the port is selected in all other views where it appears.

In this view, you can assign a port to an I/O region or location, lock an assigned port, and unlock a locked port.

Note: You can only lock ports that are currently assigned to a location.

Nets tab

The Nets tab displays the nets that connect two or more nodes in your design. The symbol to the left of the net indicates the type of driver. A checkmark appears next to a net that is assigned to a LocalClock region.



Hierarchy Window - Nets Tab

When you select a net in this view, the net is selected in all other views where it appears.

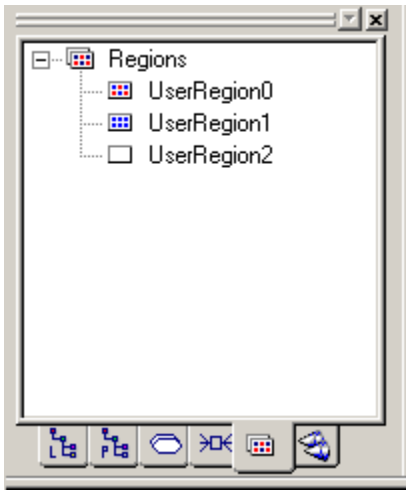
In this view, you can right-click a net and select **Properties** to display its properties (name, type, location, status, and PinList).

To display a net's properties:

1. Click the **Nets** tab in the **Hierarchy** window.
2. Select a net, right-click, and then choose **Properties** from the right-click menu.
3. In the **Net Properties** dialog box, click **Routing** to see routing details or **PinList** to see the names and locations of the pins.
4. Click **Close** to close the dialog box.

Regions Tab

The Regions tab shows regions you defined in your design. It also shows instances assigned to that region.



Hierarchy Window - Regions Tab

In this view, you can right-click a region and select **Properties** to display its properties (name, type, extents, and resource usage). You can also change a region's color in its Properties dialog box.

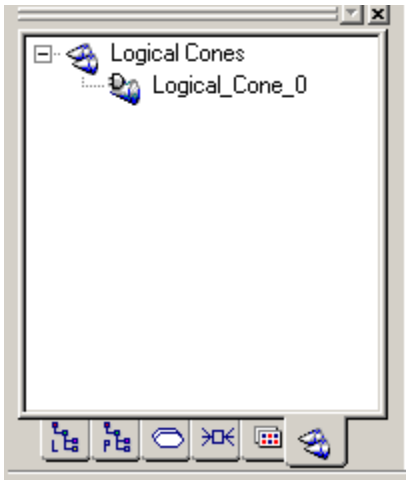
Additionally, from this view, you can assign an instance to a region, unassign instances from a region, and delete a region.

Note: To assign an instance to more than one region, those regions must be overlapping.

Logical Cones Tab

The Logical Cones tab displays a list of all Logical Cones that you created in your design

A Logical Cone is a netlist view you create to contain only the objects you want to see, such as part of the netlist. You can create Logical Cones to help you navigate and analyze a specific part of the design.



Hierarchy Window - Logical Cones Tab

Use this view to display only a specific portion of the netlist. Select the objects of interest from the netlist in NetlistViewer and add them to a specific cone view.

Note: The Logical Cones view supports cross-probing. All commands for creating a Logical Cone view are available from the LogicalCone menu in NetlistViewer and from the NetlistViewer right-click menu.

Menus, Toolbar Buttons, and Shortcut Keys

The File, Edit, View, Tools, Windows, and Help menus appear in all four tools available from the MultiView Navigator: ChipPlanner, PinEditor, NetlistViewer, and I/O Attribute Editor. Other menus are specific to the tool you are using.

File Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Commit		CTRL + S	Saves changes to the working design for this Designer session only **Note: To save changes to disk, you must also save your file in Designer.**
Print Preview			Displays the active design in a Preview window
Print		CTRL + P	Displays the Print dialog box from which you can print your active design
Exit			Closes the MultiView Navigator

Edit Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Undo		CTRL + Z	Reverses your last action
Redo		CTRL + Y	Reverses the action of your last Undo command
Cut		CTRL + X	Removes the selection from your design
Copy		CTRL + C	Copies the selection to the Clipboard
Paste		CTRL + V	Pastes the selection from the Clipboard
Select All		CTRL + A	Selects all logic in your design
Find		CTRL + F	Displays the Find dialog box, which you use to locate instances, nets, ports, and regions
Highlight		CTRL + B	Changes the pointer into the highlighter tool, which you can use to highlight objects. Clicking an object changes it to the selected highlight color
Unhighlight All		CTRL + SHIFT + B	Removes highlighting from all highlighted objects, changing them to their original colors
Highlight Color		CTRL + R	Displays the Color palette so you can select a highlight color

View Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Zoom In		CTRL + +	Magnifies the view by a factor of 2 (scale = 2x) **Note: If using the keyboard shortcut, use the + on the numeric keypad only**.
Zoom Out		CTRL + -	Reduces the view by a factor of 2 (scale = .5x) **Note: If using the keyboard shortcut, use the - on the numeric keypad only**.
Zoom Window		CTRL + W	Drag out an area to enlarge
Zoom Fit		CTRL + 0	Fits the entire design within the active Tools window
Redraw			Redraws the screen
Toolbars			Hides or displays groups of toolbar buttons
Windows			Hides or displays the Hierarchy window, Log window, Status Bar, or World window
Display Settings		CTRL + D	Displays the Display Settings dialog box, which provides a list of all the architectural features you can turn on and off in your tool
Properties			Displays the ChipPlanner Properties dialog box, which enables you to choose whether you want to bring a macro or net into view after you select it

Logic Menu

This menu is available only for the ChipPlanner, PinEditor, and I/O Attribute Editor tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Assign To Location		CTRL + K	Assigns the selected object to the selected location
Unassign From Location		CTRL + SHIFT + K	Removes the selected object from its current location
Lock		CTRL + L	Locks the selected instance
Unlock		CTRL + SHIFT + L	Unlocks the selected locked instance
Assign To Region		CTRL + N	Assigns the selected object to the selected region
Unassign From Region		CTRL + SHIFT + N	Removes the selected object from its current region
Properties			Displays the Logic Properties dialog box, in which you can change the properties of the selected logic

Nets Menu

This menu is available only for the ChipPlanner tool in the MultiView Navigator.

Command	Icon	Function
Show Input Only		Shows all input nets for the selected macro
Show Output Only		Shows all output nets for the selected macro
Show Input & Output		Shows all input and output nets for the selected macro
Hide All		Hides all input and output nets for the selected macro
Show Ratsnest		Displays net connectivity between assigned macros by connecting lines from the output pins to all input pins
Show Routes		Displays a representation of the routes
Properties		Displays the Net Properties dialog box

Region Menu

This menu is available only for the ChipPlanner tool in the MultiView Navigator.

Command	Icon	Shortcut	Function
Create Inclusive			Use to create an inclusive region in your design
Create LocalClock			Use to create a LocalClock region for the selected net
Create QuadrantClock			Use to create a Quadrant clock region for the selected clock net
Create Exclusive			Use to create an exclusive region in your design
Create Empty			Use to create an empty region in your design
Delete		Del key	Deletes the selected region from your design
Assign/Unassign Logic			Assign or unassign instances to the selected region
Properties			Displays the Region Properties dialog box, in which you can change the properties of the selected region

Package Menu

This menu is available only for the PinEditor tool in the MultiView Navigator.

Command	Shortcut	Function
View From Top		Displays a top-down view of the package
View From Bottom		Displays a bottom-up view of the package

Schematic Menu

This menu is available only for the NetlistViewer tool and Logical Cone windows in the MultiView Navigator.

Command	Icon	Function
Pop		Displays the next higher level in the design hierarchy
Push		Displays the next lower level in the design hierarchy
Top		Displays the top level of the design hierarchy
Go to First Page		Displays the first page of the current level of the design
Go to Previous Page		Displays the previous page of the current level of the design
Go to Next Page		Displays the next page of the current level of the design
Go to Last Page		Displays the last page of the current level of the design
Follow Net Into		Displays a dialog box in which you select the next page or instance of the net you want to see
Go to Net Driver		Jumps to the Net Driver
Allow Page Splitting		Enables or disables page splitting in your view
Show Pre-optimized Netlist		Displays the pre-optimized netlist. This is the default view
Show Optimized Netlist		Displays the optimized, flattened netlist.

LogicalCone Menu

This menu is available only for the NetlistViewer tool and Logical Cone windows in the MultiView Navigator.

Command	Shortcut	Function
Create New Cone		Opens a new Logical Cone window, which is set as the active cone
Rename Cone		Displays a dialog box, in which you can change the name of the active cone
Fold Selection		Hides all the logic inside the selected hierarchical instance in the cone view
Unfold Selection		Shows the logic that was added into the selected hierarchical instance in the cone view
Add to Active Cone		Displays a submenu of choices: **Add Selection** - adds selected objects to the active cone **Add Highlighted Group** - adds a group of highlighted objects to the active cone **Add Driver** - adds the instances which have a pin driving the selected net, input pin, or instance to the active cone **Add All Driven Logic** - adds all instances which have a pin driven by the selected net, output pin, or instance to the active cone **Add Adjacent** - displays a dialog box in which you select instances to add to the active cone
Remove From Active Cone		Displays a submenu of choices: **Clear** - removes all objects from the active cone **Remove Selection** - removes the selected object from the active cone **Remove Highlighted Group** - removes the selected group of objects from the active cone

Format Menu

This menu is available only for the I/O Attribute Editor tool in the MultiView Navigator.

Command	Shortcut	Function
Row > Hide		Hide the selected row(s)
Row > Unhide		Show all hidden rows between the selected rows
Column > Hide		Hide the selected column(s)
Column > Unhide		Show all hidden columns between the selected columns
Column > Freeze Pane		Freeze the selected columns(s)
Column > Unfreeze Pane		Unfreeze the selected columns(s)
Column > Autofit		Sets the width of columns within the table to accommodate all the text for any given row in those columns, including the column headings

Note: If no rows or columns are selected and you choose Unhide, all hidden rows or columns are displayed.

Tools Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Function
ChipPlanner		Displays the placement of I/O and logic macros in your chip in the Tools window
PinEditor		Displays the pin out in the Tools window
NetlistViewer		Displays the netlist in the Tools window
I/O Attribute Editor		Displays the attributes in your design in the Tools window
I/O Bank Settings		Displays the I/O Bank Settings dialog box, in which you can assign technologies to your I/O banks
DRC		Runs the Prelayout Checker to ensure that the design can be placed and routed

Window Menu

This menu is available for all tools in the MultiView Navigator.

Command	Function
New Window	Opens another window for the currently active tool **Note: Use these windows to view different parts of the design at the same time.**
Close Window	Closes the currently active tool window within the Tools window **Note: If the tool has more than one window open, this command closes all the windows for that tool.**
Cascade	Arranges windows so you can see the title bar of each window
Tile Horizontally	Arranges windows side-by-side in a horizontal pattern
Tile Vertically	Arranges windows side-by-side in a vertical pattern
Arrange Icons	Arranges minimized windows left-to-right across the bottom of the Tool window
<Tool name>	Makes the selected tool active

Help Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Function
<*Tool name*> Help		Displays the first Help topic for the active tool
MultiView Navigator Help		Displays the first Help topic for the MultiView Navigator, which provides an overview of the MVN interface
About the MultiView Navigator		Displays the current version number and copyright information for the MultiView Navigator

Contacting Actel

Actel Headquarters

Actel Corporation is a supplier of innovative programmable logic solutions, including field-programmable gate arrays (FPGAs) based on Antifuse and Flash technologies, high-performance intellectual property (IP) cores, software development tools, and design services targeted for the high-speed communications, application-specific integrated circuit (ASIC) replacement, and radiation-tolerant markets.

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Index

I

L

M

N

O

P

R

S

T

U

V

W

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