

Macro Library Guide

January 2003

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This guide includes macros for all Actel devices (including ProASIC).

Definitions

Macros

The Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. The relative placement of two module-macros is predefined. The timing characteristics are a function of the fanout on the output of the macro.

ACTgen Macro

ACTgen macros are described in Actel's publication, "A Guide to ACTgen Macros."

Combinability

For information on combinability, refer to the *Designer with Actel Manual*.

How to Use this Guide

Family Inclusion Indicator

In the titlebar of each macro is a list indicating whether the cell is a member of the ACT 1, ACT 2/1200XL, 3200DX, ACT 3, 40MX, 42MX, 54SX, 54SXA, or eX library.

Guidelines

1. All input pin loading is assumed to be a single load except macros that are built using two combinational modules or one sequential and one combinatorial module. These macros are assumed to have a load of two on some of their input pins.
2. All macros have output pin loading of zero except for the sequential macros that are built using two combinational modules only. These macros have an output pin loading of one.
3. All macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the Macro section of this manual.

Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

↑	denotes rising edge clock
↓	denotes falling edge clock
X	in an input column denotes a 'don't care' or logic simulation state 'unknown'
!Q	denotes Q not

Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

Restrictions

Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as "normal" data input/output buffers or they may be used as "special" pins. The following constraints apply to I/O pins used as "special" pins.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, 54SX, 54SXA, and eX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, 54SX, 54SXA, and eX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, 54SX, 54SXA and eX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3, 54SX, 54SXA and eX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may only be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

Advanced Application Notes

For Advanced Application notes, please refer to Actel's *Databook*.

HDL Instantiation of Macros

Refer to the *HDL Coding Style Guide* for information on instantiating macros.

Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be

shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE Interface Guides.

	Target Family					
Original Family	ACT 1/40MX	ACT 2/ 1200XL/ 3200DX/42MX	ACT 3	54SX	54SX-A	eX
ACT 1 or 40MX	X	YES	YES	NO	NO	NO
ACT 2, 1200XL, 3200DX, 42MX	NO	X	YES**	YES**	YES**	YES**
ACT 3	NO	NO	X	YES*	YES*	YES*
54SX	NO	NO	NO	X	YES	YES
54SX-A	NO	NO	NO	YES**	X	YES
eX	NO	NO	NO	YES	YES	X

* Except registered I/O, IOCLK, and IOPCL

** Except QCLK and RAM

List of Combinational Macros

AND2	29	A03B	48
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AND3A	31	A06	50
AND3B	31	A06A	50
AND3C	32	A07	51
AND4	32	A08	51
AND4A	33	A09	52
AND4B	33	A0I1	52
AND4C	34	A0I1A	53
AND4D	34	A0I1B	53
AND5A	35	A0I1C	54
AND5B	35	A0I1D	54
AND5C	36	AOI2A	55
A01	36	AOI2B	55
A010	37	AOI3A	56
A011	37	AOI4	56
A012	38	AOI4A	57
A013	38	AOI5	57
A014	39	AX1	58
A015	39	AX1A	58
A016	40	AX1B	59
A017	40	AX1C	59
A018	41	AX1D	60
A01A	41	AX1E	60
A01B	42	AXO1	61
A01C	42	AXO2	61
A01D	43	AXO3	62
A01E	43	AXO5	62
A02	44	AXO6	63
A02A	44	AXO7	63
A02B	45	AXOI1	64
A02C	45	AXOI2	64
A02D	46	AXOI3	65
A02E	46	AXOI4	65
A03	47	AXOI5	66
A03A	47	AXOI7	66

BUFA	67	DLM2A	147
BUFF	67	DLM2B	147
BUFD	68	DLM3	148
CLKINT	68	DLM3A	148
HCLKINT	69	DLM4	149
CLKINTI	70	DLM4A	149
CM7	71	DLM8A	150
CM8	72	DLM8B	151
CM8A	73	DLMA	152
CM8F	74	DLME1A	152
CM8INV	75	DLP1	153
CMA9	75	DLP1A	153
CMAF	76	DLP1B	154
CMB3	76	DLP1C	154
CMB7	77	DLP1D	155
CMBB	77	DLP1E	155
CMBF	78	DXAND7	156
CMEA	78	DXAX7	157
CMEB	79	DXNAND7	157
CMEE	79	FA1	158
CMEF	80	FA1A	158
CMF1	80	FA1B	159
CMF2	81	FA2A	159
CMF3	81	GAND2	160
CMF4	82	GMX4	160
CMF5	82	GNAND2	161
CMF6	83	GND	161
CMF7	83	GNOR2	162
CMF8	84	GOR2	162
CMF9	84	GXOR2	163
CMFA	85	HA1	163
CMFB	85	HA1A	164
CMFC	86	HA1B	164
CMFD	86	HA1C	165
CMFE	87	INV	165
CS1	87	INVD	166
CS2	88	INVA	166
CY2A	88	JKF	167
CY2B	89	JKF1B	168
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DLEC	144	JKF2B	169
DLM	145	JKF2C	169
DLM2	145	JKF2D	170

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JKF3B	171	NOR4C	194
JKF3C	171	NOR4D	195
JKF3D	172	NOR5B	195
JKF4B	173	NOR5C	196
JKFPC	173	NOR5D	196
MAJ3	174	OA1	197
MAJ3X	174	OA1A	198
MAJ3XI	175	OA1B	198
MIN3	175	OA1C	199
MIN3X	176	OA2	199
MIN3XI	177	OA2A	200
MX2	178	OA3	200
MX2A	178	OA3A	201
MX2B	179	OA3B	201
MX2C	179	OA4	202
MX4	180	OA4A	202
MXC1	180	OA5	203
MXT	181	OAI1	203
NAND2	181	OAI2A	204
NAND2A	182	OAI3	204
NAND2B	182	OAI3A	205
NAND3	183	OR2	207
NAND3A	183	OR2A	207
NAND3B	184	OR2B	208
NAND3C	184	OR3	208
NAND4	185	OR3A	209
NAND4A	185	OR3B	209
NAND4B	186	OR3C	210
NAND4C	186	OR4	210
NAND4D	187	OR4A	211
NAND5B	187	OR4B	211
NAND5C	188	OR4C	212
NAND5D	188	OR4D	212
NOR2	189	OR5A	213
NOR2A	189	OR5B	213
NOR2B	190	OR5C	214
NOR3	191	QCLKINT	214
NOR3A	191	QCLKINTI	215
NOR3B	192	TF1A	215
NOR3C	192	TF1B	216
NOR4	193	VCC	216
NOR4A	193	XA1	217

XA1A	217
XA1B	218
XA1C	218
XAI1	219
XAI1A	219
XNOR2	220
XNOR3	220
XO1	221
XO1A	221
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XOR3	222
XOR4	223
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DF1B	90	DFM3	109
DF1C	91	DFM3B	110
DFC1	91	DFM3E	110
DFC1A	92	DFM3F	111
DFC1B	92	DFM3G	111
DFC1C	93	DFM4	112
DFC1D	93	DFM4A	112
DFC1E	94	DFM4B	113
DFC1F	94	DFM4C	113
DFC1G	95	DFM4D	114
DFE	95	DFM4E	114
DFE1B	96	DFM5A	115
DFE1C	96	DFM5B	115
DFE2D	97	DFM6A	116
DFE3A	97	DFM6B	116
DFE3B	98	DFM7A	117
DFE3C	98	DFM7B	118
DFE3D	99	DFM8A	119
DFE4	99	DFM8B	120
DFE4A	100	DFMA	121
DFE4B	100	DFMB	121
DFE4C	101	DFME1A	122
DFE4F	101	DFME1B	122
DFE4G	102	DFME2A	123
DFEA	102	DFME2B	123
DFEB	103	DFME3A	124
DFEC	103	DFME3B	124
DFED	104	DFMPCA	125
DFEG	104	DFMPCB	125
DFEH	105	DFP1	126
IODFE	105	DFP1A	126
IODFEC	106	DFP1B	127
IODFEP	106	DFP1C	127
DFM	107	DFP1D	128
DFMEG	107	DFP1E	128
DFMEH	108	DFP1F	129

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DFPC	130
DFPCA	130
DFPCB	131
DFPCC	131
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DL1A	132
DL1B	133
DL1C	133
DL2A	134
DL2B	134
DL2C	135
DL2D	136
DLC	136
DLC1	137
DLC1A	137
DLC1F	138
DLC1G	138
DLCA	139
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A01A	41	AND4	32
A01B	42	AND4A	33
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A01E	43	AND4D	34
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A03B	48	AOI5	57
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A0I1C	54	AXO3	62
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AXOI4	65	CMEE	79
AXOI5	66	CMEF	80
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BBHS	263	CMF3	81
BBHSA	270	CMF4	82
BBLSA	270	CMF5	82
BBUFTH	271	CMF6	83
BBUFTL	271	CMF7	83
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CM8	72	DF1B_CC	229
CM8A	73	DF1C	91
CM8F	74	DF1C_CC	229
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DLC1G	138	FCINIT_VCC	312
DLCA	139	FECTH	278
DLE	139	FECTL	278
DLE1D	140	FECTMH	280
DLE2A	140	FECTML	280
DLE2B	141	FEPTH	279
DLE2C	141	FEPTL	279
DLE3A	142	FEPTMH	281
DLE3B	142	FEPTML	281
DLE3C	143	FIFO64K36	253
DLEA	143	GAND2	160
DLEB	144	GMX4	160
DLEC	144	GNAND2	161
DLM	145	GND	161
DLM2	145	GNOR2	162
DLM2A	147	GOR2	162
DLM2B	147	GXOR2	163
DLM3	148	HA1	163
DLM3A	148	HA1A	164
DLM4	149	HA1B	164
DLM4A	149	HA1C	165
DLM8A	150	HCLKBUF	258
DLM8B	151	HCLKBUF_LVDS; HCLKBUF_LVPECL	297
DLMA	152	HCLKBUF_X	292
DLME1A	152	HCLKINT	69
DLP1	153	IBDL	264
DLP1A	153	IBUF	282
DLP1B	154	INBUF	259
DLP1C	154	INBUF_LVDS; INBUF_LVPECL	296
DLP1D	155	INBUF_X	288

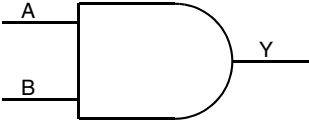
INV	165	NAND3	183
INVA	166	NAND3A	183
INVD	166	NAND3B	184
IOCLKBUF	282	NAND3C	184
IODFE	105	NAND4	185
IODFEC	106	NAND4A	185
IODFEP	106	NAND4B	186
IOFIFO (PerPin FIFO)	298	NAND4C	186
IOFIFOCTL	298	NAND4D	187
IOPCLBUF	283	NAND5B	187
IR	264	NAND5C	188
IREC	283	NAND5D	188
IREP	284	NOR2	189
IRI	265	NOR2A	189
JKF	167	NOR2B	190
JKF1B	168	NOR3	191
JKF2A	168	NOR3A	191
JKF2B	169	NOR3B	192
JKF2C	169	NOR3C	192
JKF2D	170	NOR4	193
JKF3A	170	NOR4A	193
JKF3B	171	NOR4B	194
JKF3C	171	NOR4C	194
JKF3D	172	NOR4D	195
JKF4B	173	NOR5B	195
JKFPC	173	NOR5C	196
MAJ3	174	NOR5D	196
MAJ3X	174	OA1	197
MAJ3XI	175	OA1A	198
MIN3	175	OA1B	198
MIN3X	176	OA1C	199
MIN3XI	177	OA2	199
MULT1	304	OA2A	200
MX2	178	OA3	200
MX2A	178	OA3A	201
MX2B	179	OA3B	201
MX2C	179	OA4	202
MX4	180	OA4A	202
MXC1	180	OA5	203
MXT	181	OAI1	203
NAND2	181	OAI2A	204
NAND2A	182	OAI3	204
NAND2B	182	OAI3A	205

OBDLHS	265	RAM4FR	242
OBHS	266	RAM4RA	243
OBUFTH	284	RAM4RF	244
OBFTL	285	RAM4RR	245
OR2	207	RAM64K36 /RAM64K36P	252
OR2A	207	RAM8FA	246
OR2B	208	RAM8FF	247
OR3	208	RAM8FR	248
OR3A	209	RAM8RA	249
OR3B	209	RAM8RF	250
OR3C	210	RAM8RR	251
OR4	210	SFCNTECP1	307
OR4A	211	SFCNTELDCP1	309
OR4B	211	SRCNTECP1	307
OR4C	212	SRCNTELDCP1	309
OR4D	212	SUB1	302
OR5A	213	TBDLHS	269
OR5B	213	TBHS	269
OR5C	214	TF1A	215
ORECTH	285	TF1B	216
ORECTL	286	TRIBUFF	262
OREPTH	286	TRIBUFF_X	295
OREPTL	287	VCC	216
ORH	266	XA1	217
ORIH	267	XA1A	217
ORITH	267	XA1B	218
ORTH	268	XA1C	218
OUTBUF	259	XAI1	219
OUTBUF_LVDS; OUTBUF_LVPECL ..	297	XAI1A	219
OUTBUF_X	293	XNOR2	220
PLL; PLLFB	314	XNOR3	220
PLLCLK	316	XNOR4	224
PLLINT	315	XO1	221
PLLOUT	315	XO1A	221
PLLCLK	316	XOR2	222
QCLKBIBUF	260	XOR3	222
QCLKBIBUFI	260	XOR4	223
QCLKBUF	261	ZOR3	225
QCLKBUFI	261	ZOR3I	225
QCLKINT	214		
QCLKINTI	215		
RAM4FA	240		
RAM4FF	241		

Combinational/Sequential Macros

AND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input AND

Truth Table

A	B	Y
X	0	0
0	X	0
1	1	1

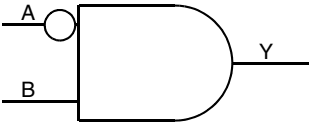
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

AND2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input AND with active low A Input

Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

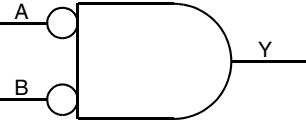
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

AND2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input AND with active low Inputs

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

Input

A, B

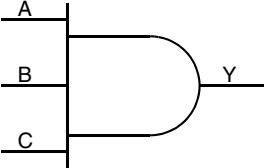
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input AND

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input

A, B,C

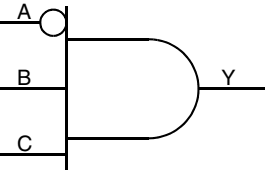
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

Input

A, B, C

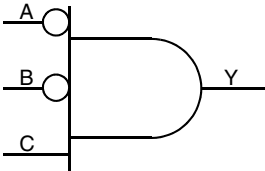
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input AND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

Input

A, B,C

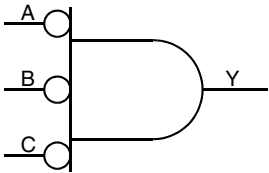
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input AND with active low Inputs

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input

A, B, C

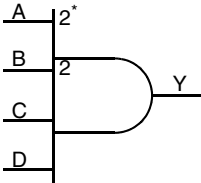
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Input

A, B, C, D

Output

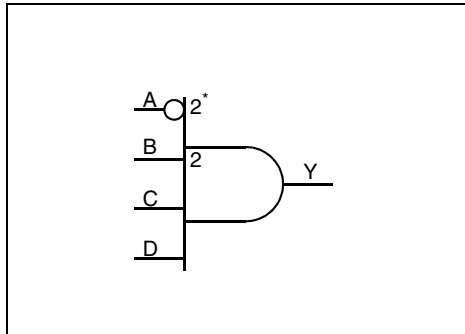
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and 40MX.

AND4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input AND with active low A-Input

Truth Table

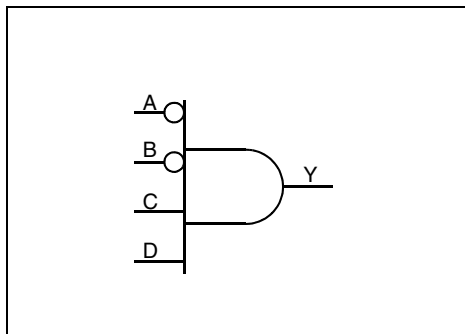
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

Family	Modules	
	Seq	Comb
40MX/ACT1		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and 40MX.

AND4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input AND with active low A- and B-Inputs

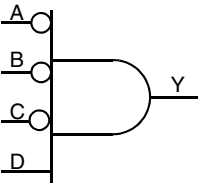
Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

AND4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND with active low A-, B-, and C-Inputs

Truth Table

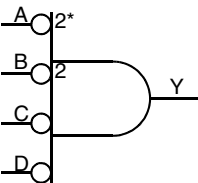
A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AND4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND with active low Inputs

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

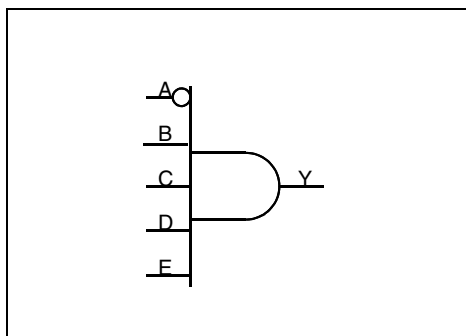
Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX, 54SX-A, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays, except 54SX, 54SX-A, and eX.

AND5A

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input AND with active low A input

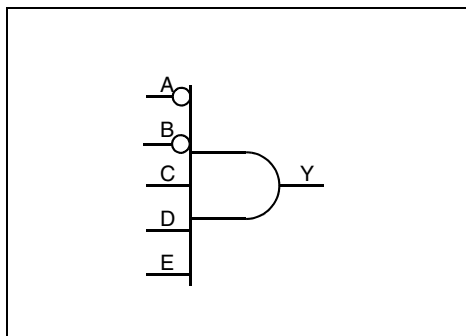
Truth Table

A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Family	Modules	
	Seq	Comb
All listed		1

AND5B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input AND with active low A-, and B-Inputs

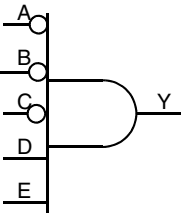
Truth Table

A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

AND5C

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function
5-Input AND with active low A-, B- and C-Inputs

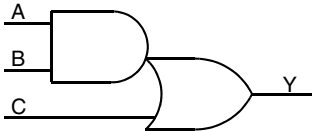
Truth Table

A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, eX, Axcelerator		1

A01

ACT1, ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function
3-Input AND-OR

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Family	Modules	
	Seq	Comb
All		1

A010

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AB[AND]; B --- AB; C --- CD[OR]; D --- CD; AB --- ABCD[AND]; CD --- ABCD; E --- ABCDE[AND]; ABCDE --- Y
```

Function
5-Input AND-OR-AND

Truth Table

A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

Input A, B, C, D, E	Output Y
-------------------------------	--------------------

Family	Modules	
	Seq	Comb
All except ACT1 and 40MX		1

A011

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AB[AND]; B --- AB; AB --- ABC[OR]; C --- ABC; ABC --- Y
```

Function
3-Input AND-OR

Truth Table

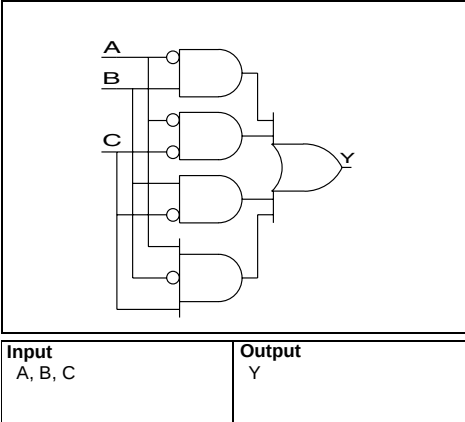
A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All except ACT1 and 40MX		1

A012

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-OR

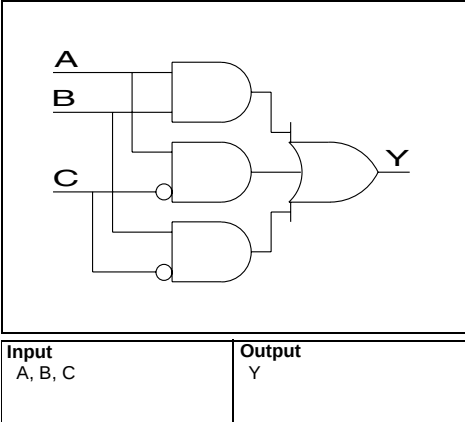
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

A013

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-OR

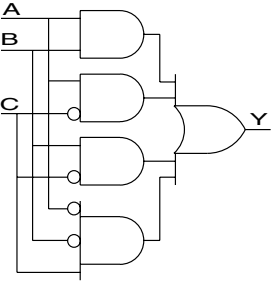
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

A014

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function
3-Input AND-OR

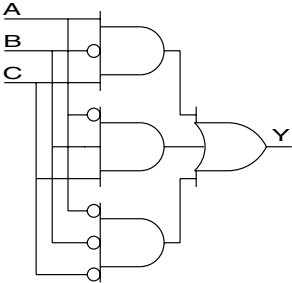
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

A015

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

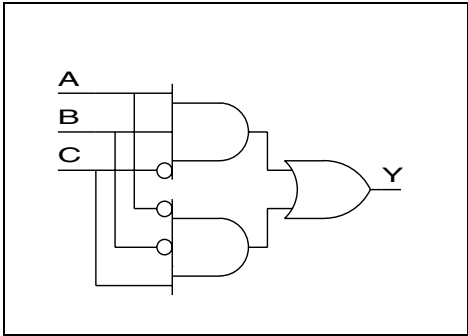
Function
3-Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

A01654SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

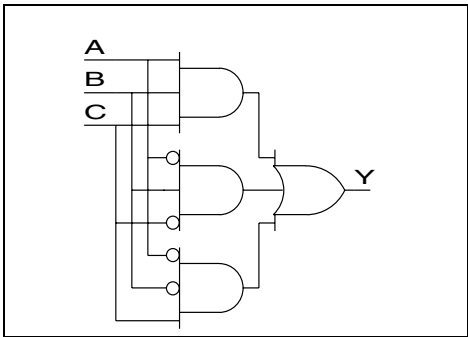
Function
3-Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

A01754SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function
3-Input AND-OR

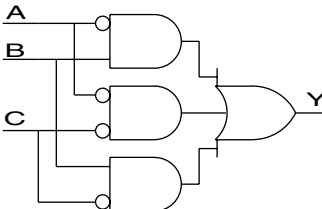
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

A018

54SX, 54SX-A, 54SX-S, eX, Axcelerator



```
graph LR; A --- AND1; B --- AND1; C --- AND1; A --- AND2; B --- AND2; C --- AND2; A --- AND3; B --- AND3; C --- AND3; AND1 --- OR; AND2 --- OR; AND3 --- OR; OR --- Y
```

Function

3-Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Input

A, B, C

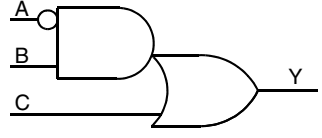
Output

Y

Family	Modules	
	Seq	Comb
All listed		1

A01A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



```
graph LR; A --- NOT1[Inverter]; NOT1 --- AND1; B --- AND1; AND1 --- OR; C --- OR; OR --- Y
```

Function

3-Input AND-OR with active low A-Input

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

Input

A, B, C

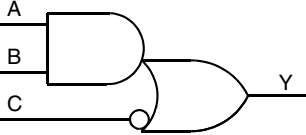
Output

Y

Family	Modules	
	Seq	Comb
All listed		1

A01B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Logic diagram for A01B: A 3-input AND-OR gate. Inputs A and B are connected to an AND gate. Input C is connected to an OR gate. The output of the AND gate and input C are connected to the OR gate. The output of the OR gate is Y.

Function
3-Input AND-OR with active low C-Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

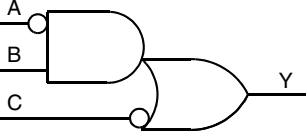
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

A01C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Logic diagram for A01C: A 3-input AND-OR gate. Input A is connected to an AND gate with an active low bubble. Input B is connected to the AND gate. Input C is connected to an OR gate with an active low bubble. The output of the AND gate and input C are connected to the OR gate. The output of the OR gate is Y.

Function
3-Input AND-OR with active low A- and C-Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

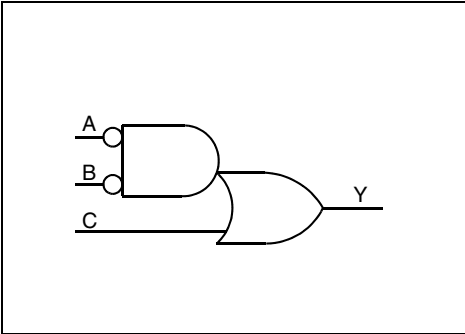
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

A01D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

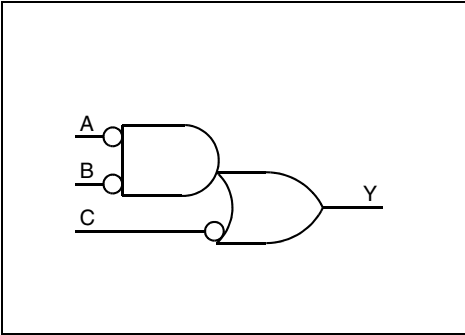
Function
3-Input AND-OR with active low A- and B-Inputs

Truth Table			
A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Family	Modules	
	Seq	Comb
All listed above		1

A01E

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

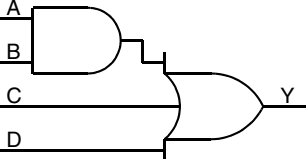
Function
3-Input AND-OR with active low Inputs

Truth Table			
A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Family	Modules	
	Seq	Comb
All listed above		1

A02

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

Input

A, B, C, D

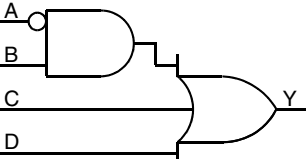
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A02A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A-Input

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

Input

A, B, C, D

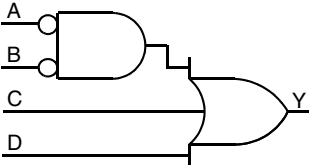
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A02B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR with active low A and B-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

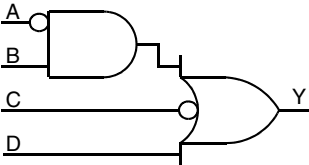
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A02C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

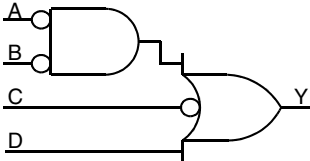
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A02D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

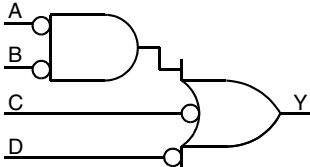
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A02E

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A03

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; C --- AND1; D --- OR1[OR]; AND1 --- OR1; OR1 --- Y
```

Function
4-Input AND-OR with active low A Input

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
ALL		1

A03A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; C --- AND1; D --- OR1[OR]; AND1 --- OR1; OR1 --- Y
```

Function
4-Input AND-OR

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

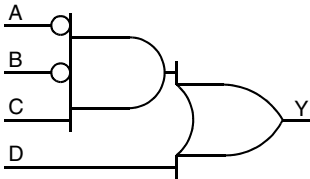
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A03B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4 Input AND-OR with active low A-, B- Inputs

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

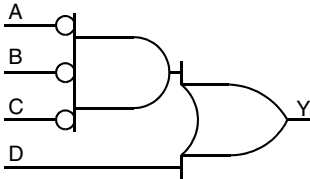
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A03C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR with active low A-, B-, C- Inputs

Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

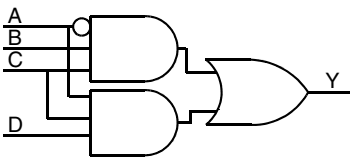
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed above		1

A04A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

Input

A, B, C, D

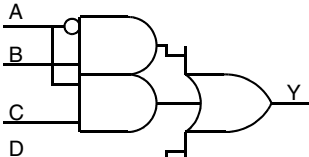
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A05A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

Input

A, B, C, D

Output

Y

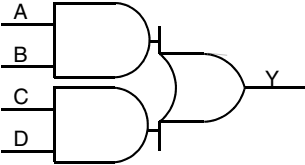
Family	Modules	
	Seq	Comb
ALL		1

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A06

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-wide 4-Inputs AND-OR

Truth Table

A	B	C	D	Y
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

Input

A, B, C, D

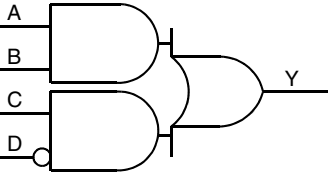
Output

Y

Family	Modules	
	Seq	Comb
All listed above		1

A06A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-wide 4-Inputs AND-OR with active low D-Input

Truth Table

A	B	C	D	Y
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

Input

A, B, C, D

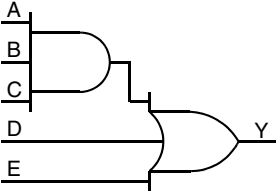
Output

Y

Family	Modules	
	Seq	Comb
All listed above		1

A07

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input AND-OR

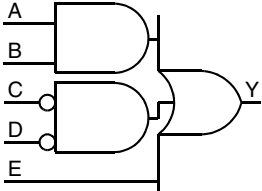
Truth Table

A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

A08

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input AND-OR with active low C- and D-Inputs

Truth Table

A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

A09

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1; B --- AND1; C --- AND2; D --- AND3; E --- AND4; AND1 --- OR1; AND2 --- OR1; AND3 --- OR1; AND4 --- OR1; OR1 --- Y
```

Function
5-Input AND-OR

Truth Table

A	B	C	D	E	Y
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

Input A, B, C, D, E	Output Y
-------------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

A011

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1; B --- AND1; C --- AND2; AND1 --- OR1; AND2 --- OR1; OR1 --- NOT1; NOT1 --- Y
```

Function
3-Input AND-OR-INVERT

Truth Table

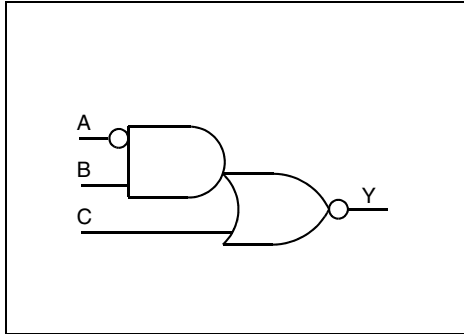
A	B	C	Y
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others		1

A0I1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input AND-OR-INVERT with active low A-Input

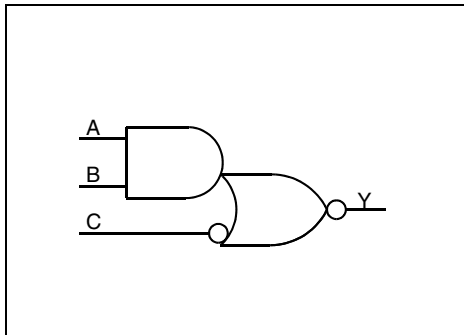
Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

Family	Modules	
	Seq	Comb
ALL		1

A0I1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input AND-OR-INVERT with active low C-Input

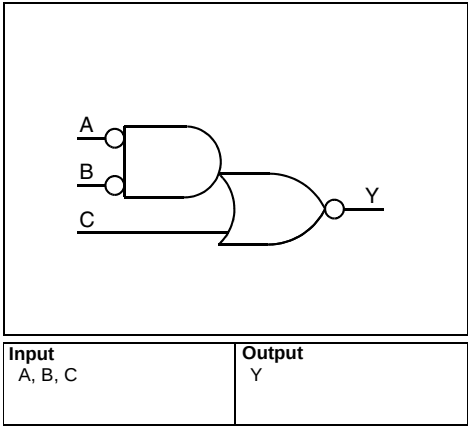
Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

Family	Modules	
	Seq	Comb
ALL		1

A011C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3 Input AND-OR-INVERT with active low A- and B-Inputs

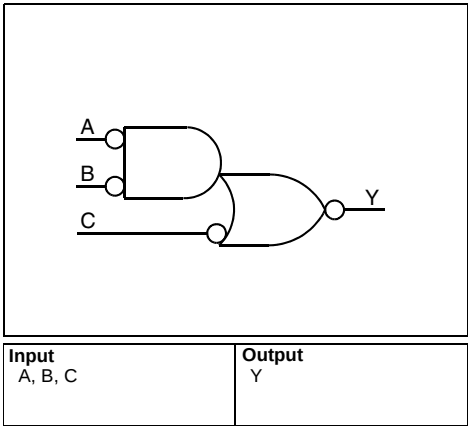
Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Family	Modules	
	Seq	Comb
All listed above		1

A011D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-OR-INVERT with active low Inputs

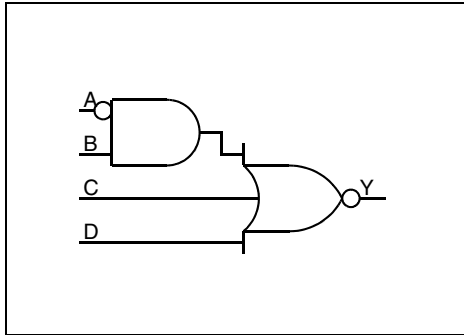
Truth Table

A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Family	Modules	
	Seq	Comb
All listed		1

AOI2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input AND-OR-INVERT with active low A-Input

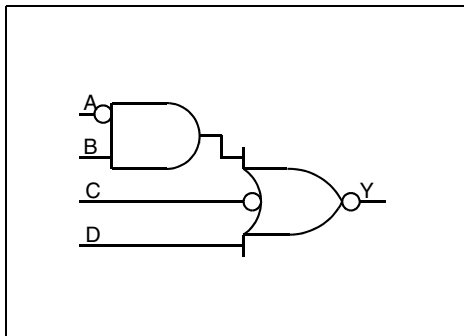
Truth Table

A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

Family	Modules	
	Seq	Comb
ALL		1

AOI2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input AND-OR-INVERT with active low A- and C-Inputs

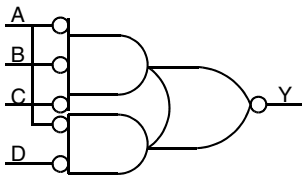
Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

Family	Modules	
	Seq	Comb
ALL		1

AOI3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input AND-OR-INVERT with active low Inputs

Truth Table

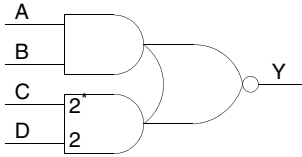
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

AOI4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
2-wide 4-Inputs AND-OR-INVERT

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

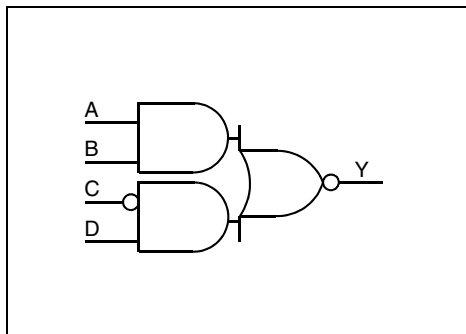
Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except 54SX, 54SX-A, 54SX-S, and eX.

AOI4A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Input**

A, B, C, D

Output

Y

Function

2-wide 4-Inputs AND-OR-INVERT with active low C-Input

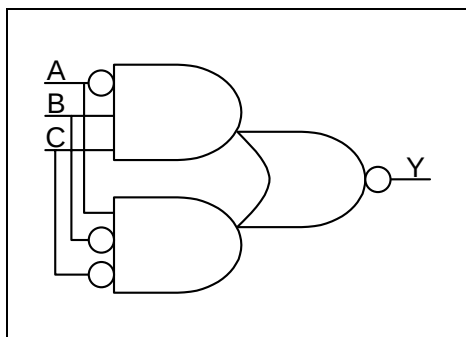
Truth Table

A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

Family	Modules	
	Seq	Comb
All listed		1

AOI5

54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Input**

A, B, C

Output

Y

Function

3-Input AND-OR-INVERT

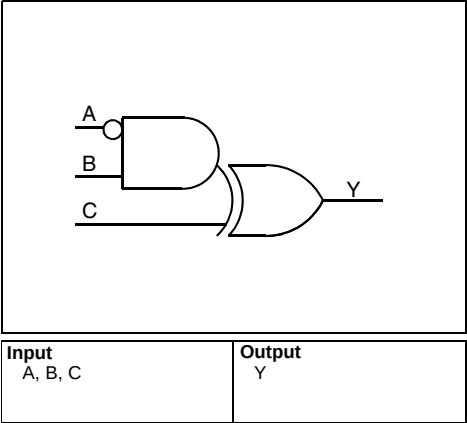
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AX1

ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-XOR with active low A-Input

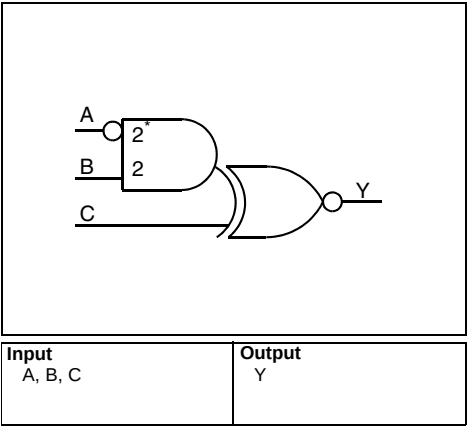
Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Family	Modules	
	Seq	Comb
All listed		1

AX1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-XOR-INVERT with active low A-Input

Truth Table

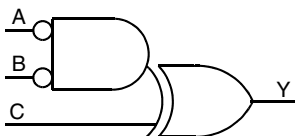
A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

Family	Modules	
	Seq	Comb
ACT 1,40MX,54SX, 54SX-A, 54SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, 40MX, 54SX, 54SX-A, 54SX-S and eX.

AX1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input AND-XOR with active low A- and B-Inputs

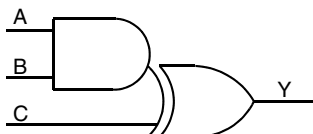
Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

Family	Modules	
	Seq	Comb
All		1

AX1C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input AND-XOR

Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AX1D

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-XNOR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

AX1E

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input AND-XNOR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

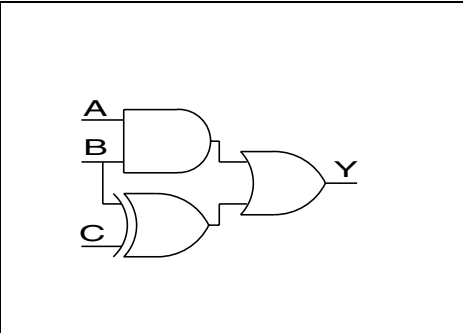
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

AXO1

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

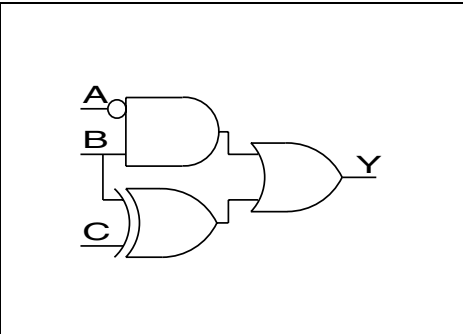
Function
3-Input Combinatorial Gate

Truth Table			
A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

AXO2

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function
3-Input Combinatorial Gate

Truth Table			
A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AXO3

54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; AND1 --- NOT1[NOT]; NOT1 --- OR1[OR]; C --- OR1; OR1 --- Y
```

Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

AXO5

54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; AND1 --- NOT1[NOT]; NOT1 --- OR1[OR]; C --- OR1; OR1 --- Y
```

Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

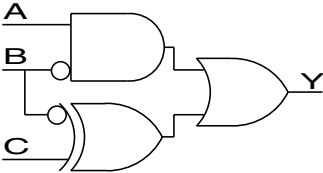
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

AXO6

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function
3-Input Combinatorial Gate

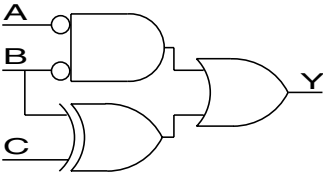
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

AXO7

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function
3-Input Combinatorial Gate

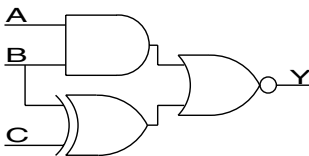
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AXOI1

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input Combinatorial Gate

Truth Table

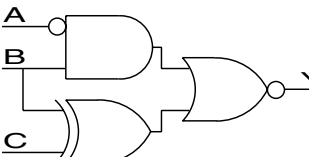
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

AXOI2

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

AXOI3

54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; AND1 --- AND2[AND]; C --- AND2; AND2 --- INV[Inverter]; INV --- Y
```

Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

AXOI4

54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A --- AND1[AND]; B --- AND1; AND1 --- AND2[AND]; C --- AND2; AND2 --- INV[Inverter]; INV --- Y
```

Function
3-Input Combinatorial Gate

Truth Table

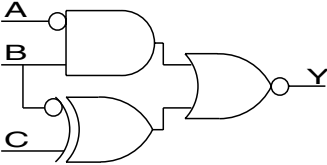
A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

AXOI5

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

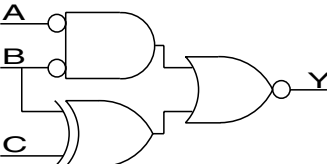
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI7

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

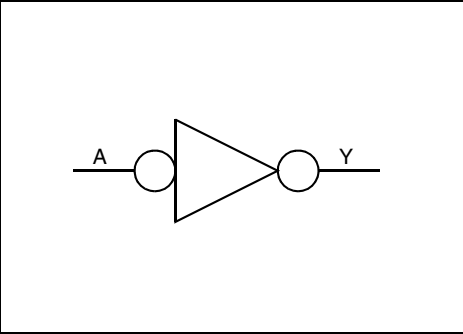
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

BUFA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Buffer, with active low Input and Output

Truth Table

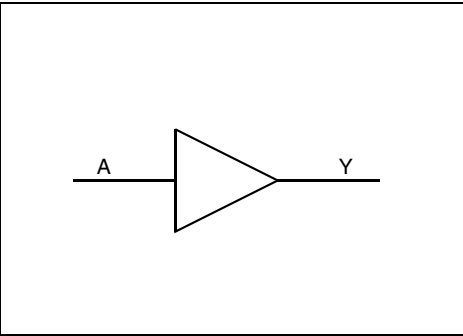
A	Y
0	0
1	1

Input A	Output Y
-------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

BUFF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Buffer

Truth Table

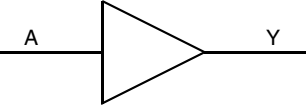
A	Y
0	0
1	1

Input A	Output Y
-------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

BUFD

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Buffer
NOTE: The Combiner will not remove this macro

Truth Table

A	Y
0	0
1	1

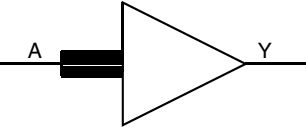
Input
A

Output
Y

Family	Modules	
	Seq	Comb
All		1

CLKINT

ACT 2/1200XL, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Internal Clock Interface

Truth Table

A	Y
0	0
1	1

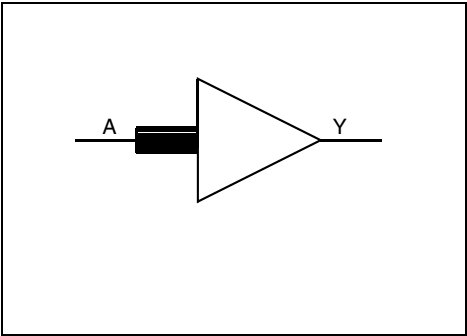
Input
A

Output
Y

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to the latest Actel datasheet.

HCLKINT

ACT 2/1200XL, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Internal Clock Interface

Truth Table

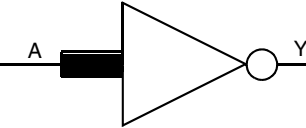
A	Y
0	0
1	1

Input A	Output Y
-------------------	--------------------

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to the latest Actel datasheet.

CLKINTI

54SX, 54SX-A, 54SX-S, eX



Function
Inverting Internal Clock Interface

Truth Table

A	Y
0	1
1	0

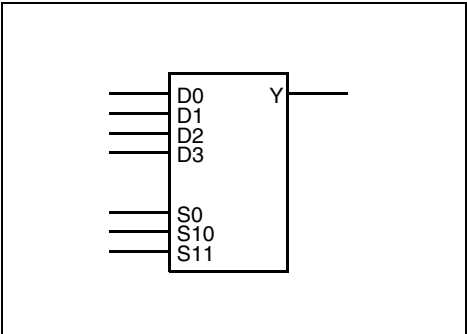
Input
A

Output
Y

NOTE: CLKINTI does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

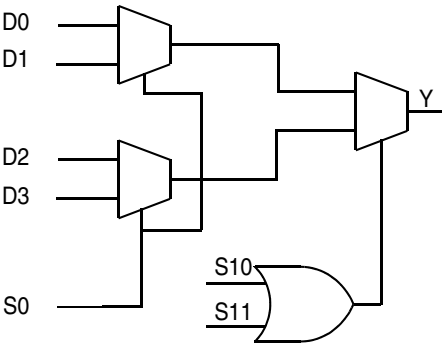
CM7

ACT2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input D0, D1, D2, D3, S0, S10, S11	Output y
--	--------------------

Function
Full Combinational Module



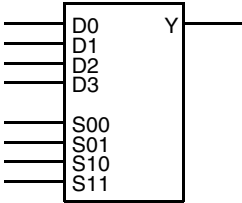
Truth Table

S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

Family	Modules	
	Seq	Comb
All listed		1

CM8

ACT2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



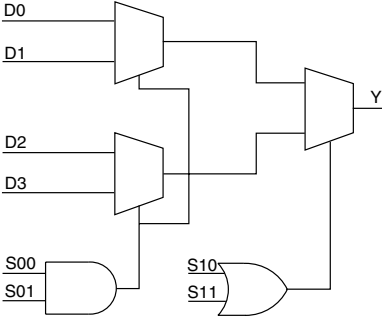
Pin diagram of the CM8 module. Inputs on the left: D0, D1, D2, D3, S00, S01, S10, S11. Output on the right: Y.

Function

Full Combinational Module

Input
D0, D1, D2, D3, S00, S01, S10, S11

Output
y



Logic diagram of the CM8 module. It consists of two 2-to-1 multiplexers (triangles) and two 2-input AND gates (D-shaped symbols). The first multiplexer has inputs D0 and D1, and its output is connected to the top input of the second multiplexer. The second multiplexer has inputs D2 and D3, and its output is connected to the bottom input of the first multiplexer. The output of the first multiplexer is also connected to the top input of the first AND gate. The output of the second multiplexer is also connected to the top input of the second AND gate. The first AND gate has inputs S00 and S01. The second AND gate has inputs S10 and S11. The outputs of both AND gates are connected to the output Y.

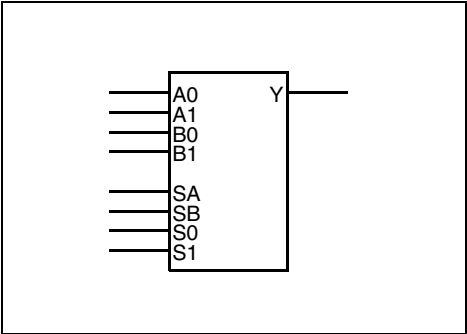
Truth Table

S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All listed		1

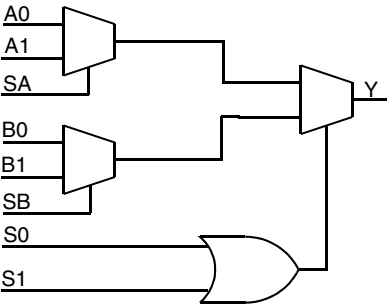
CM8A

ACT 1, 40MX



Input	Output
A0, A1, B0, B1, SA, SB, S0, S1	Y

Function
Full Combinational Module



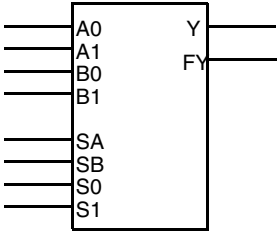
Truth Table

S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

Family	Modules	
	Seq	Comb
ACT 1, 40MX		1

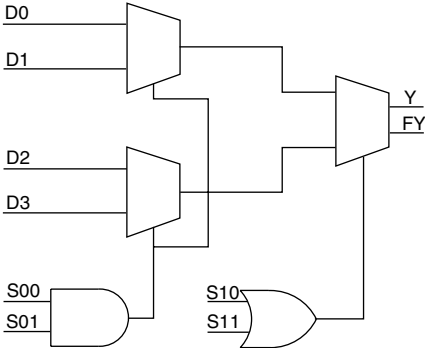
CM8F

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Full Combinational Module with fast output

Input D0, D1, D2, D3, S00, S01, S10, S11	Output Y, FY
---	------------------------



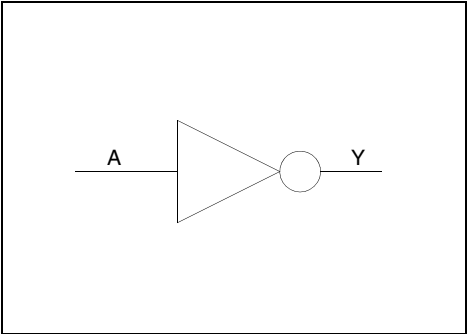
Truth Table					
S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
All listed		1

NOTE: FY is a fast output that has a maximum fanout of 1.

CM8INV

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Inverter with active low output

Truth Table

A	Y
0	1
1	0

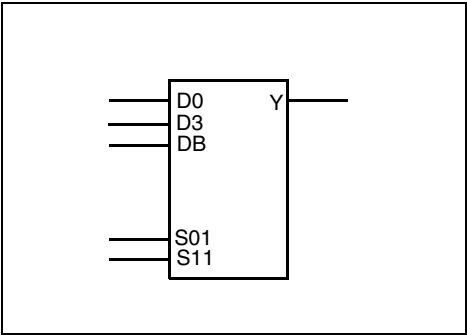
Input	Output
A	Y

Family	Modules	
	Seq	Comb
All listed		0

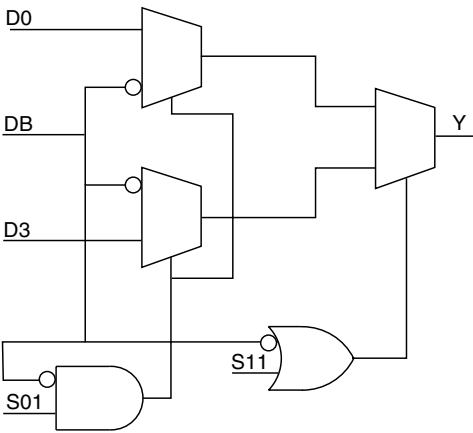
NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module.

CMA9

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Full Combinational Module



Input	Output
D0, D3, DB, S01, S11	Y

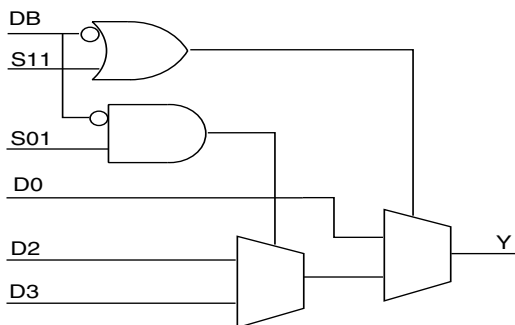
Family	Modules	
	Seq	Comb
All listed		1

54SX, 54SX-A, 54SX-S, eX, Axcelerator

Input D0, D2, D3, DB, S01, S11	Output Y
--	--------------------

Family	Modules	
	Seq	Comb
All listed		1

Full Combinational Module

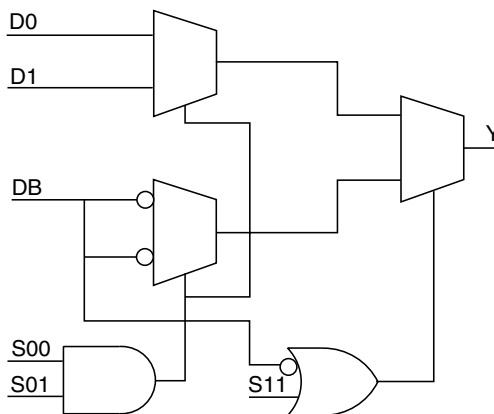


54SX, 54SX-A, 54SX-S, eX, Accelerator

Input	Output
D0, D1, DB, S00, S01, S11	Y

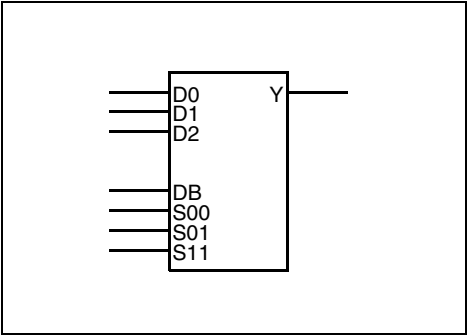
Family	Modules	
	Seq	Comb
All listed		1

Full Combinational Module



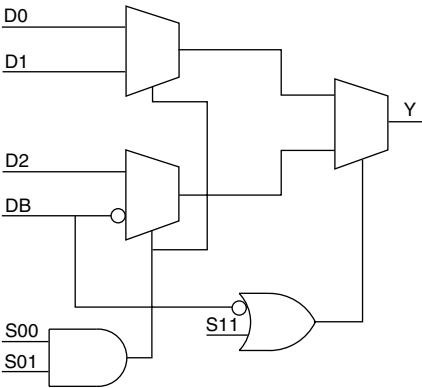
CMB7

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
D0, D1, D2, DB, S00, S01, S11	Y

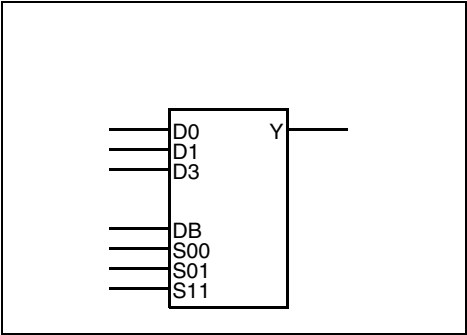
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

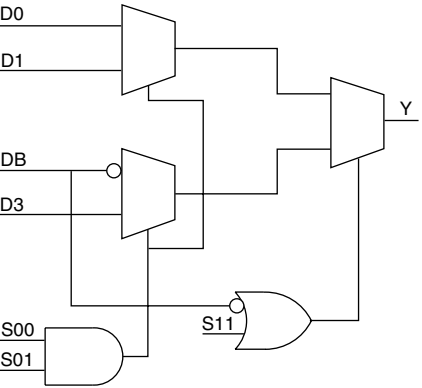
CMBB

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
D0, D1, D3, DB, S00, S01, S11	Y

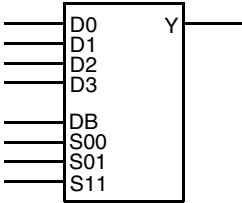
Function
Full Combinational Module



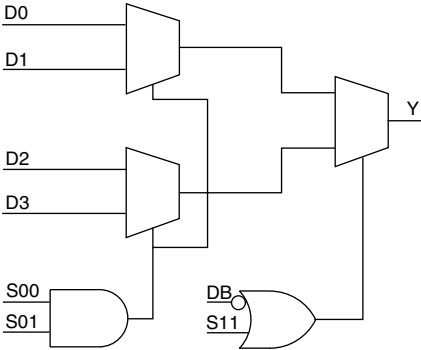
Family	Modules	
	Seq	Comb
All listed		1

CMBF

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Full Combinational Module

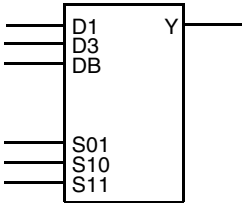


Input D0, D1, D2, D3, DB, S00, S01, S11	Output Y
---	--------------------

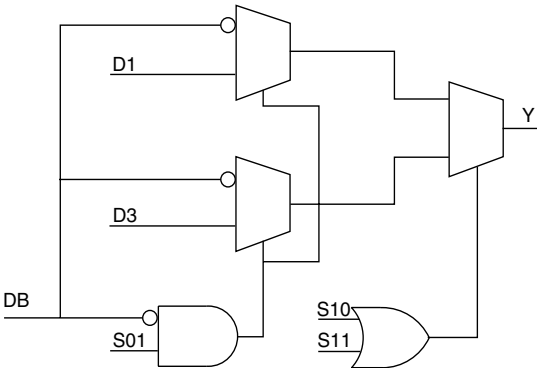
Family	Modules	
	Seq	Comb
All listed		1

CMEA

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Full Combinational Module

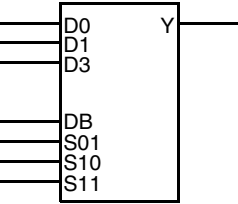


Input D1, D3, DB, S01, S10, S11	Output Y
---	--------------------

Family	Modules	
	Seq	Comb
All listed		1

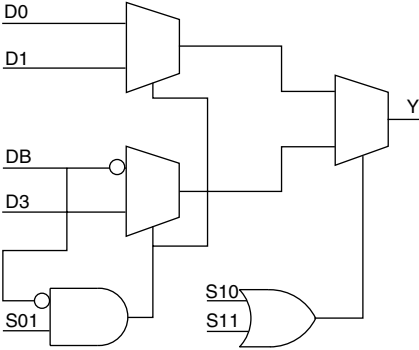
CMEB

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Full Combinational Module

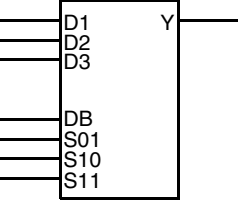


Input	Output
D0, D1, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

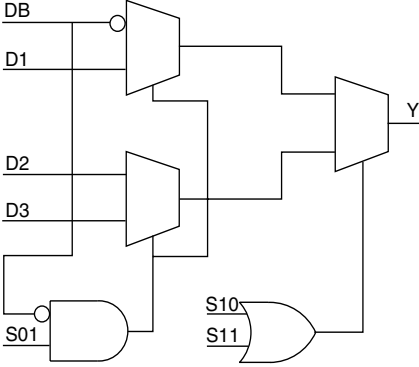
CMEE

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Full Combinational Module



Input	Output
D1, D2, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

CMEF

54SX, 54SX-A, 54SX-S, eX, Axcelerator

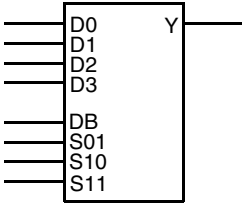
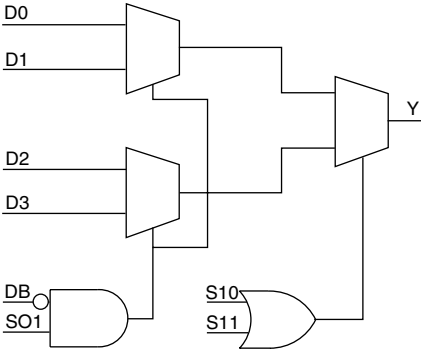


Diagram of the CMEF module symbol. It has inputs D0, D1, D2, D3, DB, S01, S10, and S11. It has one output Y.

Function
Full Combinational Module



Logic diagram for the CMEF module. Inputs D0 and D1 are connected to a 2-input AND gate. Inputs D2 and D3 are connected to another 2-input AND gate. The outputs of these two AND gates are connected to a 2-input OR gate. Input DB is connected to a 2-input AND gate along with input S01. The output of this AND gate is connected to a 2-input OR gate along with input S10. Input S11 is also connected to this OR gate. The output of the OR gate is connected to the output Y.

Input	Output	
	D0, D1, D2, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

CMF1

54SX, 54SX-A, 54SX-S, eX, Axcelerator

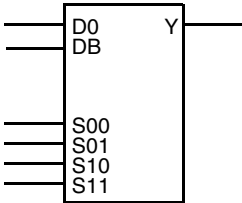
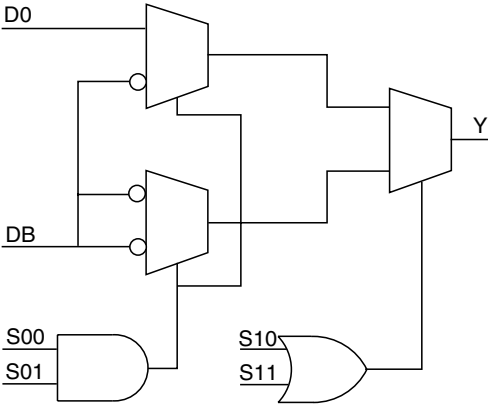


Diagram of the CMF1 module symbol. It has inputs D0, DB, S00, S01, S10, and S11. It has one output Y.

Function
Full Combinational Module



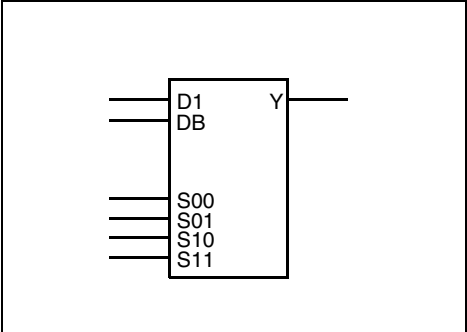
Logic diagram for the CMF1 module. Input D0 is connected to a 2-input AND gate. Input DB is connected to a 2-input AND gate along with input S00. The output of this AND gate is connected to a 2-input OR gate along with input S01. Input S10 is also connected to this OR gate. Input S11 is connected to a 2-input AND gate. The output of this AND gate is connected to a 2-input OR gate along with input S10. The output of the OR gate is connected to the output Y.

Input	Output	
	D0, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

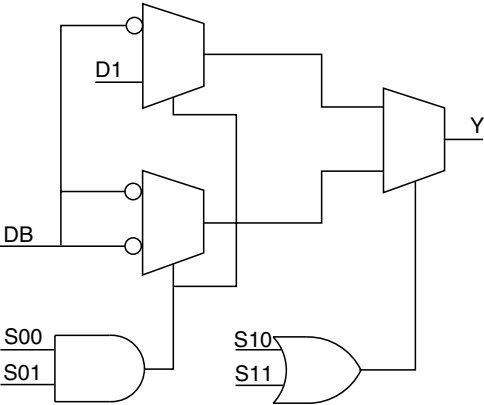
CMF2

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input D1, DB, S00, S01, S10, S11	Output Y
--	--------------------

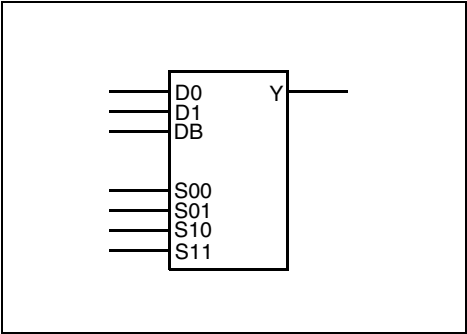
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

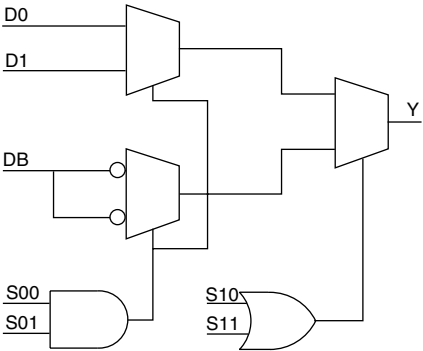
CMF3

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input D0, D1, DB, S00, S01, S10, S11	Output Y
--	--------------------

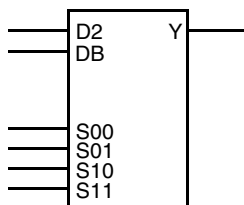
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF4 54SX, 54SX-A, 54SX-S, eX, Axcelerator

54SX, 54SX-A, 54SX-S, eX, Axcelerator

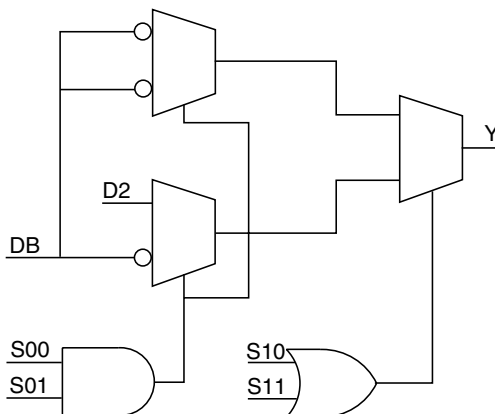


Input
D2, DB, S00, S01, S10, S11

Input	Output
Y	



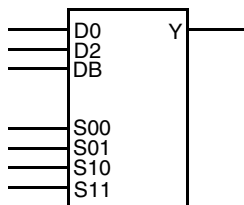
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF5 54SX, 54SX-A, 54SX-S, eX, Axcelerator

54SX, 54SX-A, 54SX-S, eX, Accelerator

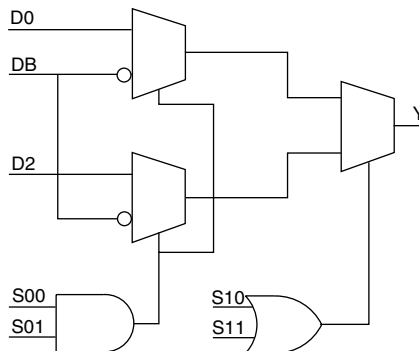


Input D0, D2, DB, S00, S01, S10, S11

Output	Y
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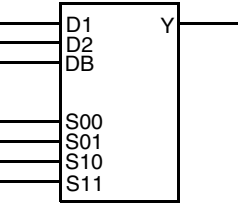
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF6

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input

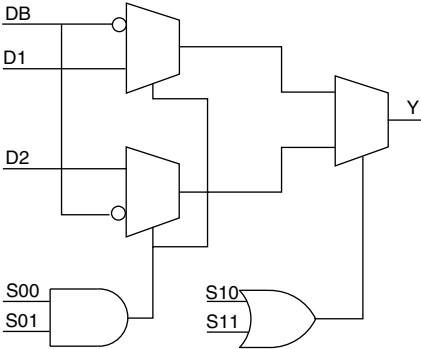
D1, D2, DB, S00, S01, S10, S11

Output

Y

Function

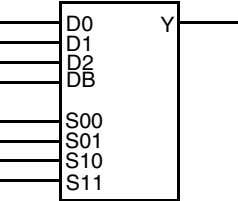
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF7

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input

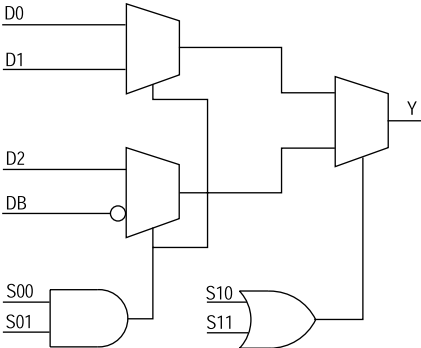
D0, D1, D2, DB, S00, S01, S10, S11

Output

Y

Function

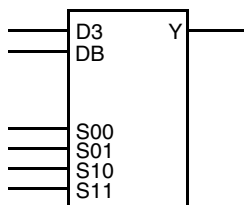
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF8 54SX, 54SX-A, 54SX-S, eX, Axcelerator

54SX, 54SX-A, 54SX-S, eX, Accelerator

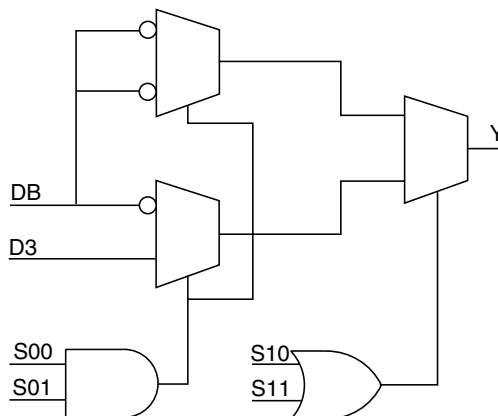


Input
D3, DB, S00, S01, S10, S11

Output
Y



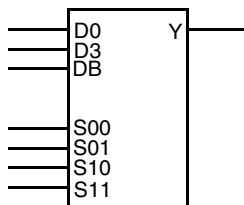
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMF9 54SX, 54SX-A, 54SX-S, eX, Axcelerator

54SX, 54SX-A, 54SX-S, eX, Axcelerator

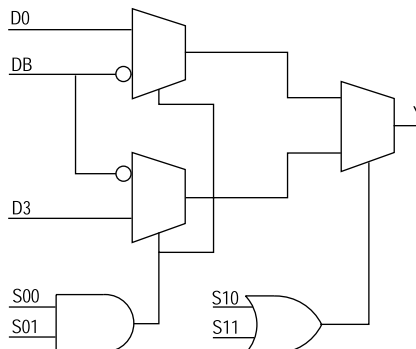


Input D0, D3, DB, S00, S01, S10, S11

Output	Y
--------	---



Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

CMFA

54SX, 54SX-A, 54SX-S, eX, Axcelerator

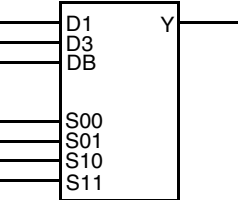
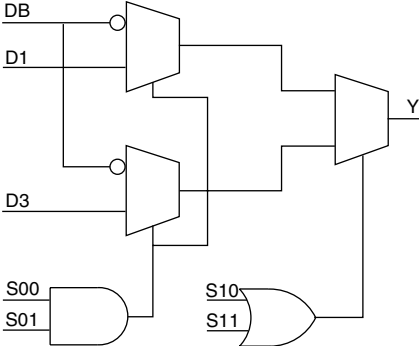


Diagram of the CMFA module symbol. It has four inputs on the left: D1, D3, DB, and a group of three inputs labeled S00, S01, and S10. There is also an input labeled S11. The output Y is on the right.

Function
Full Combinational Module



Logic diagram for the CMFA module. It shows two 3-input AND gates. The first AND gate has inputs D1, D3, and DB. The second AND gate has inputs D1, D3, and DB. The outputs of these two AND gates are connected to a 3-input OR gate. The OR gate has inputs from the two AND gates and a third input from a 2-input AND gate. The 2-input AND gate has inputs S00 and S01. The OR gate also has inputs S10 and S11. The output of the OR gate is Y.

Input	Output
D1, D3, DB, S00, S01, S10, S11	

Family	Modules	
	Seq	Comb
All listed		1

CMFB

54SX, 54SX-A, 54SX-S, eX, Axcelerator

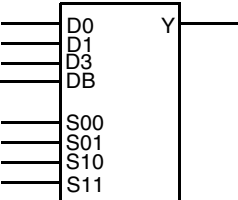
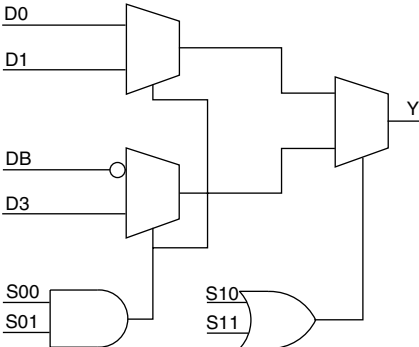


Diagram of the CMFB module symbol. It has five inputs on the left: D0, D1, D3, DB, and a group of three inputs labeled S00, S01, and S10. There is also an input labeled S11. The output Y is on the right.

Function
Full Combinational Module



Logic diagram for the CMFB module. It shows two 3-input AND gates. The first AND gate has inputs D0, D1, and DB. The second AND gate has inputs D3, DB, and D3. The outputs of these two AND gates are connected to a 3-input OR gate. The OR gate has inputs from the two AND gates and a third input from a 2-input AND gate. The 2-input AND gate has inputs S00 and S01. The OR gate also has inputs S10 and S11. The output of the OR gate is Y.

Input	Output
D0, D1, D3, DB, S00, S01, S10, S11	

Family	Modules	
	Seq	Comb
All listed		1

CMFC

54SX, 54SX-A, 54SX-S, eX, Axcelerator

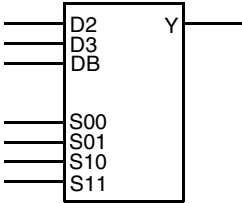
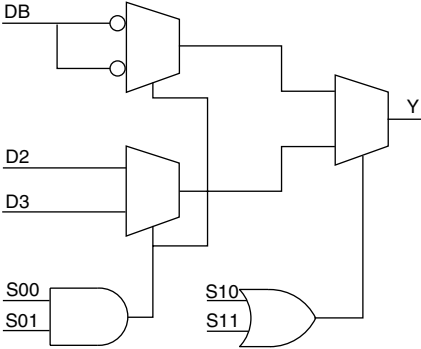


Diagram of the CMFC module symbol. It shows a rectangular box with an output line labeled 'Y' on the right. On the left side, there are two groups of inputs: a group of three inputs labeled D2, D3, and DB, and another group of four inputs labeled S00, S01, S10, and S11.

Function
Full Combinational Module



Logic diagram for the CMFC module. It shows the internal implementation using logic gates. The inputs D2, D3, and DB are connected to a 3-input AND gate. The inputs S00 and S01 are connected to a 2-input AND gate. The inputs S10 and S11 are connected to a 2-input OR gate. The outputs of these three gates are connected to a 3-input OR gate, which produces the final output Y.

Input	Output	
	D2, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

CMFD

54SX, 54SX-A, 54SX-S, eX, Axcelerator

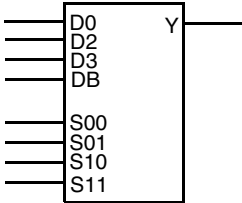
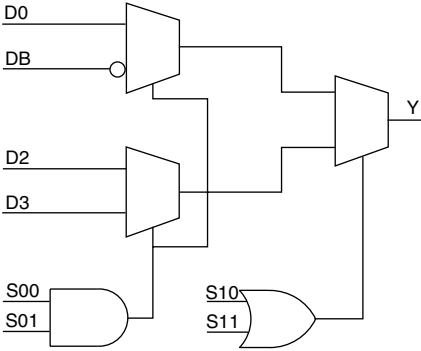


Diagram of the CMFD module symbol. It shows a rectangular box with an output line labeled 'Y' on the right. On the left side, there are two groups of inputs: a group of four inputs labeled D0, D2, D3, and DB, and another group of four inputs labeled S00, S01, S10, and S11.

Function
Full Combinational Module



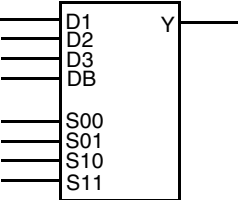
Logic diagram for the CMFD module. It shows the internal implementation using logic gates. The inputs D0, D2, and DB are connected to a 3-input AND gate. The inputs D3 and S00 are connected to a 2-input AND gate. The inputs S01 and S10 are connected to a 2-input AND gate. The inputs S11 and S10 are connected to a 2-input OR gate. The outputs of these four gates are connected to a 4-input OR gate, which produces the final output Y.

Input	Output	
	D0, DB, D2, D3, S00, S01, S10, S11	Y

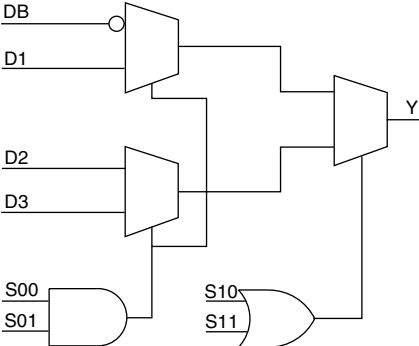
Family	Modules	
	Seq	Comb
All listed		1

CMFE

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Full Combinational Module

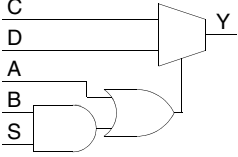


Input D1, D2, D3, DB, S00, S01, S10, S11	Output Y
--	--------------------

Family	Modules	
	Seq	Comb
All listed		1

CS1

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1
1	X	X	X	0	0
X	X	X	1	1	1

Input A, S, B, C, D	Output Y
-------------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

CS2

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; C --- OR1[OR]; D --- OR1; B --- OR1; A --- OR1; S --- AND1[AND]; B --- AND1; AND1 --- A; OR1 --- Y
```

Input
A, S, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

Function
Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1
1	X	1	X	0	0
X	X	X	1	1	1

CY2A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; B1 --- OR1[OR]; A1 --- OR1; B0 --- OR1; A0 --- OR1; OR1 --- Y
```

Input
A1, B1, A0, B0

Output
Y

Family	Modules	
	Seq	Comb
All listed		1

Function
Carry Generator

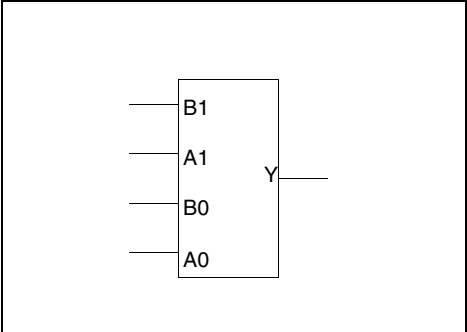
Truth Table

A1	B1	A0	B0	Y
X	0	X	0	0
X	0	0	X	0
0	0	X	X	0
0	X	X	0	0
0	X	0	X	0
X	1	1	1	1
1	X	1	1	1
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

CY2B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
A1, B1, A0, B0	Y

Function
Carry Generator

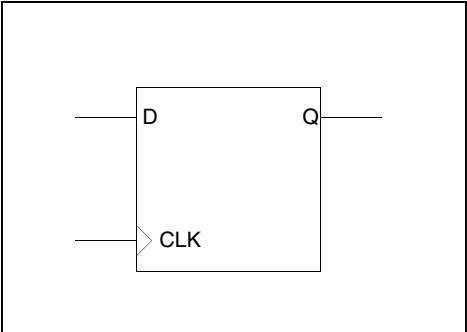
Truth Table

A1	B1	A0	B0	Y
X	0	0	0	0
0	0	X	X	0
0	X	0	0	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

DF1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input	Output
D, CLK	Q

Function
D-Type Flip-Flop

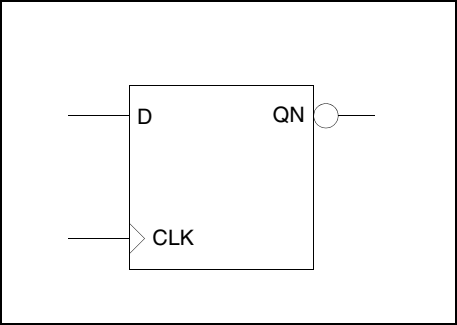
Truth Table

CLK	Q _{n+1}
↑	D

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DF1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with active low Output

Truth Table

CLK	QN _{n+1}
↑	!D

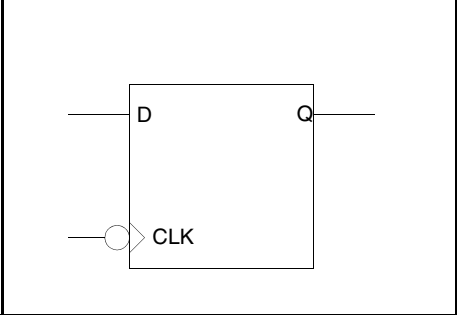
Input
D, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
D-Type Flip-Flop with active low Clock

Truth Table

CLK	Q _{n+1}
↓	D

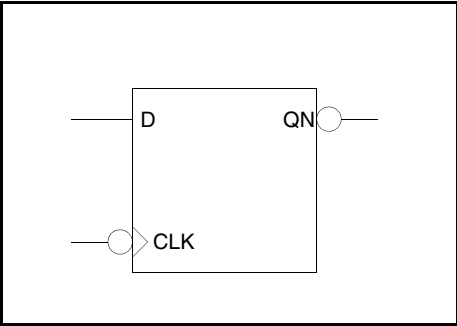
Input
D, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1C

ACT 1, 40MX,ACT2/1200XL, ACT3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

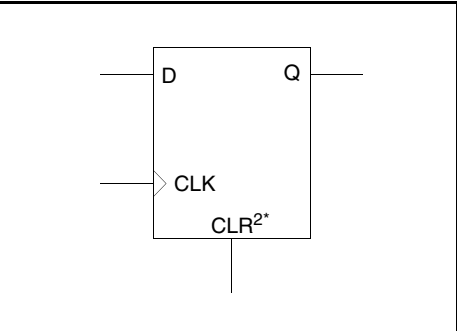
CLK	Q _N _{n+1}
↓	!D

Input	Output
D, CLK	Q _N

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active high Clear

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↑	D

Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

DFC1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic symbol for DFC1A D-Type Flip-Flop. Inputs: D, CLK (clock), CLR (active low clear, marked with *2). Output: Q.

Function
D-Type Flip-Flop with active high Clear and active low Clock

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

Input CLR, D, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

DFC1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic symbol for DFC1B D-Type Flip-Flop. Inputs: D, CLK (clock), CLR (active low clear). Output: Q.

Function
D-Type Flip-Flop with active low Clear

Truth Table

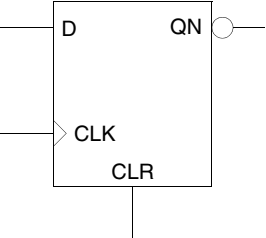
CLR	CLK	Q _{n+1}
0	X	0
1	↑	D

Input CLR, D, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFC1C

ACT 1, 40MX



Function

D-Type Flip-Flop with active high Clear and Clock

Truth Table

CLR	CLK	Q _{n+1}
1	X	1
0	↑	!D

Input

CLR, D, CLK

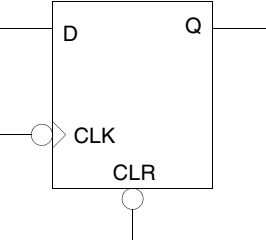
Output

QN

Family	Modules	
	Seq	Comb
ACT 1; 40MX		2

DFC1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Clear and Clock

Truth Table

CLR	CLK	Q _{n+1}
0	X	0
1	↓	D

Input

CLR, D, CLK

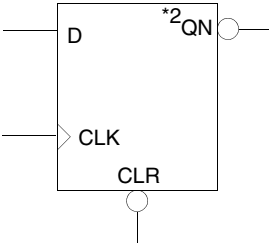
Output

Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFC1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with active low Clear and Output

Truth Table

CLR	CLK	QN _{n+1}
0	X	1
1	↑	!D

Input
CLR, D, CLK

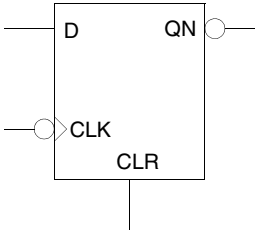
Output
QN

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFC1F

ACT 1, 40MX



Function
D-Type Flip-Flop with active high Clear, active low Clock and Output

Truth Table

CLR	CLK	QN _{n+1}
1	X	1
0	↓	!D

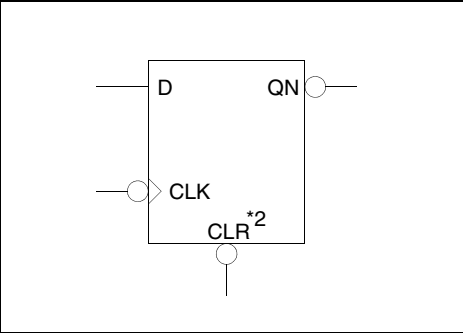
Input
CLR, D, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2

DFC1G

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with active low Clear, Clock and Output

Truth Table

CLR	CLK	Q _{n+1}
0	X	1
1	↓	!D

Input
CLR, D, CLK

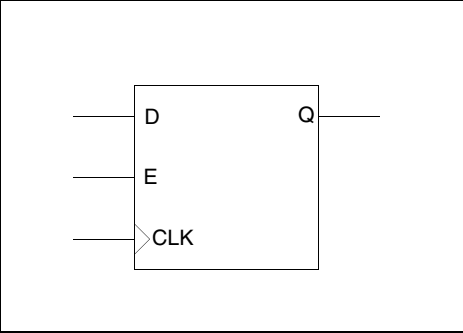
Output
QN

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFE

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with active high Enable

Truth Table

E	CLK	Q _{n+1}
0	X	Q
1	↑	D

Input
D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFE1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram of DFE1B: A D-Type Flip-Flop with active low Enable. The inputs are D, E (active low), and CLK (active low). The output is Q.

Function
D-Type Flip-Flop with active low Enable

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Input
D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFE1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram of DFE1C: A D-Type Flip-Flop with active low Enable and Clock. The inputs are D, E (active low), and CLK (active low). The output is Q.

Function
D-Type Flip-Flop with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

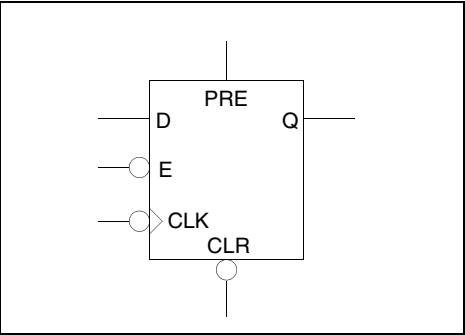
Input
D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFE2D

ACT 1, 40MX



Input
CLR, D, E, PRE, CLK

Output
Q

Function

D-Type Flip-Flop with active high Preset, active low Enable, Clear, and Clock

Truth Table

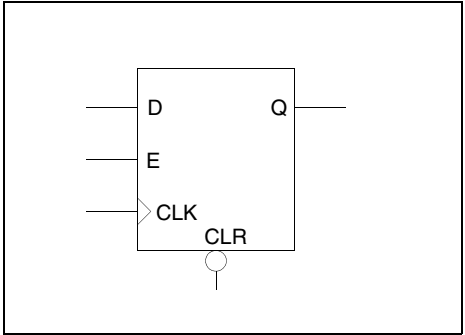
CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFE3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Input
CLR, D, E, CLK

Output
Q

Function

D-Type Flip-Flop, with Enable and active low Clear

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	0	X	Q
1	1	↑	D

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFE3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic diagram of DFE3B D-Type Flip-Flop with Enable and active low Clear and Clock. Inputs: D, E, CLR (active low), CLK (active low). Output: Q.

Function
D-Type Flip-Flop with Enable and active low Clear and Clock

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	0	X	Q
1	1	↓	D

Input
CLR, D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram of DFE3C D-Type Flip-Flop with Active Low Enable and Clear. Inputs: D, E (active low), CLR (active low), CLK. Output: Q.

Function
D-Type Flip-Flop with Active Low Enable and Clear

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input
CLR, D, E, CLK

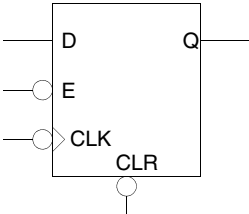
Output
Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

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DFE3D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable, Clear and Clock

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↓	D

Input

CLR, D, E, CLK

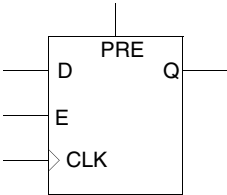
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE4

ACT 1, 40MX



Function

D-Type Flip-Flop with active high Enable and Preset

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	0	X	Q
0	1	↑	D

Input

D, E, PRE, CLK

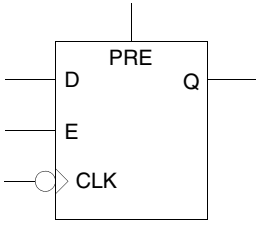
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4A

ACT 1, 40MX



Function

D-Type Flip-Flop with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	0	X	Q
0	1	↓	D

Input

D, E, PRE, CLK

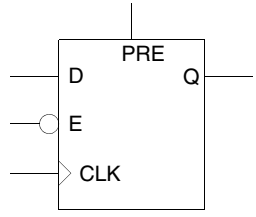
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4B

ACT 1, 40MX



Function

D-Type Flip-Flop with active low Enable, and active high Preset

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	1	X	Q
0	0	↑	D

Input

D, E, PRE, CLK

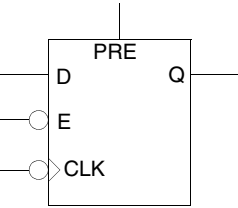
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4C

ACT 1, 40MX



Function

D-Type Flip-Flop with active low Enable and Clock, and active high Preset

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	1	X	Q
0	0	↓	D

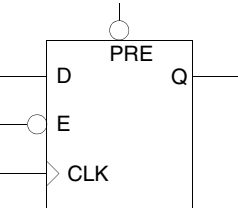
Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4F

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable and Preset

Truth Table

PRE	E	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

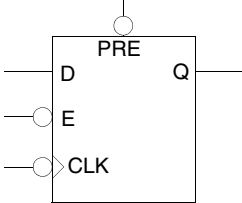
Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
All listed	1	

DFE4G

54SX, 54SX-A, 54SX-S, eX, Accelerator



Function

D-Type Flip-Flop with active low Enable, Clock, and Preset

Truth Table

PRE	E	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↓	D

Input

D, E, PRE, CLK

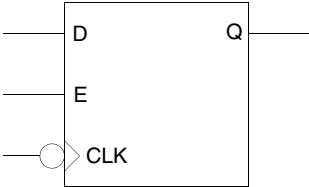
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFEA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q _{n+1}
0	X	Q
1	↓	D

Input

D, E, CLK

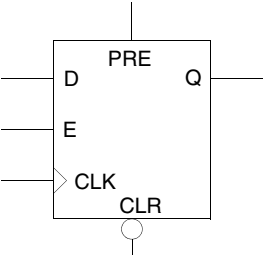
Output

Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	

DFEB

ACT 1, 40MX



Function
D-Type Flip-Flop with Enable, Preset, and active low Clear

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

Input
CLR, D, E, PRE, CLK

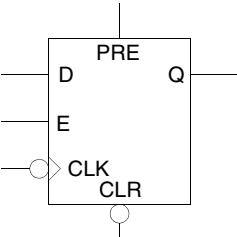
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

*Your design should not allow both PRE and CLR to be asserted at the same time.

DFEC

ACT 1, 40MX



Function
D-Type Flip-Flop with Enable, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFED

ACT 1, 40MX

Logic symbol for DFED D-Type Flip-Flop. Inputs: D, E (active low), CLK, CLR (active low). Output: Q. PRE is also shown as an input.

Function
D-Type Flip-Flop with active low Enable and Clear, and active high Preset

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↑	D
0	1	X	X	*

Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFEG

54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic symbol for DFEG D-Type Flip-Flop. Inputs: D, E (active low), CLK, CLR (active low). Output: Q. PRE is also shown as an input.

Function
D-Type Flip-Flop with active low Enable, Preset, and Clear

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↑	D

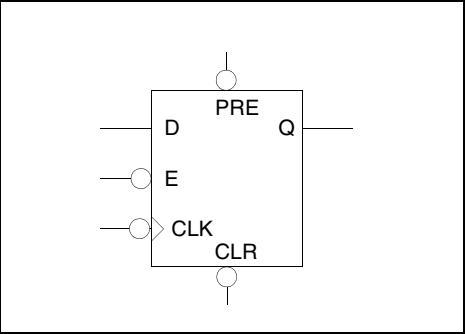
Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
All listed	1	

DFEH

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input

CLR, D, E, PRE, CLK

Output

Q

Function

D-Type Flip-Flop with active low Enable, Clear, Preset, and Clock

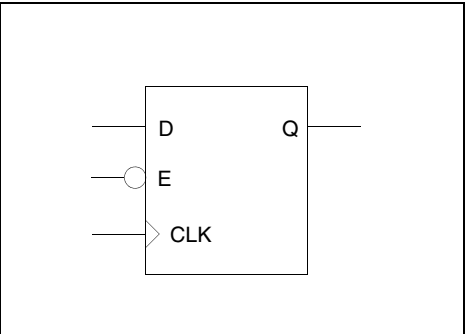
Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

Family	Modules	
	Seq	Comb
All listed	1	

IODFE

ACT 3



Input

D, E, CLK

Output

Q

Function

D-Type Flip-Flop with active low Enable

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↑	D

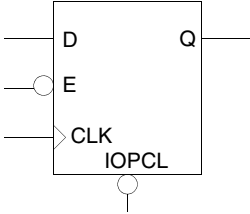
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.

NOTE 2: Uses an I/O module.

IODFEC

ACT 3



The logic diagram shows a D-Type Flip-Flop with inputs D, E, CLK, and IOPCL. The output is Q. The IOPCL input is active low, indicated by a bubble at the input pin.

Function

D-Type Flip-Flop with active low Enable and Clear

Truth Table

IOPCL	E	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input

IOPCL, D, E, CLK

Output

Q

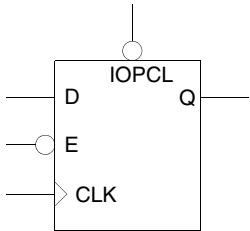
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

NOTE 2: Uses an I/O module.

NOTE 3: The IOPCL pin must be driven by the IOPCLBUF macro.

IODFEP

ACT 3



The logic diagram shows a D-Type Flip-Flop with inputs D, E, CLK, and IOPCL. The output is Q. The IOPCL input is active low, indicated by a bubble at the input pin.

Function

D-Type Flip-Flop with active low Enable and Preset

Truth Table

IOPCL	E	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Input

IOPCL, D, E, CLK

Output

Q

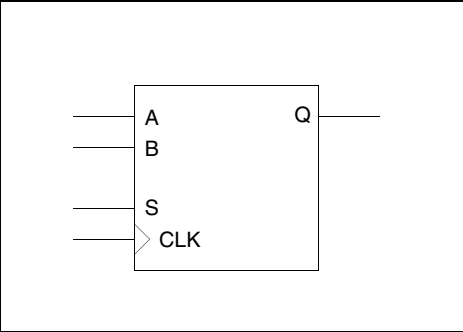
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.

NOTE 3: Uses an I/O module.

DFM

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Input A, B, S, CLK	Output Q
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Function
D-Type Flip-Flop with 2-input Multiplexed Data

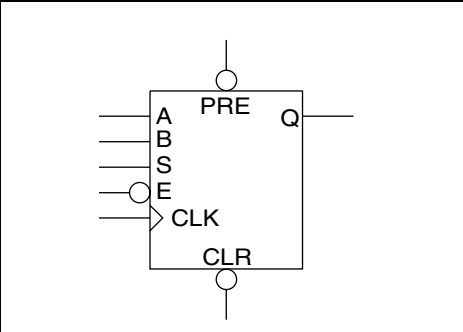
Truth Table

S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFMEG

Axcelerator



Input CLK, A, B, S, E, PRE, CLR	Output Q
------------------------------------	-------------

Function
D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable, Preset, and Clear

Truth Table

CLR	PRE	E	S	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↑	A
1	1	0	1	↑	B

Family	Modules	
	Seq	Comb
All listed	1	

DFMEH

Axcelerator

Logic diagram of DFMEH D-Type Flip-Flop. Inputs: A, B, S, E, CLK, CLR. Output: Q. PRE is also shown as an input.

Input
CLK, A, B, S, E, PRE, CLR

Output
Q

Function
D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable, Preset, and Clear

Truth Table

CLR	PRE	E	S	CLK	Q _{n+1}
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↓	A
1	1	0	1	↓	B

Family	Modules	
	Seq	Comb
All listed	1	

DFM1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic diagram of DFM1B D-Type Flip-Flop. Inputs: A, B, S, CLK. Output: QN.

Input
A, B, S, CLK

Output
QN

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

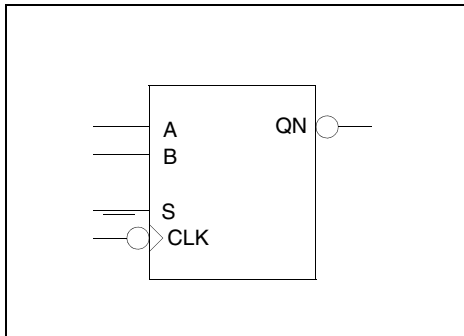
Truth Table

S	CLK	QN _{n+1}
0	↑	!A
1	↑	!B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

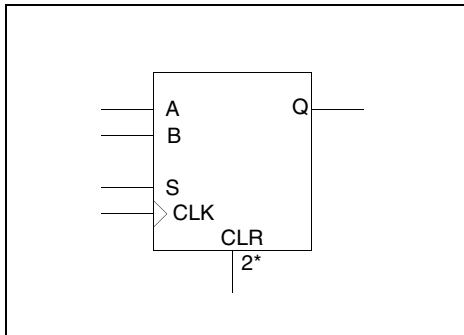
S	CLK	QN _{n+1}
0	↓	!A
1	↓	!B

Input A, B, S, CLK	Output QN
------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM3

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear

Truth Table

CLR	S	CLK	Q _{n+1}
1	x	x	B
0	1	↑	0
0	0	↑	A

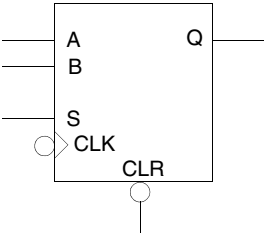
Input A, B, CLR, S, CLK	Output Q
-----------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

DFM3B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

Truth Table

CLR	S	CLK	Q _{n+1}
0	X	X	0
1	0	↓	A
1	1	↓	B

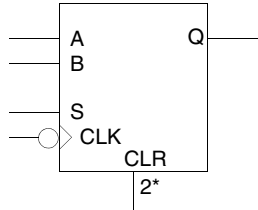
Input
A, B, CLR, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM3E

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

Truth Table

CLR	S	CLK	Q _{n+1}
1	X	X	0
0	0	↓	A
0	1	↓	B

Input
A, B, CLR, S, CLK

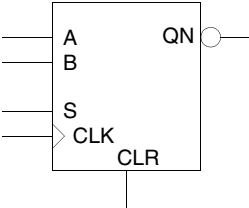
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

DFM3F

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output

Truth Table

CLR	S	CLK	QN _{n+1}
1	X	X	1
0	0	↑	!A
0	1	↑	!B

Input

A, B, CLR, S, CLK

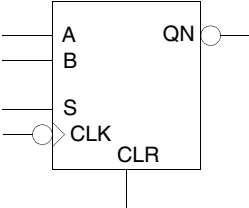
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM3G

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output

Truth Table

CLR	S	CLK	QN _{n+1}
1	X	X	1
0	0	↓	!A
0	1	↓	!B

Input

A, B, CLR, S, CLK

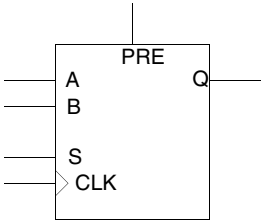
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

Truth Table

PRE	S	CLK	Q _{n+1}
1	X	X	1
0	0	↑	A
0	1	↑	B

Input

A, B, PRE, S, CLK

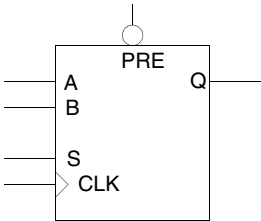
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4A

ACT 1, 40MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

Truth Table

PRE	S	CLK	Q _{n+1}
0	X	X	1
1	0	↑	A
1	1	↑	B

Input

A, B, PRE, S, CLK

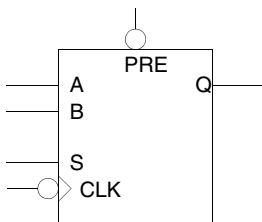
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4B

ACT 1, 40MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↓	A
1	1	↓	B

Input

A, B, PRE, S, CLK

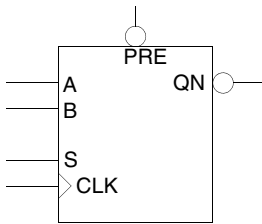
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

Truth Table

PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↑	!A
1	1	↑	!B

Input

A, B, PRE, S, CLK

Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM4D

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic diagram of DFM4D: A D-Type Flip-Flop with 2-input Multiplexed Data (A, B), active low Preset (PRE), Set (S), and Clock (CLK). The output is QN.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

Truth Table

PRE	S	CLK	QN _{n+1}
0	X	X	0
1	0	↓	!A
1	1	↓	!B

Input
A, B, PRE, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM4E

ACT 1, 40MX

Logic diagram of DFM4E: A D-Type Flip-Flop with 2-input Multiplexed Data (A, B), Preset (PRE), Set (S), and Clock (CLK). The output is Q.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

Truth Table

PRE	S	CLK	Q _{n+1}
1	X	X	1
0	0	↓	A
0	1	↓	B

Input
A, B, PRE, S, CLK

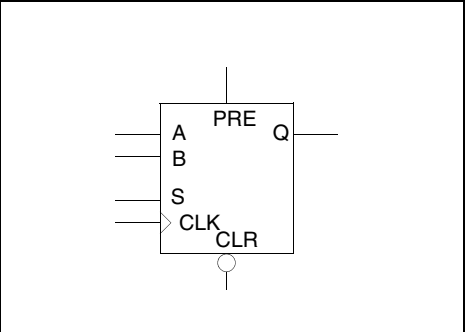
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

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DFM5A

ACT 1, 40MX



Input	Output
A, B, CLR, PRE, S, CLK	Q

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

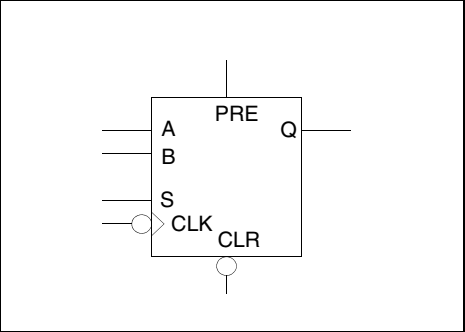
Truth Table				
CLR	PRE	S	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↑	A
1	0	1	↑	B
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM5B

ACT 1, 40MX



Input	Output
A, B, CLR, PRE, S, CLK	Q

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

Truth Table				
CLR	PRE	S	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↓	A
1	0	1	↓	B
0	1	X	X	*

Family	Modules	
	Seq	Comb
All listed		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM6A

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Logic diagram of DFM6A: A D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock. Inputs: D0, D1, D2, D3, S0, S1, CLK, CLR. Output: Q. CLR is active low.

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

CLR	S1	S0	CLK	Q _{n+1}
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

Input

D0, D1, D2, D3, S0, S1, CLK, CLR

Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFM6B

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Logic diagram of DFM6B: A D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock. Inputs: D0, D1, D2, D3, S0, S1, CLK, CLR. Output: Q. CLR is active low.

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

Truth Table

CLR	S1	S0	CLK	Q _{n+1}
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Input

D0, D1, D2, D3, S0, S1, CLK, CLR

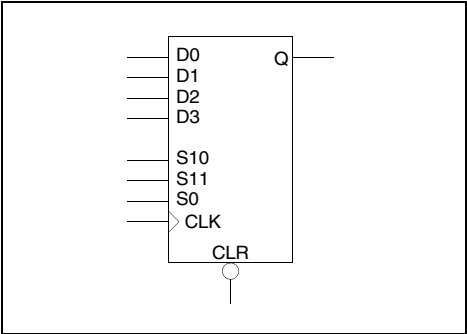
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFM7A

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Input	Output
D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Q

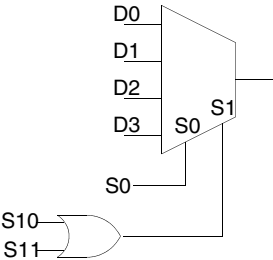
Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table					
CLR	S11	S10	S0	CLK	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

Family	Modules	
	Seq	Comb
All listed	1	

NOTE 1: The DFM7A macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM7B

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table

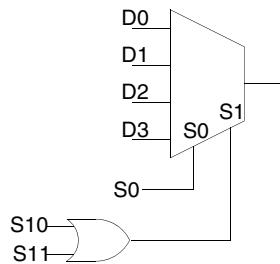
CLR	S11	S10	S0	CLK	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Input	Output
D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

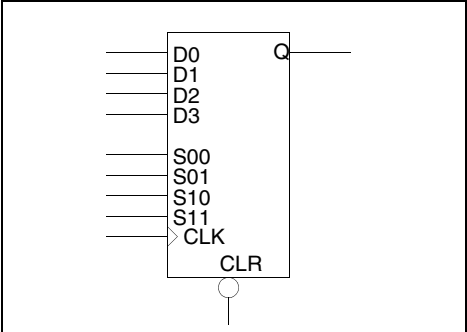
NOTE 1: The DFM7B macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8A

ACT 3



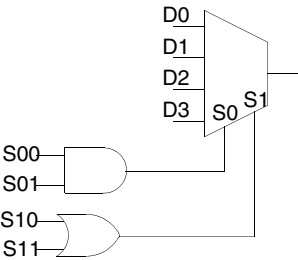
Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Q

Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table						
CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2
1	1	X	1	1	↑	D3
1	X	1	1	1	↑	D3

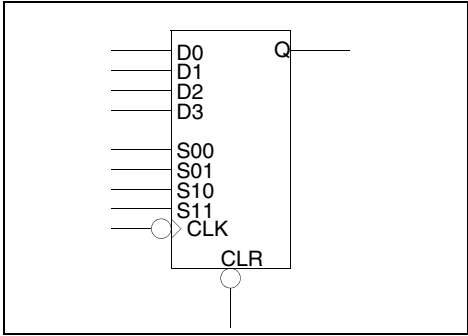
Family	Modules	
	Seq	Comb
ACT3	1	

NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8B

ACT 3



Input

D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Output

Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table

CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2
1	1	X	1	1	↓	D3
1	X	1	1	1	↓	D3

Family	Modules	
	Seq	Comb
ACT3	1	

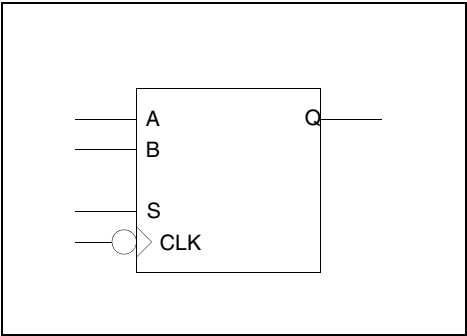
NOTE 1: The DFM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.

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DFMA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Input	Output
A, B, S, CLK	Q

Function

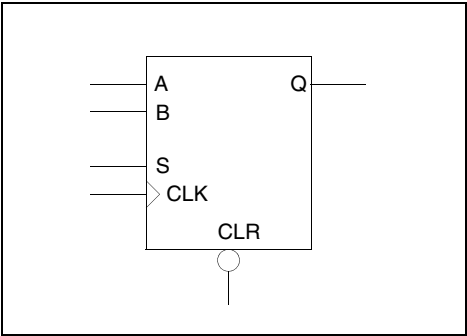
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q_{n+1}
0	↓	A
1	↓	B

DFMB

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Input	Output
A, B, CLR, S, CLK	Q

Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear

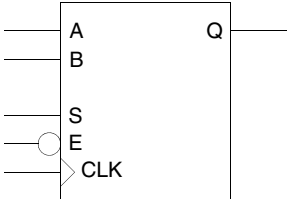
Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFME1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Function

2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

Truth Table

E	S	CLK	Q _{n+1}
1	X	X	Q
0	0	↑	A
0	1	↑	B

Input

A, B, S, E, CLK

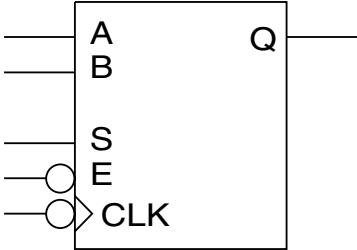
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFME1B

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable

Truth Table

E	S	CLK	Q _{n+1}
1	X	X	Q
0	0	↓	A
0	1	↓	B

Input

CLK, A, B, S, E,

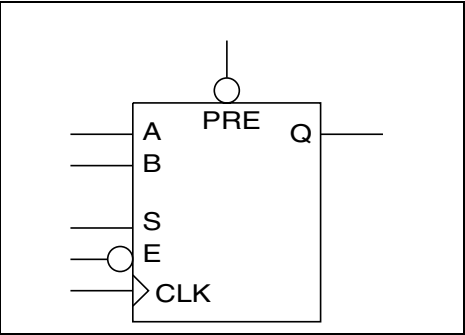
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME2A

Axcelerator



Input
CLK, A, B, S, E, PRE

Output
Q

Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Preset

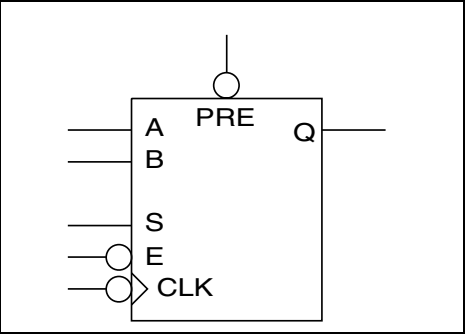
Truth Table

PRE	E	S	CLK	Q_{n+1}
0	X	X	X	1
1	1	X	X	Q
1	0	0	$\uparrow$	A
1	0	1	$\uparrow$	B

Family	Modules	
	Seq	Comb
All listed	1	

DFME2B

Axcelerator



Input
CLK, A, B, S, E, PRE

Output
Q

Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Preset

Truth Table

PRE	E	S	CLK	Q_{n+1}
0	X	X	X	1
1	1	X	X	Q
1	0	0	$\downarrow$	A
1	0	1	$\downarrow$	B

Family	Modules	
	Seq	Comb
All listed	1	

DFME3A

Axcelerator

Logic diagram of DFME3A D-Type Flip-Flop. Inputs: A, B, S, E (active-low), CLK (rising-edge), CLR (active-low). Output: Q.

Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Clear

Truth Table

CLR	E	S	CLK	Q_{n+1}
0	X	X	X	0
1	1	X	X	Q
1	0	0	↑	A
1	0	1	↑	B

Input

CLK, A, B, S, E, CLR

Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME3B

Axcelerator

Logic diagram of DFME3B D-Type Flip-Flop. Inputs: A, B, S, E (active-low), CLK (falling-edge), CLR (active-low). Output: Q.

Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Clear

Truth Table

CLR	E	S	CLK	Q_{n+1}
0	X	X	X	0
1	1	X	X	Q
1	0	0	↓	A
1	0	1	↓	B

Input

CLK, A, B, S, E, CLR

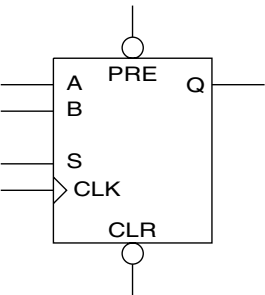
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFMPCA

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Preset and Clear

Truth Table

CLR	PRE	S	CLK	Q _{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	0	↑	A
1	1	1	↑	B

Input

CLK, A, B, S, E, PRE, CLR

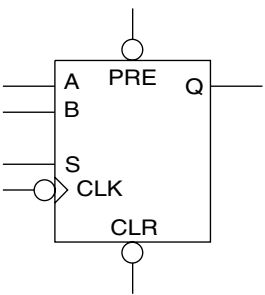
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFMPCB

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Preset and Clear

Truth Table

CLR	PRE	S	CLK	Q _{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	0	↓	A
1	1	1	↓	B

Input

CLK, A, B, S, E, PRE, CLR

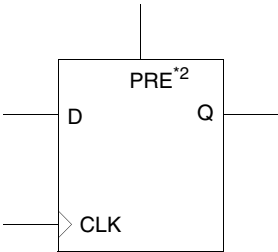
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DFP1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↑	D

Input

D, PRE, CLK

Output

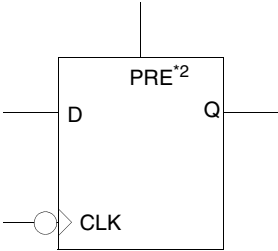
Q

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX, 54SX-A, 54SX-S, and eX.

DFP1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↓	D

Input

D, PRE, CLK

Output

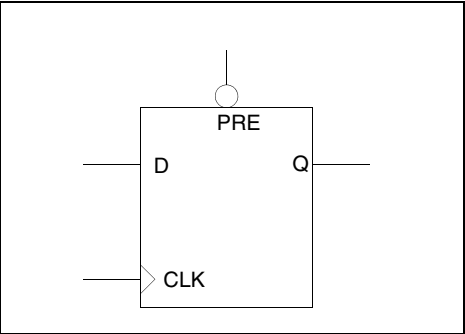
Q

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX, 54SX-A, 54SX-S, and eX.

DFP1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, SX-A, 54SX-S, eX, Axcelerator



Function
D-Type Flip-Flop with active low Preset

Truth Table

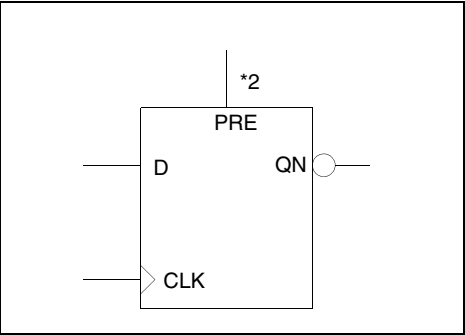
PRE	CLK	Q _{n+1}
0	X	1
1	↑	D

Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX	1	
Others		2

DFP1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with active high Preset, and active low Output

Truth Table

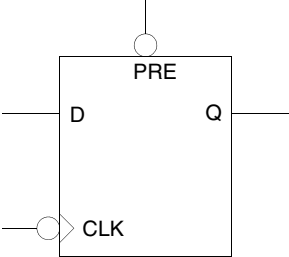
PRE	CLK	QN _{n+1}
1	X	0
0	↑	!D

Input D, PRE, CLK	Output QN
-----------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

DFP1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

Input

D, PRE, CLK

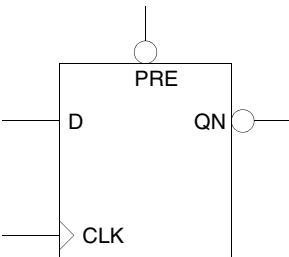
Output

Q

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX	1	
Others		2

DFP1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active low Preset and Output

Truth Table

PRE	CLK	QN_{n+1}
0	X	0
1	↑	!D

Input

D, PRE, CLK

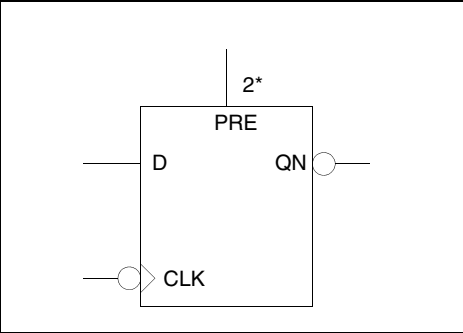
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFP1F

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active high Preset, and active low Clock and Output

Truth Table

PRE	CLK	QN _{n+1}
1	X	0
0	↓	!D

Input

D, PRE, CLK

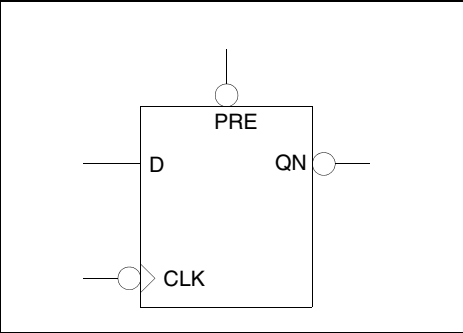
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

DFP1G

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active low Preset, Clock and Output

Truth Table

PRE	CLK	QN _{n+1}
0	X	0
1	↓	!D

Input

D, PRE, CLK

Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFPC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Input
CLR, D, PRE, CLK

Output
Q

Function
D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

Family	Modules	
	Seq	Comb
Others	1	1
ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX		2

* A 2 on the symbol implies 2 logic module delays only for 54SX, 54SX-A, 54SX-S, and eX.

** In ACT 1/40MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DFPCA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Input
CLR, D, PRE, CLK

Output
Q

Function
D-Type Flip-Flop with active high Preset, active low Clear and Clock

Truth Table

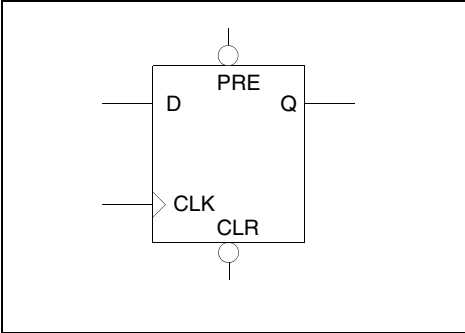
CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFPCB

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop, with active low Clear, and Preset

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	X	X	0
1	0	X	1
1	1	↑	D

Input

CLR, D, PRE, CLK

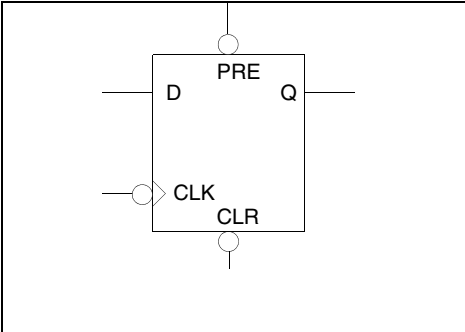
Output

Q

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX	1	

DFPCC

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset, Clear and Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	X	X	0
1	0	X	1
1	1	↓	D

Input

CLR, D, PRE, CLK

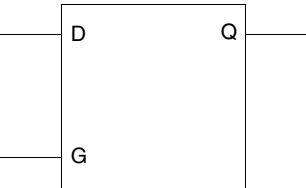
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DL1

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Data Latch

Truth Table

G	Q _{n+1}
0	Q
1	D

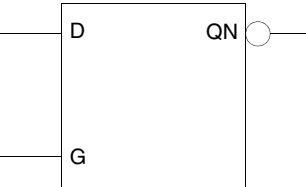
Input
D, G

Output
Q

Family	Modules	
	Seq	Comb
ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX		1
Others	1	

DL1A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Function
Data Latch with active low Output

Truth Table

G	QN _{n+1}
0	QN
1	!D

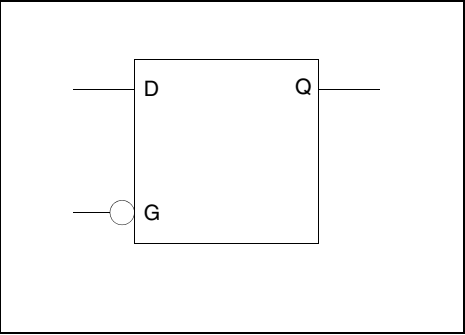
Input
D, G

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DL1B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
D, G

Output
Q

Function

Data Latch with active low Clock

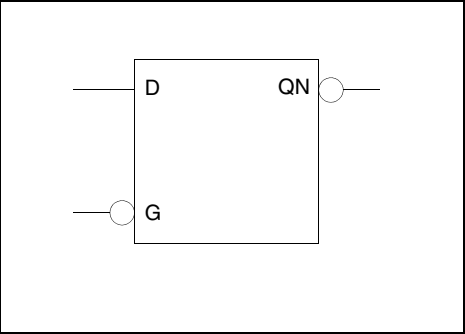
Truth Table

G	Q _{n+1}
1	Q
0	D

Family	Modules	
	Seq	Comb
ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX		1
Others	1	

DL1C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Input
D, G

Output
QN

Function

Data Latch, with active low Clock and Output

Truth Table

G	QN _{n+1}
1	QN
0	!D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DL2A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Function
Data Latch with active low Clear and active high Preset

Truth Table

CLR	PRE	G	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

Input CLR, D, G, PRE	Output Q
--------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

*In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

Function
Data Latch with active high Clear and active low Preset, Clock, and Output

Truth Table

CLR	PRE	G	QN _{n+1}
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

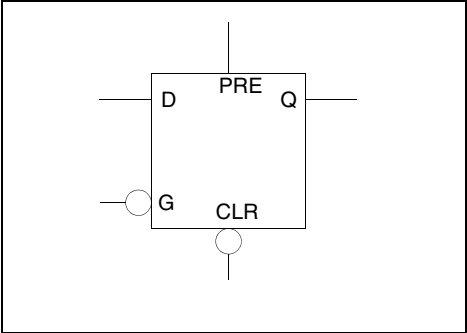
Input CLR, D, G, PRE	Output QN
--------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

*In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Data Latch with active low Clear, active high Preset, and active low Clock

Truth Table

CLR	PRE	G	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

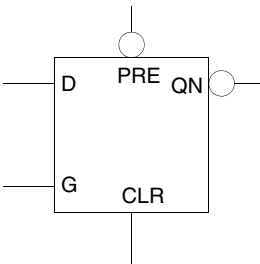
Input CLR, D, G, PRE	Output Q
--------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

*In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2D

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX



Function
Data Latch with active high Clear and active low Preset and Output

Truth Table

CLR	PRE	G	QN _{n+1}
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	ID
1	0	X	*

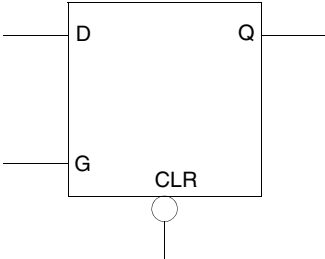
Input CLR, D, G, PRE	Output QN
--------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

*In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DLC

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
Data Latch with active low Clear

Truth Table

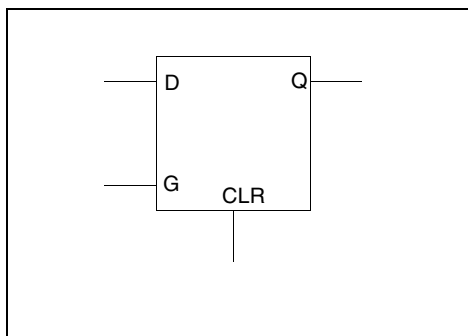
CLR	G	Q _{n+1}
0	X	0
1	0	Q
1	1	D

Input CLR, D, G	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX		1
Others	1	

DLC1

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Data Latch with active high Clear

Truth Table

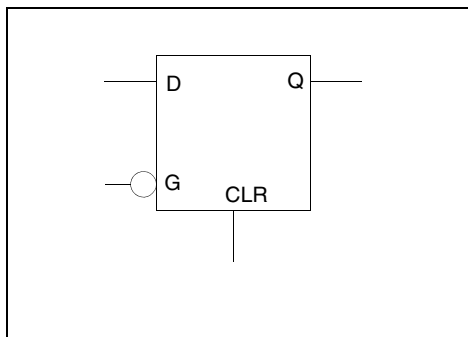
CLR	G	Q_{n+1}
1	X	0
0	0	Q
0	1	D

Input
CLR, D, GOutput
Q

Family	Modules	
	Seq	Comb
All		1

DLC1A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Data Latch with active high Clear and active low Clock

Truth Table

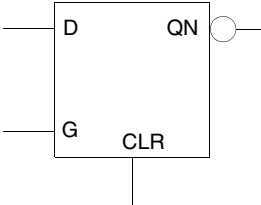
CLR	G	Q_{n+1}
1	X	0
0	1	Q
0	0	D

Input
CLR, D, GOutput
Q

Family	Modules	
	Seq	Comb
All		1

DLC1F

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Function

Data Latch with active high Clear and active low Output

Truth Table

CLR	G	QN _{n+1}
1	X	1
0	0	QN
0	1	!D

Input

CLR, D, G

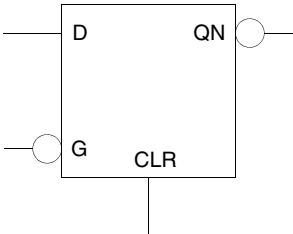
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

DLC1G

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Function

Data Latch with active high Clear and active low Clock and Output

Truth Table

CLR	G	QN _{n+1}
1	X	1
0	1	QN
0	0	!D

Input

CLR, D, G

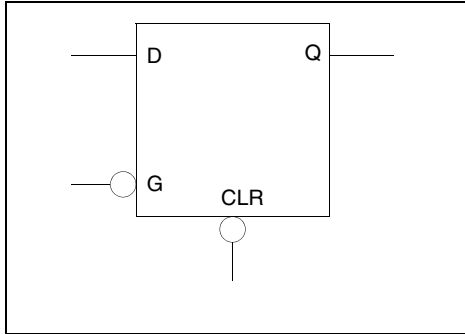
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

DLCA

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Data Latch with active low Clear and Clock

Truth Table

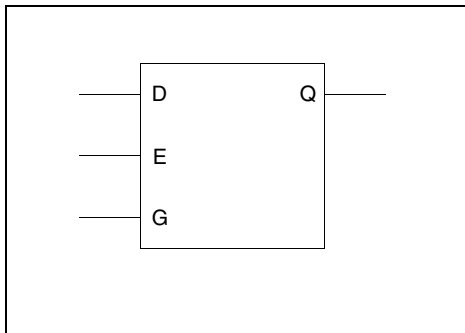
CLR	G	Q_{n+1}
0	X	0
1	1	Q
1	0	D

Input
CLR, D, G**Output**
Q

Family	Modules	
	Seq	Comb
Others		1
ACT 2, 1200XL, ACT 3, 3200DX, 42MX	1	

DLE

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator

**Function**

Data Latch with active high Enable

Truth Table

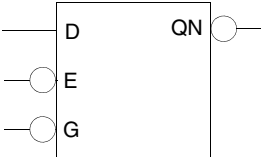
E	G	Q_{n+1}
0	X	Q
X	0	Q
1	1	D

Input
D, E, G**Output**
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE1D

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Function

Data Latch with active low Enable and Clock and active low Output

Truth Table

E	G	QN _{n+1}
1	X	QN
X	1	QN
0	0	!D

Input

D, E, G

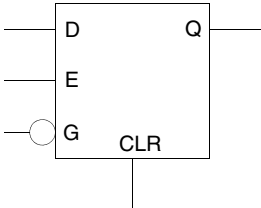
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE2A

ACT 1, 40MX



Function

Data Latch with active high Enable and Clear, and active low Clock

Truth Table

CLR	E	G	Q _{n+1}
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	D

Input

CLR, D, E, G

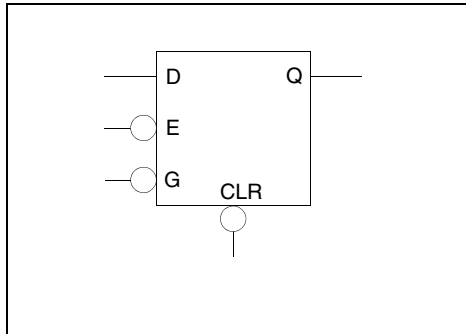
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

DLE2B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator



Input
CLR, D, E, G

Output
Q

Function

Data Latch with active low Enable, Clear, and Clock

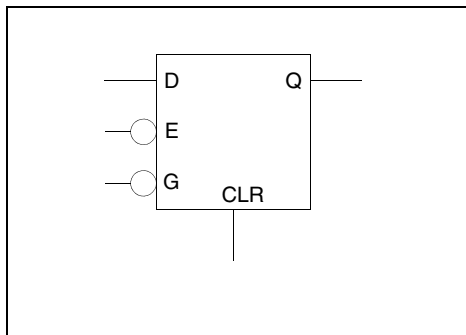
Truth Table

CLR	E	G	Q_{n+1}
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE2C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
CLR, D, E, G

Output
Q

Function

Data Latch with active low Enable and Clock, and active high Clear

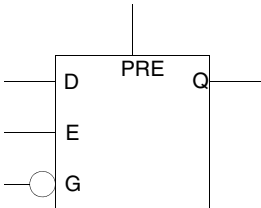
Truth Table

CLR	E	G	Q_{n+1}
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Family	Modules	
	Seq	Comb
All		1

DLE3A

ACT 1, 40MX



Function

Data Latch with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	G	Q _{n+1}
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Input

D, E, G, PRE

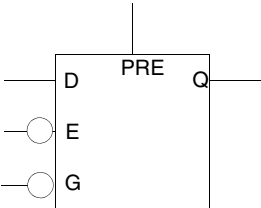
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

DLE3B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Data Latch with active low Enable and Clock, and active high Preset

Truth Table

PRE	E	G	Q _{n+1}
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

Input

D, E, G, PRE

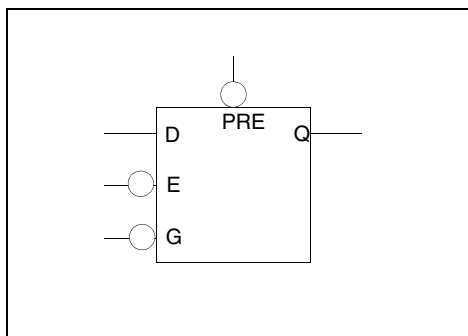
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLE3C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator


Input
D, E, G, PRE

Output
Q
Function

Data Latch with active low Enable, Preset, and Clock

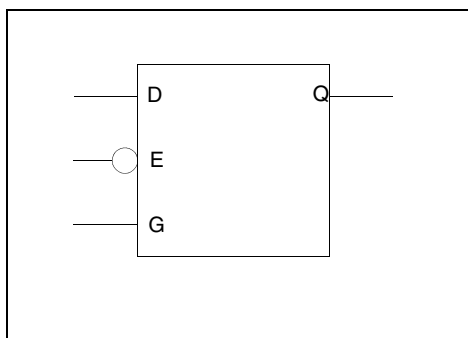
Truth Table

PRE	E	G	Q_{n+1}
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
All		1

DLEA

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, Axcelerator


Input
D, E, G

Output
Q
Function

Data Latch with active low Enable and active high Clock

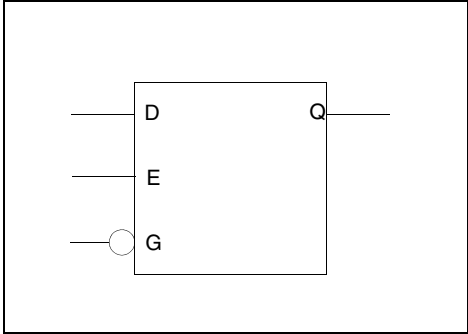
Truth Table

E	G	Q_{n+1}
1	X	Q
X	0	Q
0	1	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLEB

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Input D, E, G	Output Q
-------------------------	--------------------

Function

Data Latch with active high Enable, and active low Clock

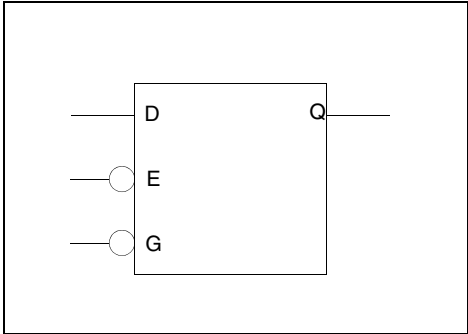
Truth Table

E	G	Q _{n+1}
0	X	Q
X	1	Q
1	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLEC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Input D, E, G	Output Q
-------------------------	--------------------

Function

Data Latch with active low Enable and Clock

Truth Table

E	G	Q _{n+1}
1	X	Q
X	1	Q
0	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLM

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator

Function
Data Latch with 2-input Multiplexed Data

Truth Table

S	G	Q_{n+1}
X	0	Q
0	1	A
1	1	B

Input A, B, S, G	Output Q
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLM2

ACT 2/1200XL, ACT 3, 3200DX, 42MX, Axcelerator

Function
Data Latch with 2-input Multiplexed Data and Active-Low Clear

Truth Table

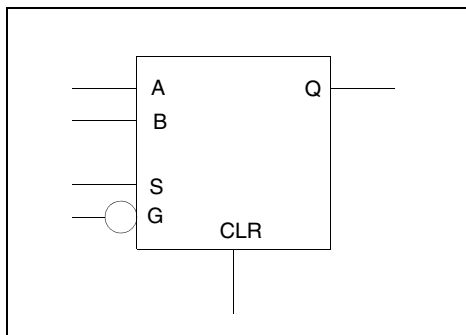
CLR	S	G	Q_{n+1}
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Input A, B, S, G, CLR	Output Q
---------------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed	1	

DLM2A

ACT 1, 40MX



Input
A, B, CLR, S, G

Output
Q

Function

Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

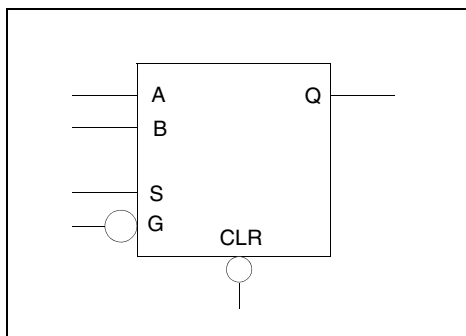
Truth Table

CLR	S	G	Q_{n+1}
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

DLM2B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, Accelerator



Input
A, B, CLR, S, G

Output
Q

Function

Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

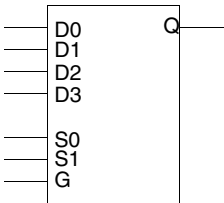
Truth Table

CLR	S	G	Q_{n+1}
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

Family	Modules	
	Seq	Comb
All listed	1	

DLM3

ACT 2/1200XL, ACT 3, 3200DX, 42MX, Axcelerator



Function

Data Latch with 4-input Multiplexed Data

Truth Table

S1	S0	G	Q _{n+1}
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

Input

D0, D1, D2, D3, S0, S1, G

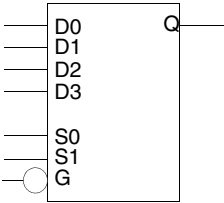
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DLM3A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, Axcelerator



Function

Data Latch with 4-input Multiplexed Data, and active low Clock

Truth Table

S1	S0	G	Q _{n+1}
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

Input

D0, D1, D2, D3, S0, S1, G

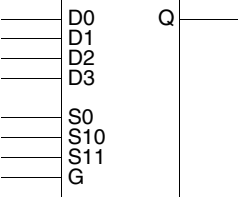
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

DLM4

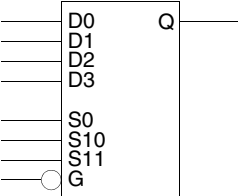
ACT 2/1200XL, ACT 3, 3200DX, 42MX, Axcelerator

		Function Data Latch with 4-input Multiplexed Data		
Input D0, D1, D2, D3, S0, S10, S11, G		Output Q		
Truth Table				
S10	S11	S0	G	Q_{n+1}
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM4A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, Axcelerator



Input D0, D1, D2, D3, S0, S10, S11, G	Output Q
---	--------------------

Function
Data Latch with 4-input Multiplexed Data and active low Clock

Truth Table

S10	S11	S0	G	Q _{n+1}
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM8A

ACT 3

D0

D1

D2

D3

S00

S01

S10

S11

G

CLR

Q

Input

D0, D1, D2, D3, S00, S01, S10, S11, G, CLR

Output

Q

Function

D-Type Latch with 4-input Multiplexed Data and active low Clear

Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3
1	X	1	1	1	1	D3

Family	Modules	
	Seq	Comb
ACT 3	1	

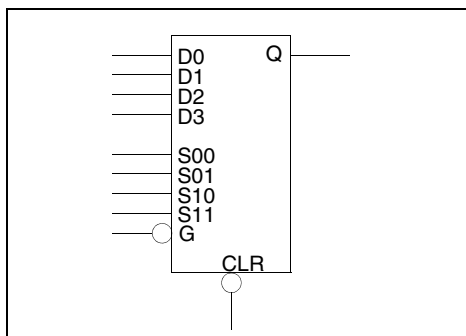
NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.

150

DLM8B

ACT 3



Input
D0, D1, D2, D3, S00,
S01, S10, S11, G, CLR

Output
Q

Function

D-Type Latch with 4-input Multiplexed Data and active low Clear and Clock

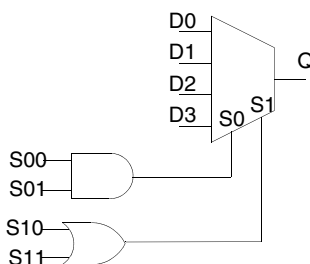
Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	1	Q
1	0	0	0	X	0	D0
1	0	0	X	0	0	D0
1	0	0	1	1	0	D1
1	1	X	0	X	0	D2
1	X	1	0	X	0	D2
1	1	X	X	0	0	D2
1	X	1	X	0	0	D2
1	1	X	1	1	0	D3
1	X	1	1	1	0	D3

Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1: The DLM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DLMA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator

Function

Data Latch with 2-input Multiplexed Data and active low Clock

Truth Table

S	G	Q _{n+1}
X	1	Q
0	0	A
1	0	B

Input
A, B, G, S

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLME1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator

Function

2-bit Data Latch with Multiplexed Data and Enable and active low Clock and Enable

Truth Table

E	S	G	Q _{n+1}
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

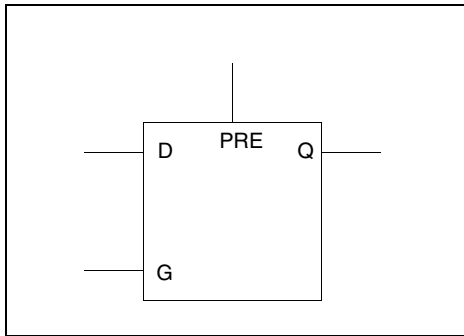
Input
A, B, E, G, S

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLP1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Data Latch with active high Preset and Clock

Truth Table

PRE	G	Q_{n+1}
1	X	1
0	0	Q
0	1	D

Input

D, G, PRE

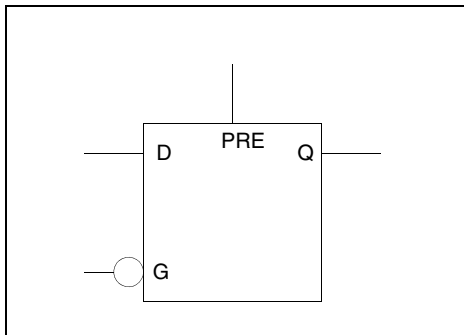
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Data Latch with active high Preset and active low Clock

Truth Table

PRE	G	Q_{n+1}
1	X	1
0	1	Q
0	0	D

Input

D, G, PRE

Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic symbol for DLP1B: A square block with inputs D, PRE (active low), and G. The output is Q.

Function

Data Latch with active low Preset and active high Clock

Truth Table

PRE	G	Q _{n+1}
0	X	1
1	0	Q
1	1	D

Input

D, G, PRE

Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic symbol for DLP1C: A square block with inputs D, PRE (active low), and G (active low). The output is Q.

Function

Data Latch with active low Preset and Clock

Truth Table

PRE	G	Q _{n+1}
0	X	1
1	1	Q
1	0	D

Input

D, G, PRE

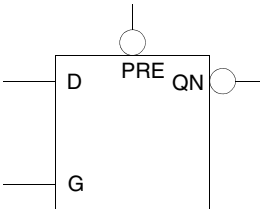
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Function

Data Latch with active low Preset and Output, and active high Clock

Truth Table

PRE	G	QN _{n+1}
0	X	0
1	0	QN
1	1	!D

Input

D, G, PRE

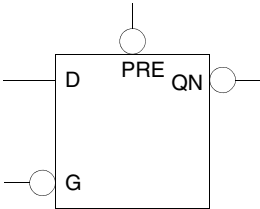
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1

DLP1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, Axcelerator



Function

Data Latch with active low Preset, Clock, and Output

Truth Table

PRE	G	Q _{n+1}
0	X	0
1	0	!D
1	1	QN

Input

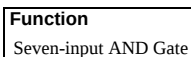
D, G, PRE

Output

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

3200DX, 42MX

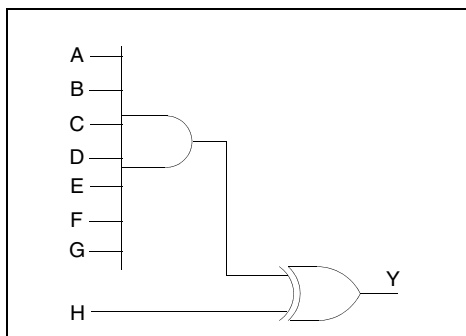


A through G	Y
All inputs = 1	1
Any input = 0	0

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXAX7

3200DX, 42MX

**Function**

Eight-input AND/Exclusive-OR Gate

Truth Table

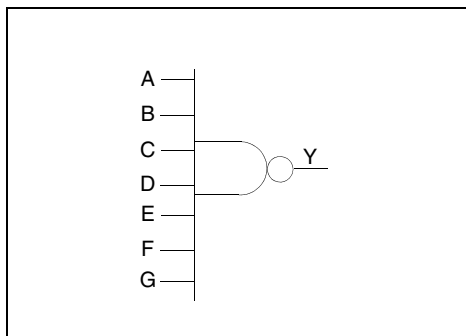
A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

Input A, B, C, D, E, F, G, H	Output Y
--	--------------------

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXNAND7

3200DX, 42MX

**Function**

Seven-input NAND Gate

Truth Table

A through G	Y
All inputs = 1	0
Any input = 0	1

Input A, B, C, D, E, F, G	Output Y
-------------------------------------	--------------------

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

FA1

ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

A

B

Cl

CO

S

2*

Input

A, B, Cl

Output

CO, S

Function

1 bit adder with active high I/Os

Truth Table

A	B	Cl	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		3
54SX, 54SX-A, 54SX-S, eX		2

* A 2 on the symbol implies 2 logic module delays only in ACT 1 and 40MX.

FA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

A

B

Cl

CO

S

2*

Input

A, B, Cl

Output

CO, S

Function

1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

Truth Table

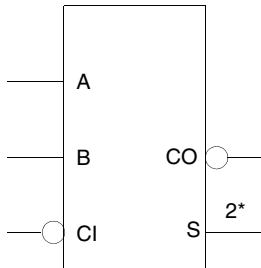
A	B	Cl	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX and 54SXA.

FA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

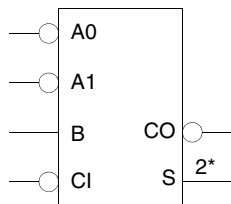
		Function 1-bit Adder with active low Carry In and Carry Out Truth Table<table><tr><th>A</th><th>B</th><th>CI</th><th>CO</th><th>S</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr></table>	A	B	CI	CO	S	0	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	1	1	1	1	0	0	1
A	B	CI	CO	S																																						
0	0	0	1	1																																						
0	0	1	1	0																																						
0	1	0	0	0																																						
0	1	1	1	1																																						
1	0	0	0	0																																						
1	0	1	1	1																																						
1	1	0	0	1																																						
Input A, B, CI	Output CO, S																																									

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX and 54SXA.

FA2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input

A0, A1, B, CI

Output

CO, S

Family	Modules	
	Seq	Comb
All		2

Function

1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

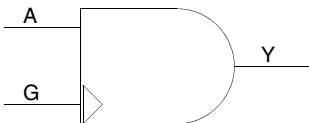
Truth Table ¹

A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1

* A 2 on the symbol implies 2 logic module delays in all families.

GAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input AND Clock Net

Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

Input

Input
A, G

Output

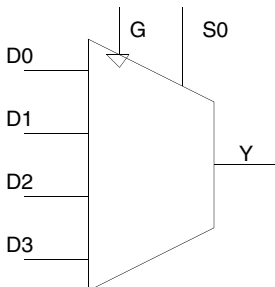
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GMX4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-to-1 Mux Clock Net

Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Input

D0, D1, D2, D3, S0, G

Output

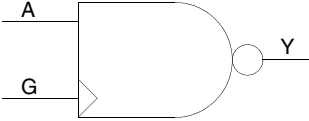
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GNAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input NAND Clock Net

Truth Table

A	G	Y
X	0	1
0	X	1
1	1	0

Input

A, G

Output

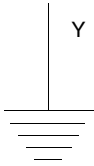
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GND

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Ground

Input

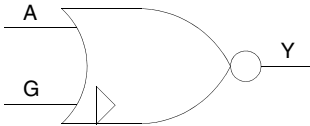
Output

Y

NOTE: Ground does not use any modules.

GNOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input NOR Clock Net

Truth Table

A	G	Y
0	0	1
X	1	0
1	X	0

Input

A, G

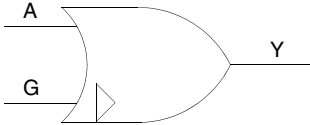
Output

Y

Family	Modules	
	Seq	Comb
All		1

GOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input OR Clock Net

Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

Input

A, G

Output

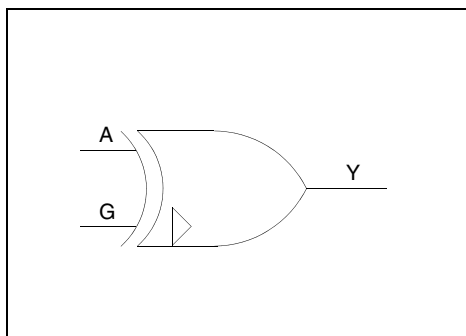
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GXOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input XOR Clock Net

Truth Table

A	G	Y
0	0	0
0	1	1
1	0	1
1	1	0

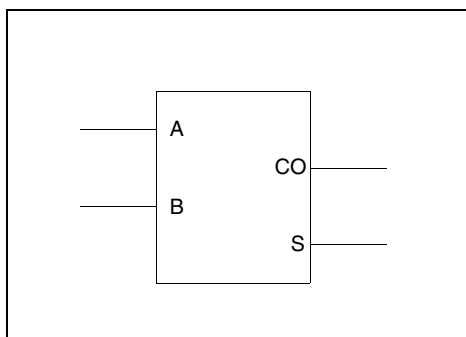
Input
A, G**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

HA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Half Adder

Truth Table

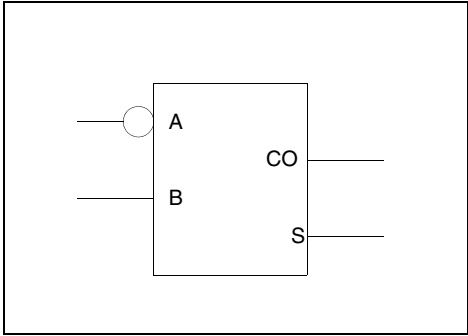
A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Input
A, B**Output**
CO, S

Family	Modules	
	Seq	Comb
All		2

HA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B

Output
CO, S

Function

Half-Adder with active low A-Input

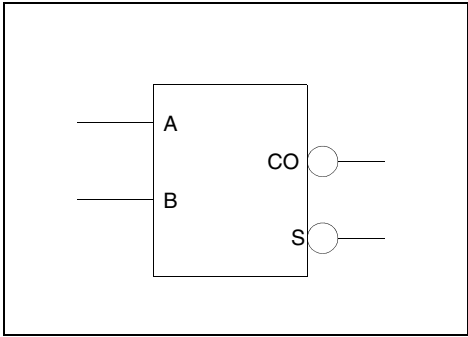
Truth Table

A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

Family	Modules	
	Seq	Comb
All		2

HA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B

Output
CO, S

Function

Half-Adder with active low Carry Out and Sum

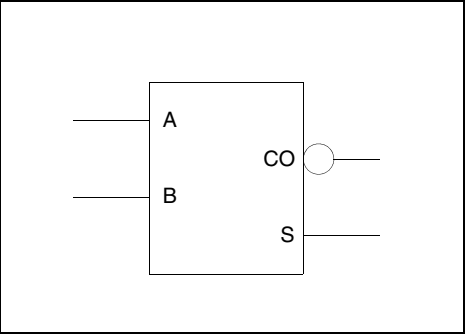
Truth Table

A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

Family	Modules	
	Seq	Comb
All		2

HA1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Half-Adder with active low Carry Out

Truth Table

A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

Input

A, B

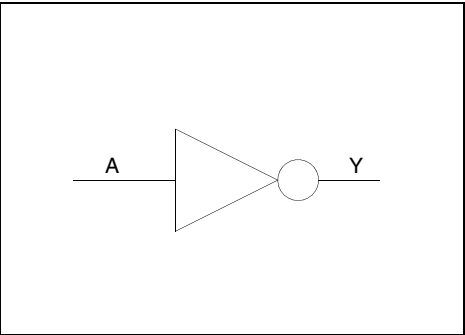
Output

CO, S

Family	Modules	
	Seq	Comb
All		2

INV

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Inverter with active low Output

Truth Table

A	Y
0	1
1	0

Input

A

Output

Y

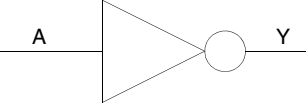
Family	Modules	
	Seq	Comb
All		1

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INVD

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Inverter with active low Output
NOTE: The Combiner will not remove this macro

Truth Table

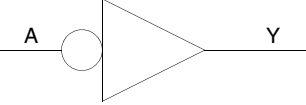
A	Y
0	1
1	0

Input A	Output Y
------------	-------------

Family	Modules	
	Seq	Comb
All		1

INVA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Inverter with active low Input

Truth Table

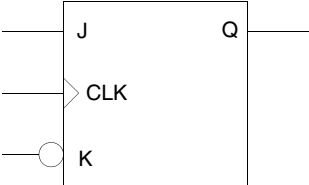
A	Y
0	1
1	0

Input A	Output Y
------------	-------------

Family	Modules	
	Seq	Comb
All		1

JKF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low K-Input

Truth Table

J	K	CLK	Q _{n+1}
0	0	↑	0
0	1	↑	Q
1	0	↑	!Q
1	1	↑	1

Input

J, K, CLK

Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1
Others	1	

JKF1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram of JKF1B JK Flip-Flop. Inputs: J, K, CLK (active low). Output: Q.

Function

JK Flip-Flop with active low Clock and K-Input

Truth Table

J	K	CLK	Q_{n+1}
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

Input

J, K, CLK

Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1
Others	1	

JKF2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram of JKF2A JK Flip-Flop. Inputs: J, K, CLR (active low), CLK (active low). Output: Q.

Function

JK Flip-Flop with active low Clear and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

Input

CLR, J, K, CLK

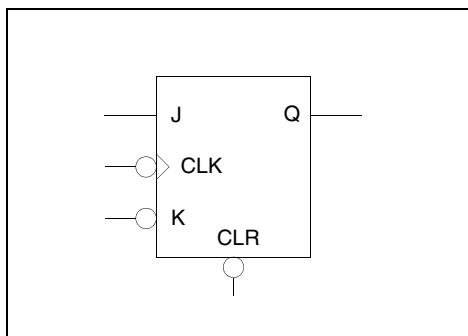
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1
Others	1	

JKF2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
CLR, J, K, CLK

Output
Q

Function

JK Flip-Flop with active low Clear, Clock, and K-Input

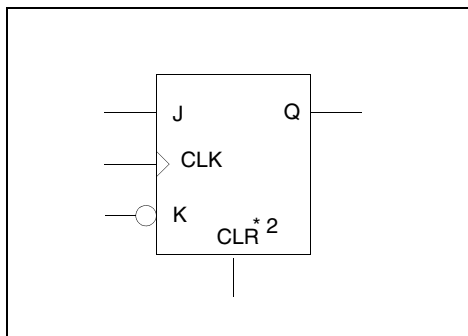
Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1
Others	1	

JKF2C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Input
CLR, J, K, CLK

Output
Q

Function

JK Flip-Flop with active high Clear and active low K-Input

Truth Table

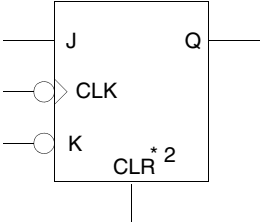
CLR	J	K	CLK	Q_{n+1}
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

JKF2D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

JK Flip-Flop with active high Clear and active low Clock and K-Input

Truth Table

CLR	J	K	CLK	Q _{n+1}
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Input

CLR, J, K, CLK

Output

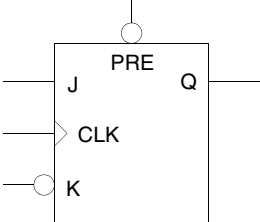
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

JKF3A

ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Preset and K-Input

Truth Table

PRE	J	K	CLK	Q _{n+1}
0	X	X	X	1
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

Input

J, K, PRE, CLK

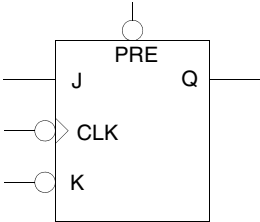
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

JKF3B

ACT 1, 40MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Preset, Clock, and K-Input

Truth Table

PRE	J	K	CLK	Q _{n+1}
0	X	X	X	1
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Input

J, K, PRE, CLK

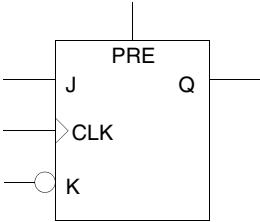
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

JKF3C

ACT 1, 40MX



Function

JK Flip-Flop with active high Preset and active low K-Input

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Input

J, K, PRE, CLK

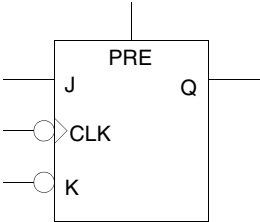
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

JKF3D

ACT 1, 40MX



Function
JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

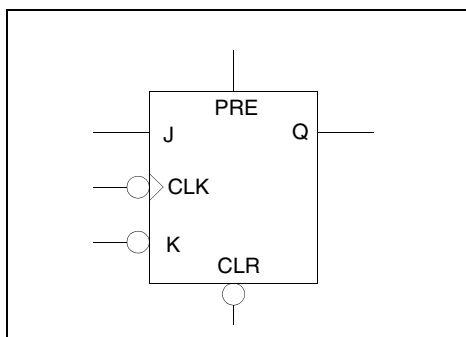
Input
J, K, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

JKF4B

ACT 1, 40MX



Input
CLR, J, K, PRE, CLK

Output
Q

Function

JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

Truth Table

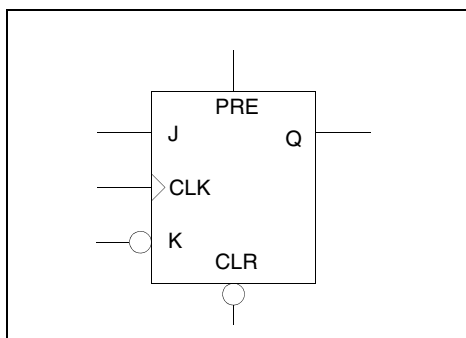
CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

Your design should not allow both PRE and CLR to be asserted at the same time.

JKFPC

ACT 1, 40MX



Input
CLR, J, K, PRE, CLK

Output
Q

Function

JK Flip-Flop with active high Preset, and active low Clear and K- Input

Truth Table

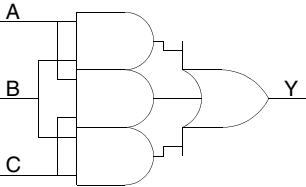
CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

MAJ3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input majority function

Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

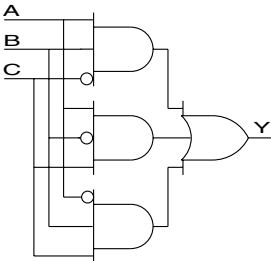
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

MAJ3X

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
2 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

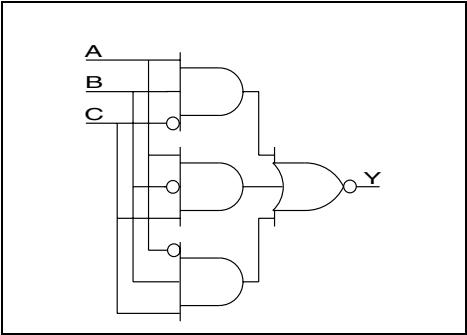
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

MAJ3XI

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input A, B, C	Output Y
-------------------------	--------------------

Function
2 of 3 function with active low output

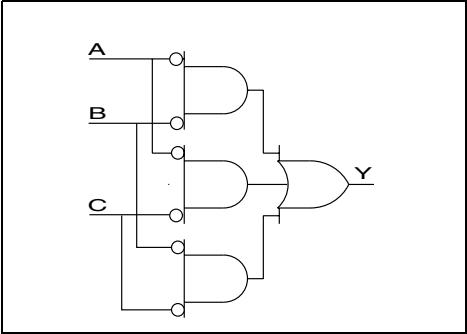
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

MIN3

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input A, B, C	Output Y
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Function
3-Input minority function

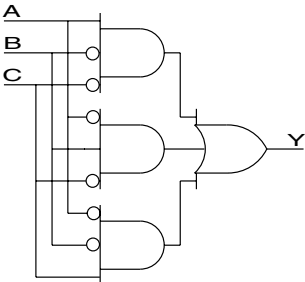
Truth Table

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

MIN3X

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

1 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Input

A, B, C

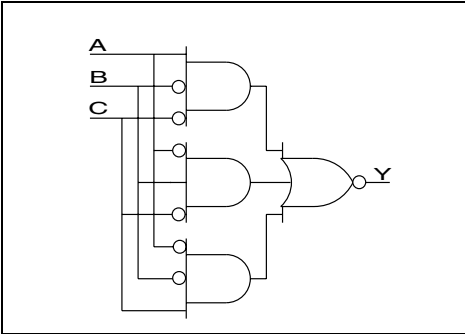
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

MIN3XI

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input A, B, C	Output Y
-------------------------	--------------------

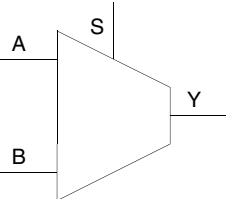
Function
1 of 3 function with active low output

Truth Table			
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

MX2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
2 to 1 Multiplexer

Truth Table

S	Y
0	A
1	B

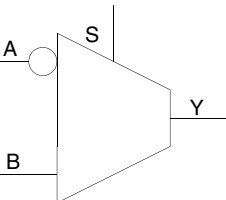
Input
A, B, S

Output
Y

Family	Modules	
	Seq	Comb
All		1

MX2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
2 to 1 Multiplexer with active low A-Input

Truth Table

S	Y
0	!A
1	B

Input
A, B, S

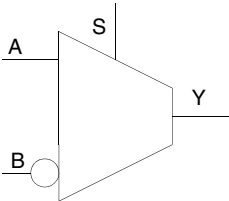
Output
Y

Family	Modules	
	Seq	Comb
All		1

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MX2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer with active low B-Input

Truth Table

S	Y
0	A
1	$\overline{B}$

Input

A, B, S

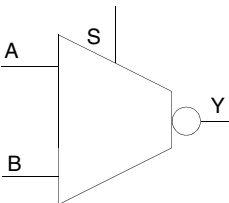
Output

Y

Family	Modules	
	Seq	Comb
All		1

MX2C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer with active low Output

Truth Table

S	Y
0	$\overline{A}$
1	$\overline{B}$

Input

A, B, S

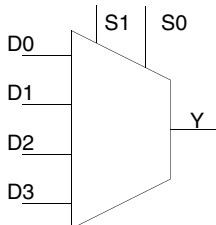
Output

Y

Family	Modules	
	Seq	Comb
All		1

MX4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

4 to 1 Multiplexer

Truth Table

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Input

D0, S0, S1, D1, D2, D3

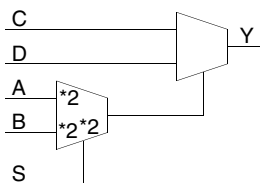
Output

Y

Family	Modules	
	Seq	Comb
All		1

MXC1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

Carry select multiplexer, used in adders

Truth Table

A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

Input

S, A, B, C, D

Output

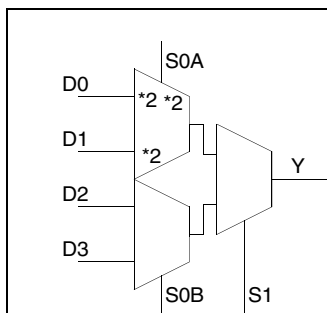
Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

MXT

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

Multiplexer with separate select lines

Truth Table

SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

Input

D0, D1, D2, D3, S0A, S0B, S1

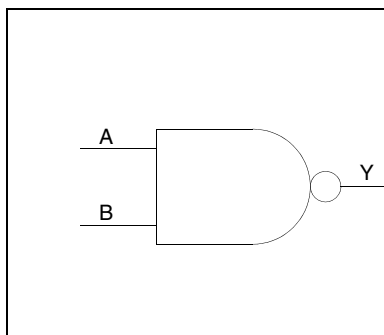
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

NAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input NAND

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Input

A, B

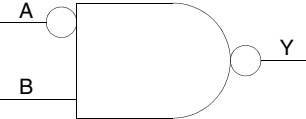
Output

Y

Family	Modules	
	Seq	Comb
All		1

NAND2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input NAND with active low A-Input

Truth Table

A	B	Y
X	0	1
0	1	0
1	X	1

Input

A, B

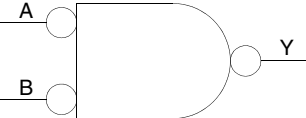
Output

Y

Family	Modules	
	Seq	Comb
All		1

NAND2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input NAND with active low Inputs

Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

Input

A, B

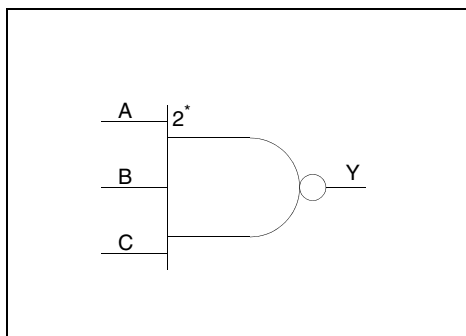
Output

Y

Family	Modules	
	Seq	Comb
All		1

NAND3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input NAND

Truth Table

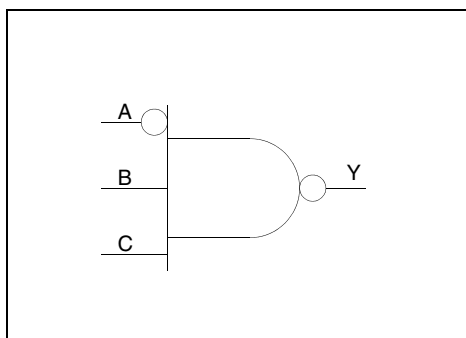
A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NAND3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input NAND with active low A-Input

Truth Table

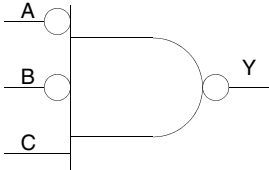
A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NAND3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input NAND with active low A- and B-Inputs

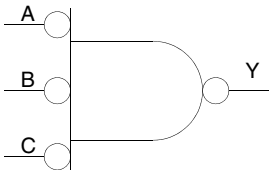
Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

Family	Modules	
	Seq	Comb
All		1

NAND3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C

Output
Y

Function

3-Input NAND with active low Inputs

Truth Table

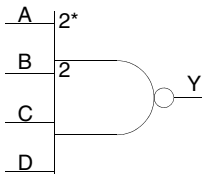
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Family	Modules	
	Seq	Comb
All		1

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NAND4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

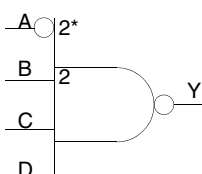
		Function 4-Input NAND																														
		Truth Table																														
		<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td></tr><tr><td>X</td><td>X</td><td>0</td><td>X</td><td>1</td></tr><tr><td>X</td><td>0</td><td>X</td><td>X</td><td>1</td></tr><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	D	Y	X	X	X	0	1	X	X	0	X	1	X	0	X	X	1	0	X	X	X	1	1	1	1	1	0
A	B	C	D	Y																												
X	X	X	0	1																												
X	X	0	X	1																												
X	0	X	X	1																												
0	X	X	X	1																												
1	1	1	1	0																												
Input A, B, C, D	Output Y																															

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except in 54SX, 54SX-A, 54SX-S, and eX.

NAND4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

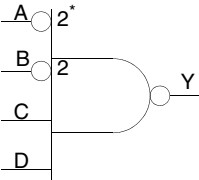
		Function 4-Input NAND with active low A-Input																														
		Truth Table																														
		<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td></tr><tr><td>X</td><td>X</td><td>0</td><td>X</td><td>1</td></tr><tr><td>X</td><td>0</td><td>X</td><td>X</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>X</td><td>X</td><td>X</td><td>1</td></tr></table>	A	B	C	D	Y	X	X	X	0	1	X	X	0	X	1	X	0	X	X	1	0	1	1	1	0	1	X	X	X	1
A	B	C	D	Y																												
X	X	X	0	1																												
X	X	0	X	1																												
X	0	X	X	1																												
0	1	1	1	0																												
1	X	X	X	1																												
Input A, B, C, D	Output Y																															

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NAND4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NAND with active low A- and B-Inputs

Truth Table

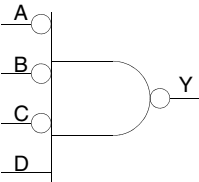
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NAND4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NAND with active low A-, B- and C-Inputs

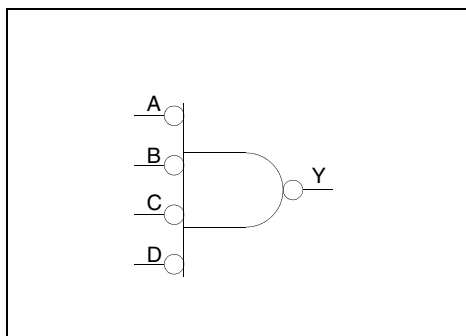
Truth Table

A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

NAND4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NAND with active low Inputs

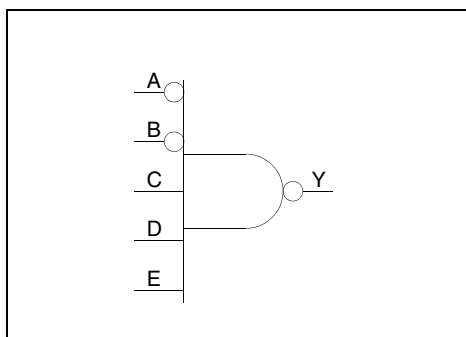
Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

NAND5B

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-input NAND with active low A- and B-inputs

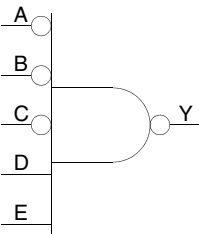
Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

NAND5C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input NAND with active low A-, B- and C-Inputs

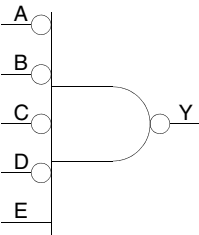
Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

NAND5D

Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input NAND with active low A-, B-, C-, and D-Inputs

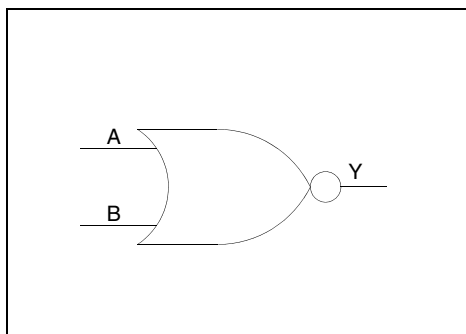
Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	1	X	1
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1
0	0	0	0	1	0

Family	Modules	
	Seq	Comb
All listed		1

NOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input NOR

Truth Table

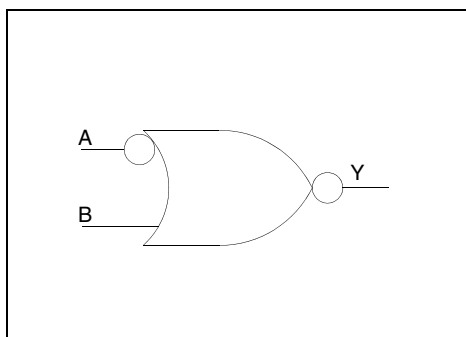
A	B	Y
0	0	1
X	1	0
1	X	0

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input NOR with active low A-Input

Truth Table

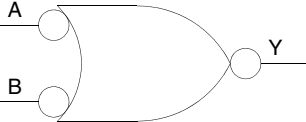
A	B	Y
0	X	0
1	0	1
X	1	0

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input NOR with active low Inputs

Truth Table

A	B	Y
X	0	0
0	X	0
1	1	1

Input
A, B

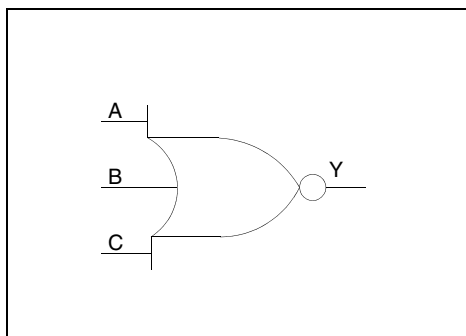
Output
Y

Family	Modules	
	Seq	Comb
All		1

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NOR3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input NOR

Truth Table

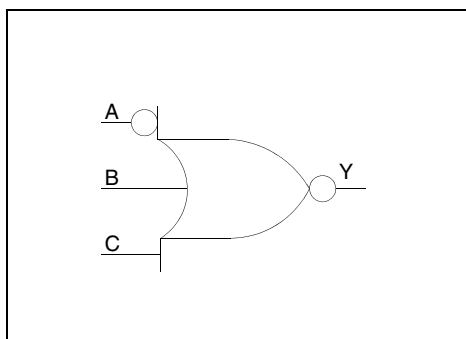
A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NOR3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input NOR with active low A-Input

Truth Table

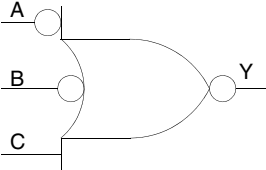
A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NOR3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input NOR with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

Input

A, B, C

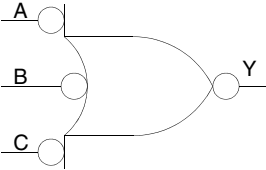
Output

Y

Family	Modules	
	Seq	Comb
All		1

NOR3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input NOR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input

A, B, C

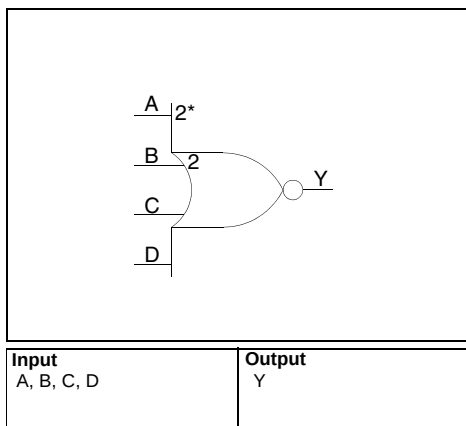
Output

Y

Family	Modules	
	Seq	Comb
All		1

NOR4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

4-Input NOR

Truth Table

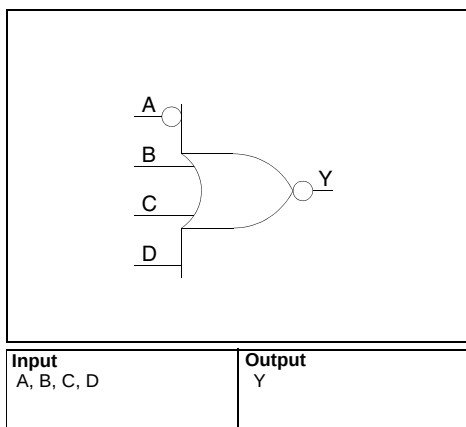
A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except 54SX, 54SX-A, 54SX-S, and eX.

NOR4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

4-Input NOR with active low A-Input

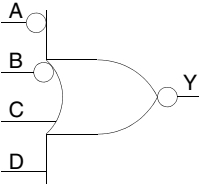
Truth Table

A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

Family	Modules	
	Seq	Comb
All		1

NOR4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NOR with active low A- and B-Inputs

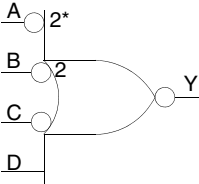
Truth Table

A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

Family	Modules	
	Seq	Comb
All		1

NOR4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NOR with active low A-, B- and C-Inputs

Truth Table

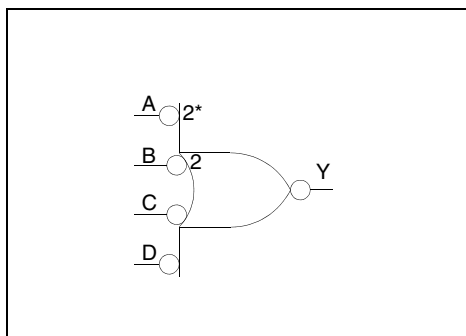
A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NOR4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D

Output
Y

Function

4-Input NOR with active low Inputs

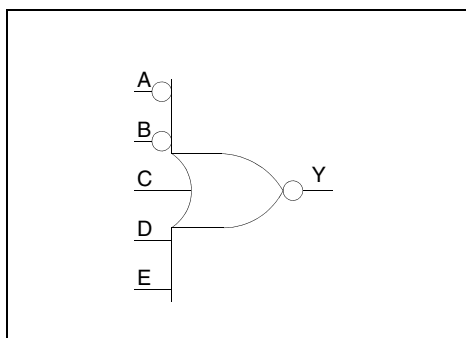
Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NOR5B

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input NOR with active low A- and B-Inputs

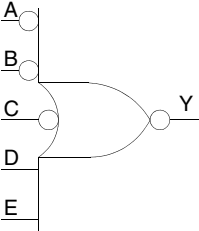
Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

NOR5C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input NOR with active low A-, B- and C-Inputs

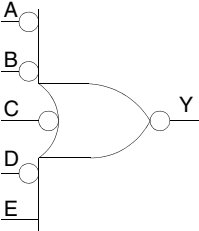
Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Family	Modules	
	Seq	Comb
All listed		1

NOR5D

Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input NOR with active low A-, B-, C-, and D-Inputs

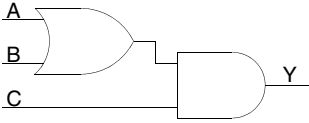
Truth Table

A	B	C	D	E	Y
X	X	X	X	1	0
X	X	X	0	X	0
X	X	0	X	X	0
X	0	X	X	X	0
0	X	X	X	X	0
1	1	1	1	0	1

Family	Modules	
	Seq	Comb
All listed		1

OA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3 Input OR-AND

Truth Table

A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Input

A, B, C

Output

Y

Family	Modules	
	Seq	Comb
All		1

OA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A((A)) --- OR1[OR]; B((B)) --- OR1; C((C)) --- OR1; OR1 --- AND1[AND]; C --- AND1; AND1 --- Y((Y))
```

Function
3 Input OR-AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

OA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

```
graph LR; A((A)) --- OR1[OR]; B((B)) --- OR1; C((C)) --- OR1; OR1 --- AND1[AND]; C --- AND1; AND1 --- Y((Y))
```

Function
3 Input OR-AND with active low C-Input

Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

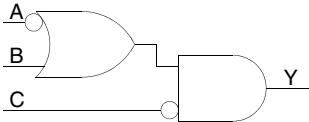
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

OA1C

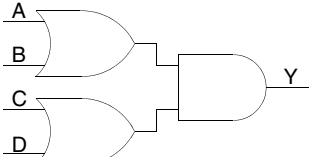
ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

		Function 3 Input OR-AND with active low A- and C-Inputs																				
Truth Table																						
<table><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr><tr><td>0</td><td>X</td><td>0</td><td>1</td></tr><tr><td>X</td><td>X</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>X</td><td>0</td></tr><tr><td>X</td><td>1</td><td>0</td><td>1</td></tr></table>		A	B	C	Y	0	X	0	1	X	X	1	0	1	0	X	0	X	1	0	1	
A	B	C	Y																			
0	X	0	1																			
X	X	1	0																			
1	0	X	0																			
X	1	0	1																			
Input A, B, C	Output Y																					

Family	Modules	
	Seq	Comb
All		1

OA2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

		Function 2-wide 4-Input OR-AND Truth Table<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>X</td><td>X</td><td>0</td></tr><tr><td>X</td><td>1</td><td>X</td><td>1</td><td>1</td></tr><tr><td>X</td><td>1</td><td>1</td><td>X</td><td>1</td></tr><tr><td>1</td><td>X</td><td>X</td><td>1</td><td>1</td></tr><tr><td>1</td><td>X</td><td>1</td><td>X</td><td>1</td></tr></table>	A	B	C	D	Y	X	X	0	0	0	0	0	X	X	0	X	1	X	1	1	X	1	1	X	1	1	X	X	1	1	1	X	1	X	1
A	B	C	D	Y																																	
X	X	0	0	0																																	
0	0	X	X	0																																	
X	1	X	1	1																																	
X	1	1	X	1																																	
1	X	X	1	1																																	
1	X	1	X	1																																	
Input A, B, C, D	Output Y																																				

Family	Modules	
	Seq	Comb
All		1

OA2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram for OA2A: A 4-input OR-AND gate. Inputs A, B, C, and D are connected to the OR input. The output of the OR gate is connected to the AND input. The output of the AND gate is Y.

Function
2 wide 4-Input OR-AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All		1

OA3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

Logic diagram for OA3: A 4-input OR-AND gate. Inputs A, B, C, and D are connected to the OR input. The output of the OR gate is connected to the AND input. The output of the AND gate is Y.

Function
4- Input OR-AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

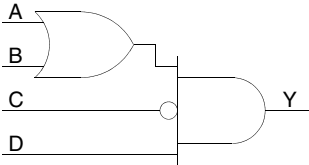
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All		1

OA3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input OR-AND with active low C-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

Input

A, B, C, D

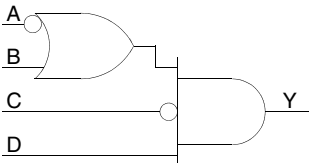
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input OR-AND with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

Input

A, B, C, D

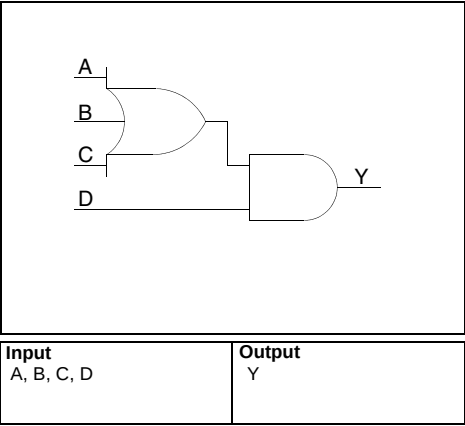
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA4

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



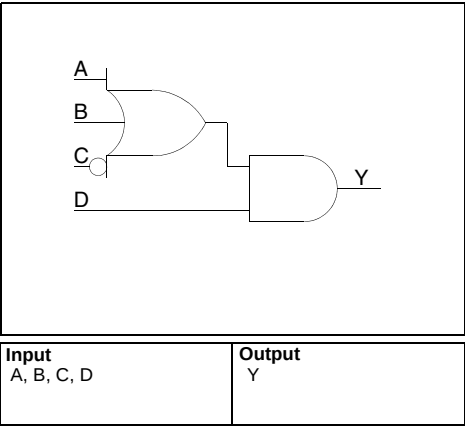
Function
4-Input OR-AND

Truth Table				
A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All listed		1

OA4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



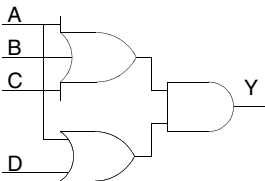
Function
4-Input OR-AND with active low C-Input

Truth Table				
A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

OA5

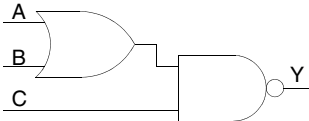
ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

		Function 4-Input complex OR-AND																														
		Truth Table																														
		<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>0</td><td>X</td><td>X</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td><td>0</td></tr><tr><td>X</td><td>X</td><td>1</td><td>1</td><td>1</td></tr><tr><td>X</td><td>1</td><td>X</td><td>1</td><td>1</td></tr><tr><td>1</td><td>X</td><td>X</td><td>X</td><td>1</td></tr></table>	A	B	C	D	Y	0	X	X	0	0	0	0	0	X	0	X	X	1	1	1	X	1	X	1	1	1	X	X	X	1
A	B	C	D	Y																												
0	X	X	0	0																												
0	0	0	X	0																												
X	X	1	1	1																												
X	1	X	1	1																												
1	X	X	X	1																												
Input A, B, C, D	Output Y																															

Family	Modules	
	Seq	Comb
All		1

OAI1

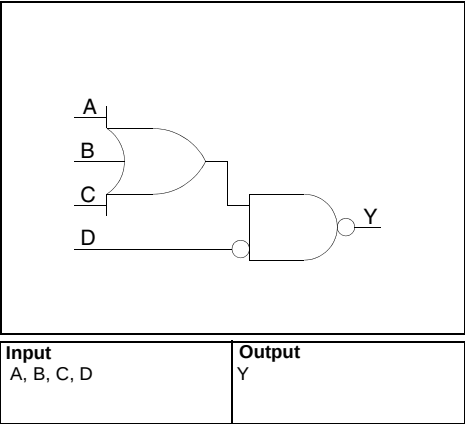
ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

		Function 3-Input OR-AND-INVERT																				
		Truth Table																				
		<table><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr><tr><td>X</td><td>X</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>X</td><td>1</td></tr><tr><td>X</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>X</td><td>1</td><td>0</td></tr></table>	A	B	C	Y	X	X	0	1	0	0	X	1	X	1	1	0	1	X	1	0
A	B	C	Y																			
X	X	0	1																			
0	0	X	1																			
X	1	1	0																			
1	X	1	0																			
Input A, B, C	Output Y																					

Family	Modules	
	Seq	Comb
All		1

OAI2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input OR-AND-INVERT with active low D-Input

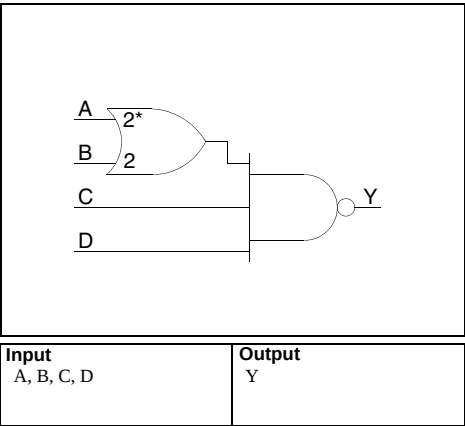
Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

OAI3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4 Input OR-AND-INVERT

Truth Table

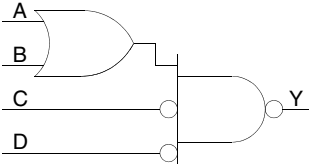
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 implies 2 logic module delays only for ACT 1 and 40MX.

OAI3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4 Input OR-AND-INVERT with active low C- and D-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input

A, B, C, D

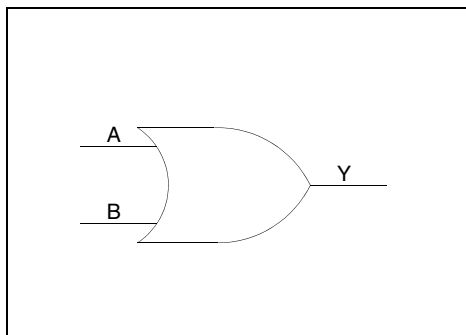
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input OR

Truth Table

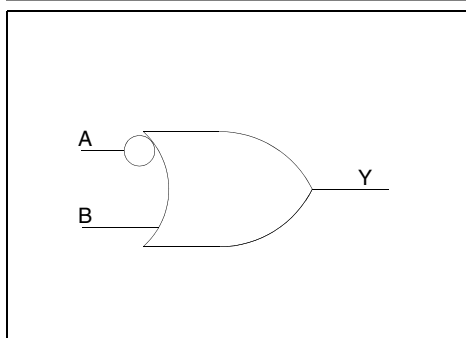
A	B	Y
0	0	0
X	1	1
1	X	1

Input
A, B**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

2-Input OR with active low A-Input

Truth Table

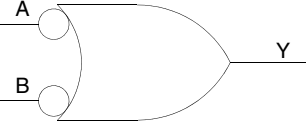
A	B	Y
0	X	1
1	0	0
X	1	1

Input
A, B**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

2-Input OR with active low Inputs

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Input

A, B

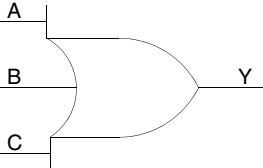
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input OR

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Input

A, B, C

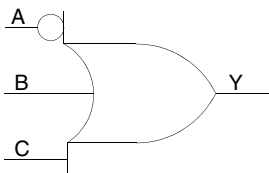
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input OR with active low A-Input

Truth Table

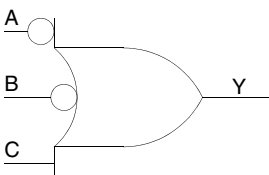
A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

3-Input OR with active low A- and B-Inputs

Truth Table

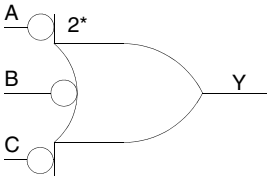
A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input
A, B, C

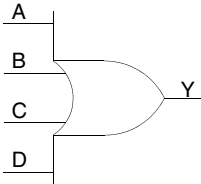
Output
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
4-Input OR

Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

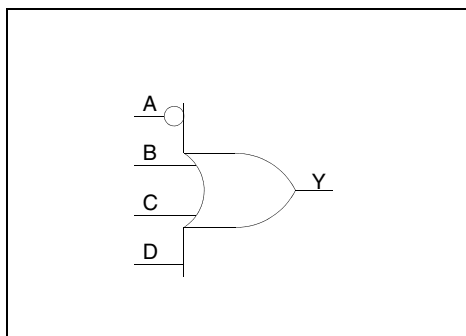
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All		1

OR4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

4-Input OR with active low A-Input

Truth Table

A	B	C	D	Y
0	X	X	X	1
1	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1

Input

A, B, C, D

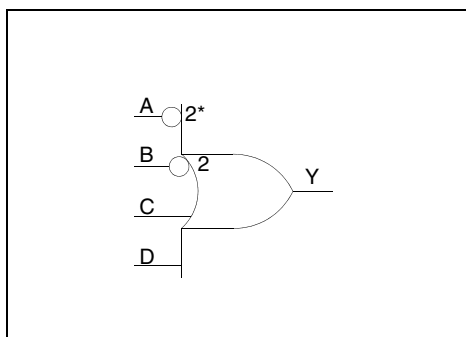
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

4-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

Input

A, B, C, D

Output

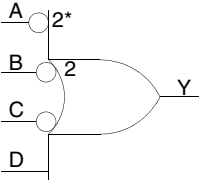
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

Input

A, B, C, D

Output

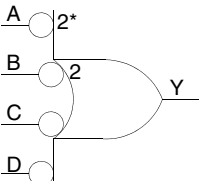
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

*A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

4-Input OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Input

A, B, C, D

Output

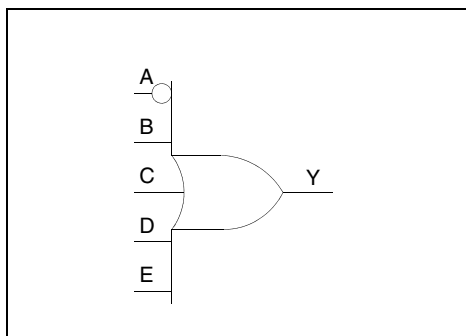
Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except for 54SX, 54SX-A, 54SX-S, eX.

OR5A

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input OR with active low A- Input

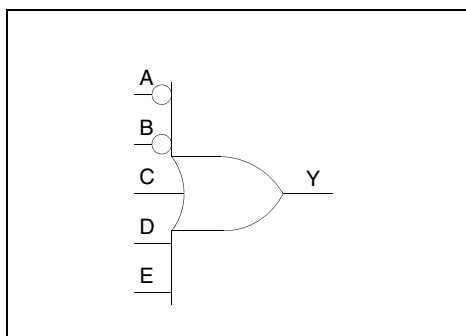
Truth Table

A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

OR5B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input OR with active low A- and B-Inputs

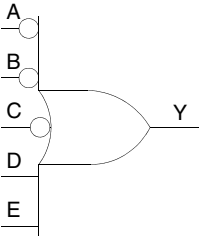
Truth Table

A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

OR5C

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Input
A, B, C, D, E

Output
Y

Function

5-Input OR with active low A-, B- and C-Inputs

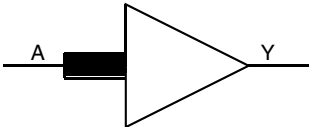
Truth Table

A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

QCLKINT

3200DX, 42MX, 54SX-A, 54SX-S



Input
A

Output
Y

Function

Internal Clock Interface

Truth Table

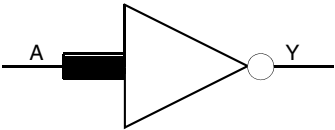
A	Y
0	0
1	1

NOTE: QCLKINT does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

QCLKINTI

54SX-A, 54SX-S



Function

Internal Clock Interface

Truth Table

A	Y
0	1
1	0

Input
A

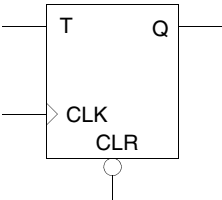
Output
Y

NOTE: QCLKINTI does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

TF1A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

T-Type Flip-Flop with active low Clear

Truth Table

CLR	T	CLK	Q _{n+1}
0	X	X	0
1	1	↑	!Q
1	0	↑	Q

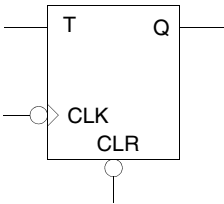
Input
CLR, T, CLK

Output
Q

Family	Modules	
	Seq	Comb
All listed	1	

TF1B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

T-Type Flip-Flop with active low Clear and Clock

Truth Table

CLR	T	CLK	Q _{n+1}
0	X	X	0
1	1	↓	!Q
1	0	↓	Q

Input

CLR, T, CLK

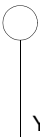
Output

Q

Family	Modules	
	Seq	Comb
All listed	1	

VCC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Power

Input

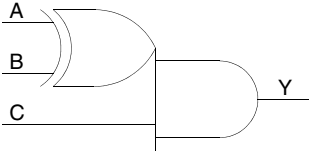
Output

Y

NOTE: VCC does not use any modules.

XA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input XOR-AND

Truth Table

A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

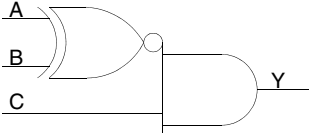
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

XA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input XNOR-AND

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

Input
A, B, C

Output
Y

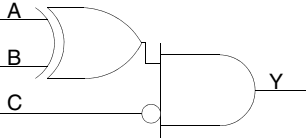
Family	Modules	
	Seq	Comb
All		1

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XA1B

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	X	0
1	0	0	1
0	1	0	1
1	1	X	0

Input

A, B, C

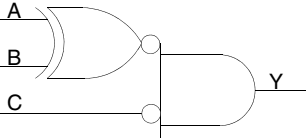
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

XA1C

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	0	1
1	0	X	0
0	1	X	0
1	1	0	1

Input

A, B, C

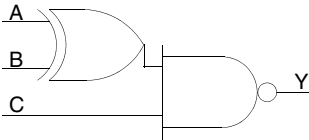
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

XAI1

54SX, 54SX-A, 54SX-S, eX, Accelerator



Function

3-Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
1	0	1	0
0	1	1	0
1	1	X	1

Input

A, B, C

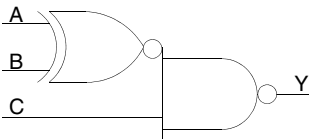
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

XAI1A

54SX, 54SX-A, 54SX-S, eX, Accelerator



Function

3-Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
1	0	X	1
0	1	X	1
1	1	1	0

Input

A, B, C

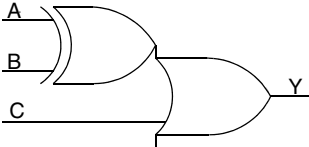
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

XO1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input XOR-OR

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

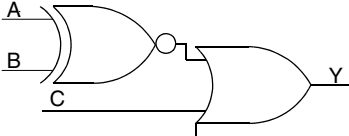
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

XO1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input XNOR-OR

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

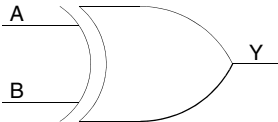
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

XOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
2-Input XOR

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

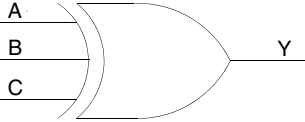
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

XOR3

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function
3-Input XOR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

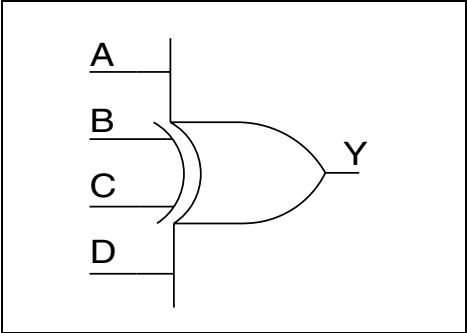
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

XOR4

Axcelerator



Function
4-Input Exclusive OR Gate

Truth Table

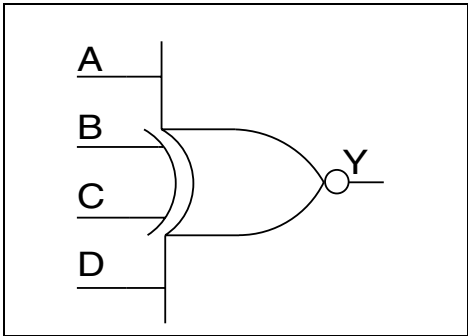
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		2

XNOR4

Axcelerator



Function
4-input Exclusive NOR gate

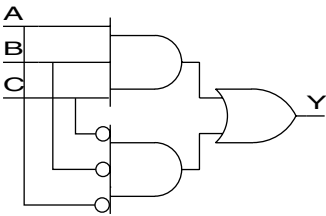
Truth Table				
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		2

ZOR3

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input function

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Input

A, B, C

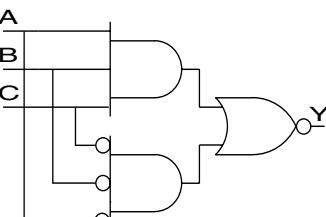
Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

ZOR3

54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

3-Input function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Input

A, B, C

Output

Y

Family	Modules	
	Seq	Comb
54SX, 54SX-A, 54SX-S, eX		1

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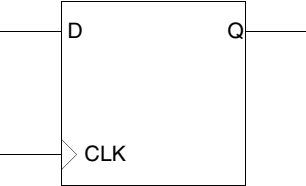
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CC-Module Flip Flops

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays*.)

DF1_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop

Truth Table

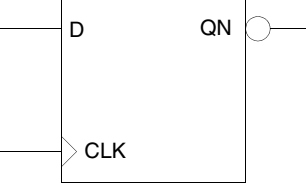
CLK	Q _{n+1}
↑	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
All		2

DF1A_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Output

Truth Table

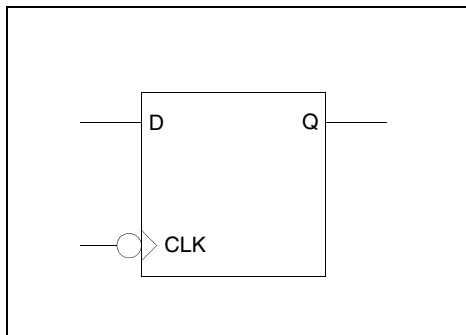
CLK	QN _{n+1}
↑	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DF1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop with active low Clock

Truth Table

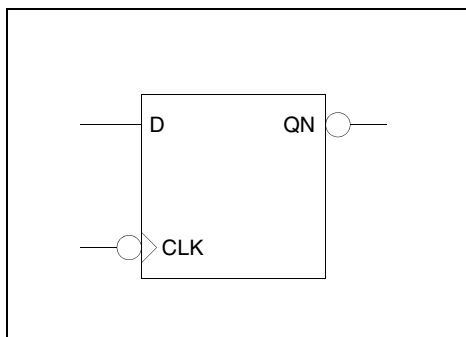
CLK	Q_{n+1}
↓	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	

DF1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

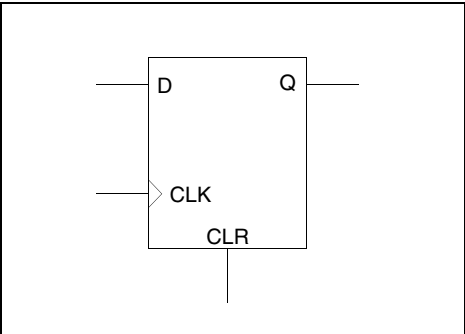
CLK	QN_{n+1}
↓	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2

DFC1_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active high Clear

Truth Table

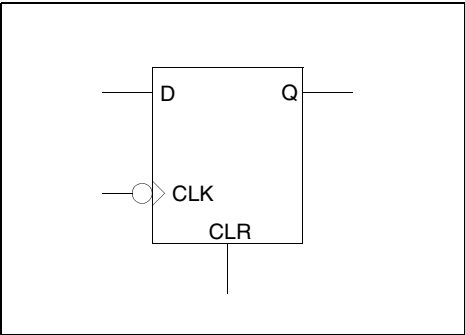
CLR	CLK	Q _{n+1}
1	X	0
0	↑	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2

DFC1A_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

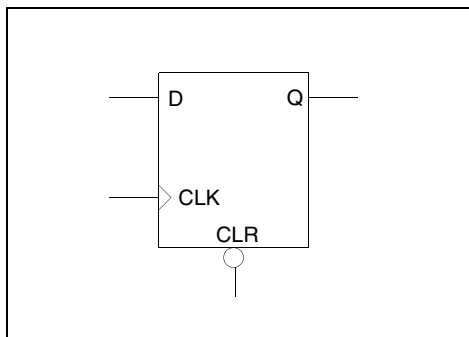
CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2

DFC1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop, with active low Clear

Truth Table

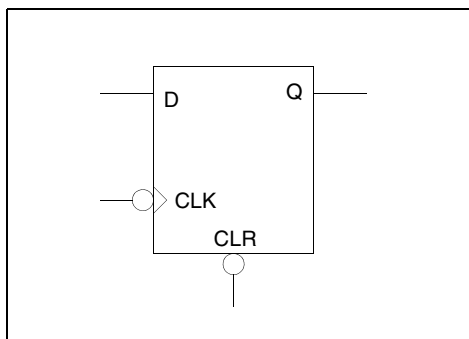
CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed		2

DFC1D_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop, with active low Clear and Clock

Truth Table

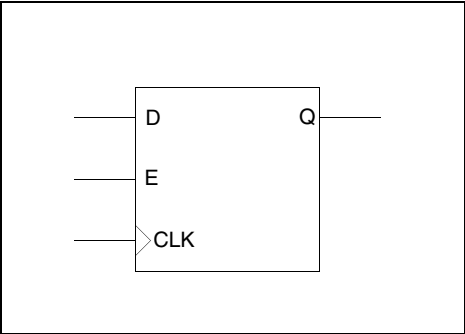
CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	

DFE_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with active high Enable

Truth Table

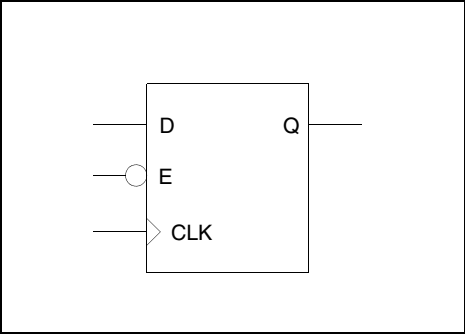
E	CLK	Q _{n+1}
0	X	Q
1	↑	D

Input D, E, CLK	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2

DFE1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function
D-Type Flip-Flop with active low Enable

Truth Table

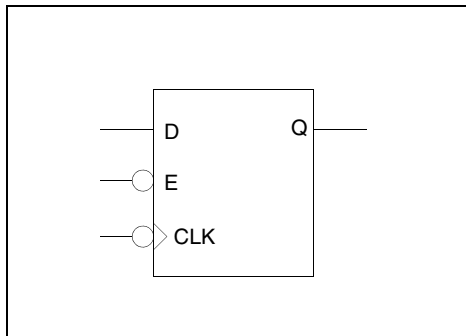
E	CLK	Q _{n+1}
1	X	Q
0	↑	D

Input D, E, CLK	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	

DFE1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop with active low Enable and Clock

Truth Table

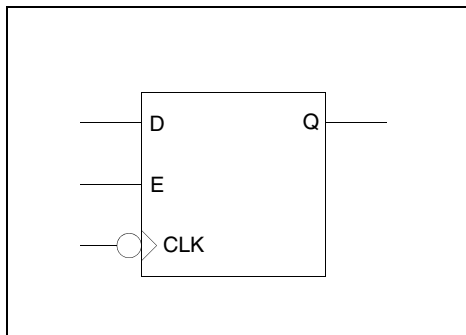
E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	

DFEA_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with Enable and active low Clock

Truth Table

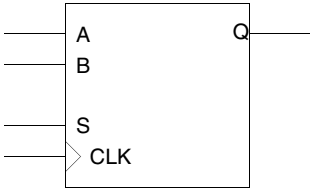
E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2

DFM_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Logic diagram of DFM_CC: A D-Type Flip-Flop with 2-input Multiplexed Data. Inputs A and B are multiplexed into the D input. Input S is the Set input. Input CLK is the clock. Output Q is the data output.

Function
D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

S	CLK	Q _{n+1}
0	↑	A
1	↑	B

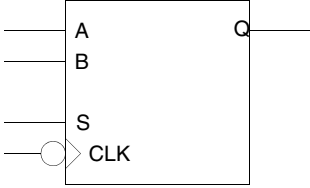
Input
A, B, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
All listed		2

DFMA_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Logic diagram of DFMA_CC: A D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock. Inputs A and B are multiplexed into the D input. Input S is the Set input. Input CLK is the active low clock. Output Q is the data output.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q _{n+1}
0	↓	A
1	↓	B

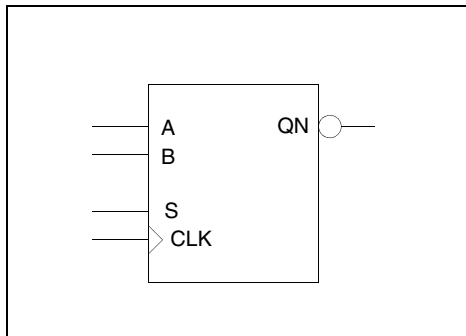
Input
A, B, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT3, 3200DX, 42MX		2

DFM1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

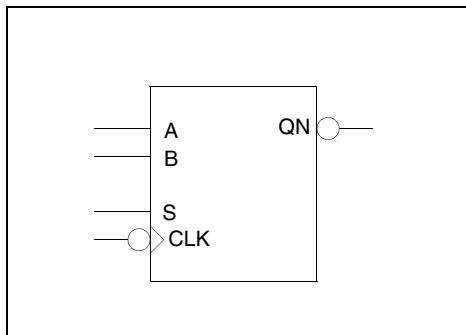
S	CLK	QN _{n+1}
0	↑	!A
1	↑	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DFM1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data and active low Clock and Output

Truth Table

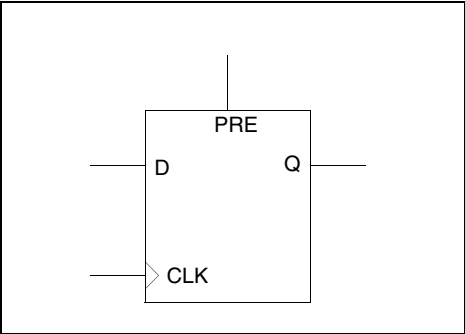
S	CLK	QN _{n+1}
0	↓	!A
1	↓	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DFP1_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function
D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↑	D

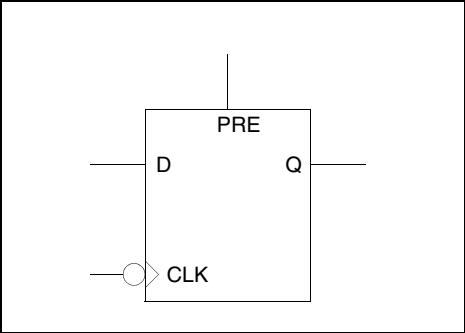
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

* Identical to macro DFP1.

DFP1A_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↓	D

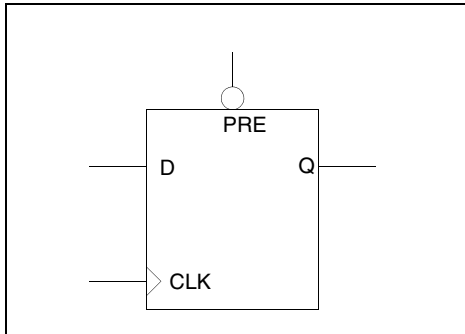
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

* Identical to macro DFP1A.

DFP1B_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

Input

D, PRE, CLK

Output

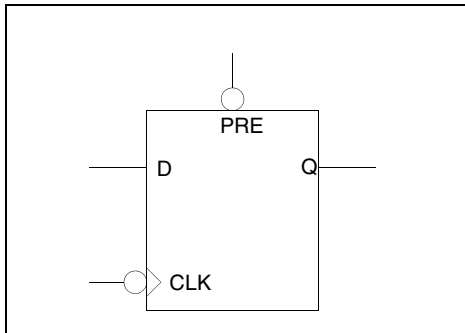
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1B.

DFP1D_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

Input

D, PRE, CLK

Output

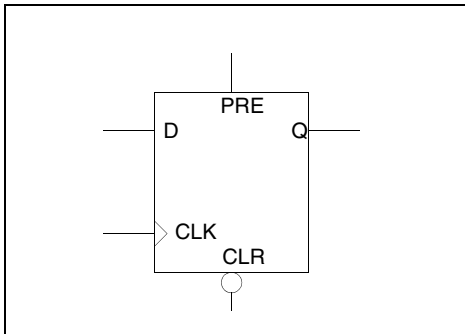
Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	

* Identical to macro DFP1D.

DFPC_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	1	X	1
1	0	↑	D

Input

CLR, D, PRE, CLK

Output

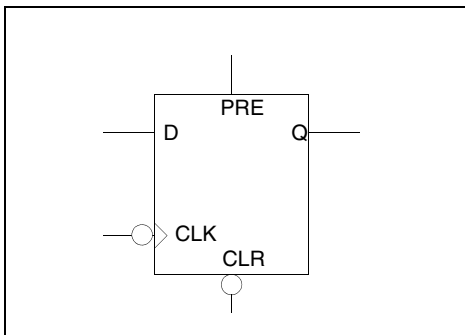
Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

* Identical to macro DFPC.

DFPCA_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

Input

CLR, D, PRE, CLK

Output

Q

Family	Modules	
	Seq	Comb
ACT 2/1200XL, ACT 3, 3200DX, 42MX		2
54SX, 54SX-A, 54SX-S, eX	1	1

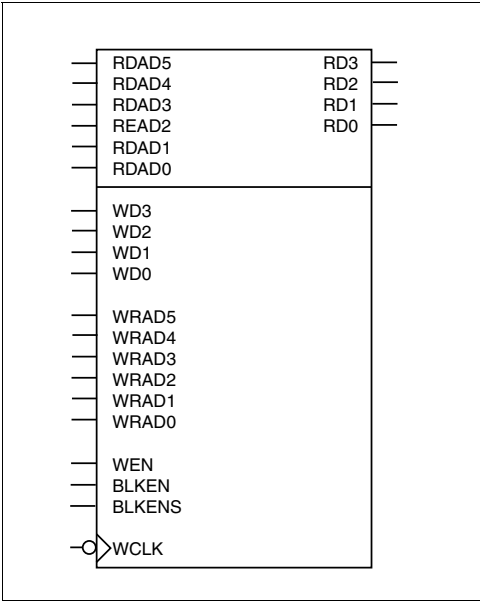
* Identical to Macro DFPCA.

** Your design should not allow both PRE and CLR to be asserted at the same time.

Memory Macros

RAM4FA

3200DX, 42MX



Function

64X4 dual-port RAM with falling Write clock and asynchronous Read

Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

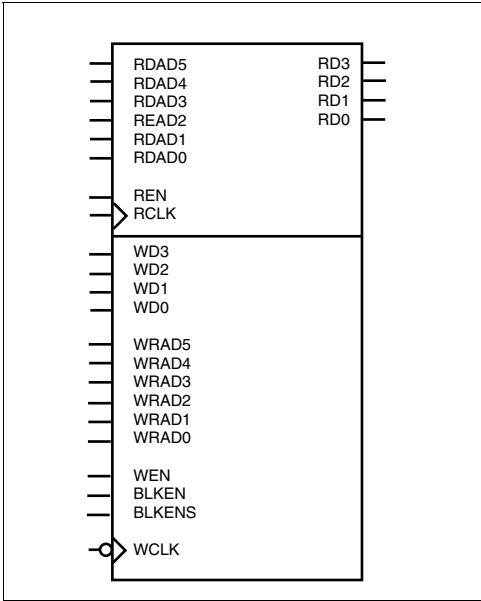
Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All listed	1

RAM4FR

3200DX, 42MX



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function
64X4 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

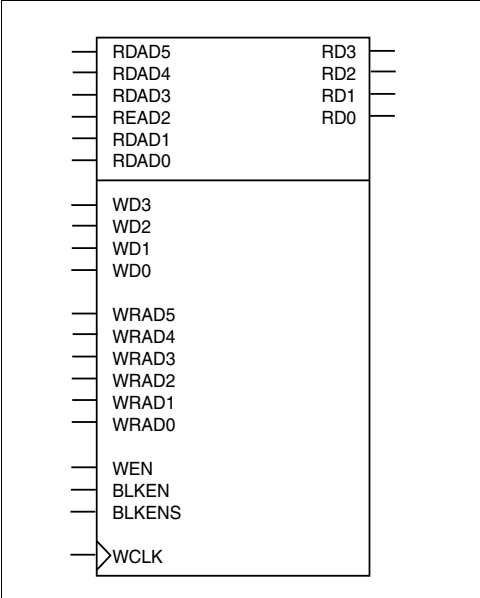
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM4RA

3200DX, 42MX



Function

64X4 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

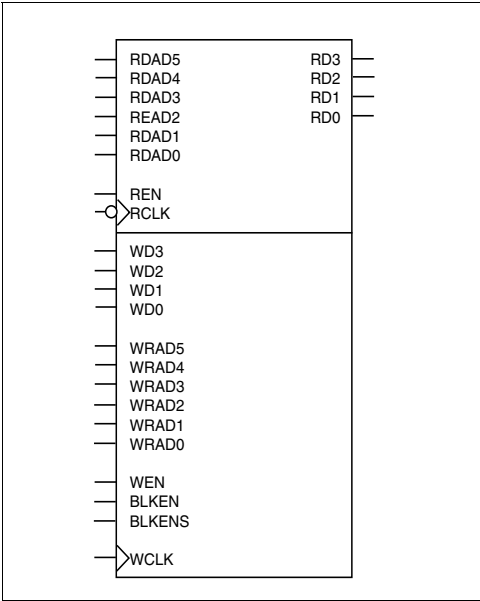
Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All listed	1

RAM4RF

3200DX, 42MX



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function
64X4 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

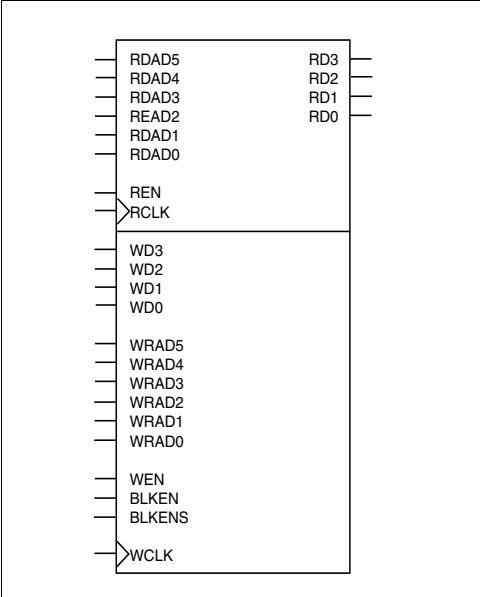
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM4RR

3200DX, 42MX



Input
RDAD5, RDAD4,
RDAD3, RDAD2,
RDAD1, RDAD0, REN,
RCLK, WD3, WD2, WD1,
WD0, WRAD5, WRAD4,
WRAD3, WRAD2,
WRAD1, WRAD0, WEN,
BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function
64X4 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM8FA

3200DX, 42MX

RDAD4

RDAD3

RDAD2

RDAD1

RDAD0

RD7

RD6

RD5

RD4

RD3

RD2

RD1

RD0

WD7

WD6

WD5

WD4

WD3

WD2

WD1

WD0

WRAD4

WRAD3

WRAD2

WRAD1

WRAD0

WEN

BLKEN

BLKENS

WCLK

Input

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1:

RDAD contents always appear at RD.

NOTE 2:

BLKENS must be driven by a GND or VCC macro.

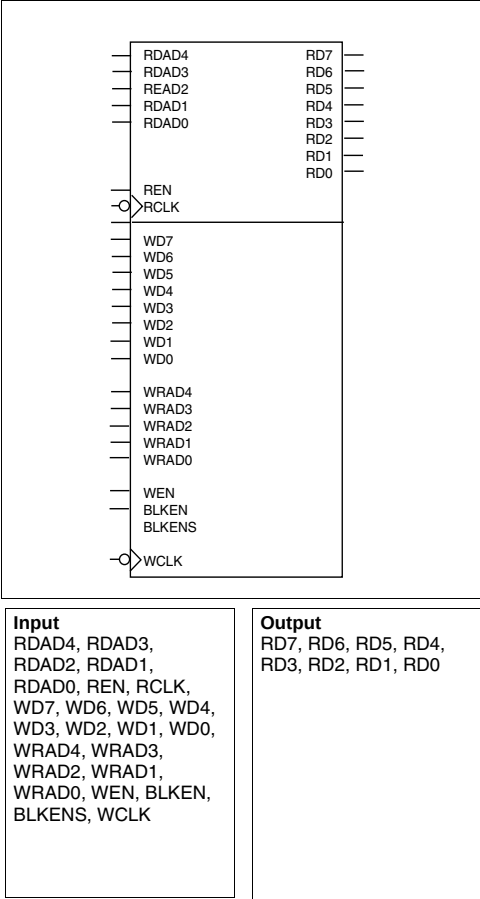
NOTE 3:

The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

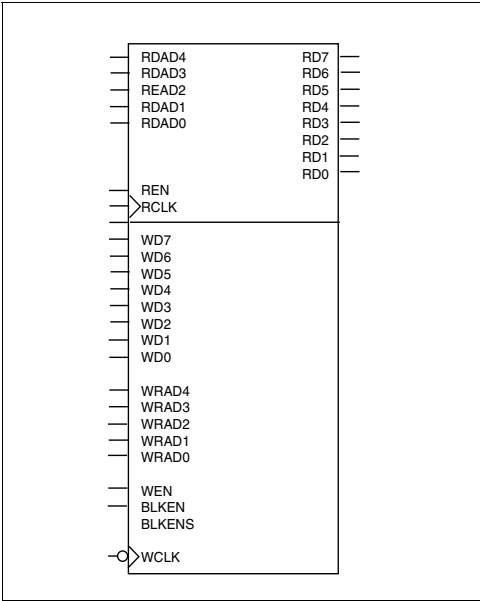
RAM8FF

3200DX, 42MX



RAM8FR

3200DX, 42MX



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function
32X8 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

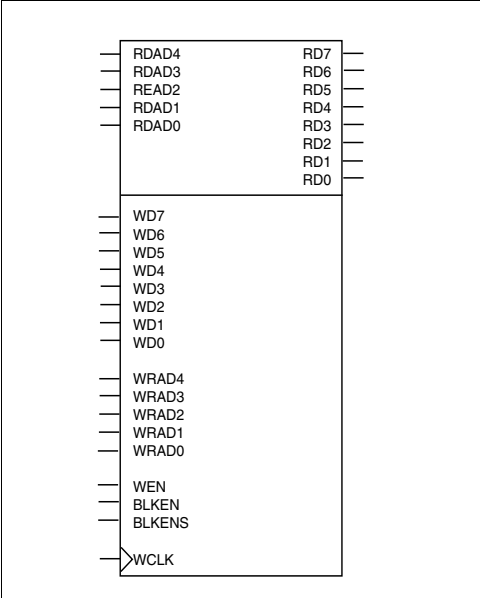
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM8RA

3200DX, 42MX



Function

32X8 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: RDAD contents always appear at RD.

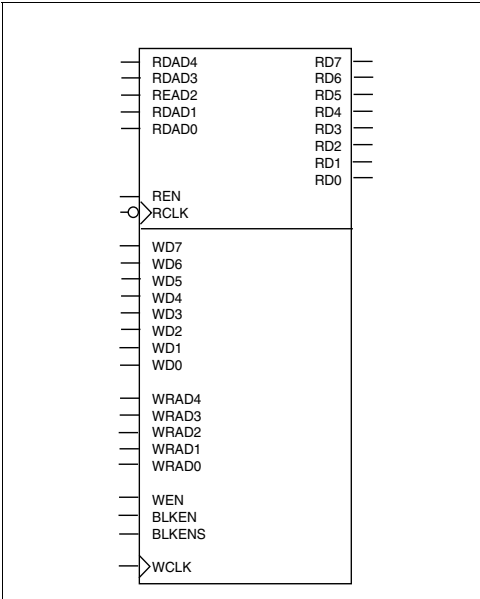
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM8RF

3200DX, 42MX



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function
32X8 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

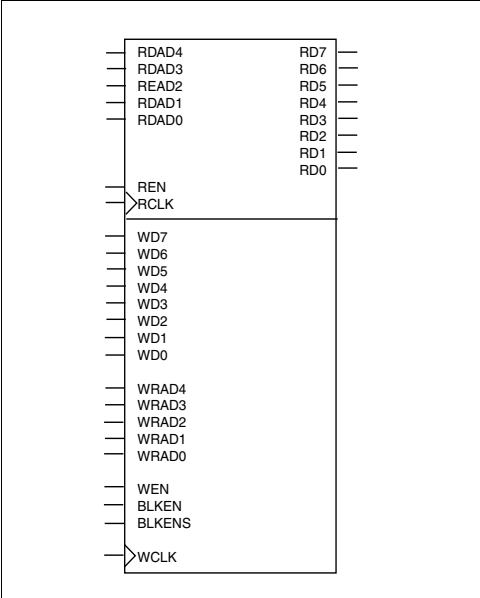
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

RAM8RR

3200DX, 42MX



Input
RDAD4, RDAD3,
RDAD2, RDAD1,
RDAD0, REN, RCLK,
WD7, WD6, WD5, WD4,
WD3, WD2, WD1, WD0,
WRAD4, WRAD3,
WRAD2, WRAD1,
WRAD0, WEN, BLKEN,
BLKENS, WCLK

Output
RD7, RD6, RD5, RD4,
RD3, RD2, RD1, RD0

Function
32X8 dual-port RAM with rising Write clock and rising Read clock

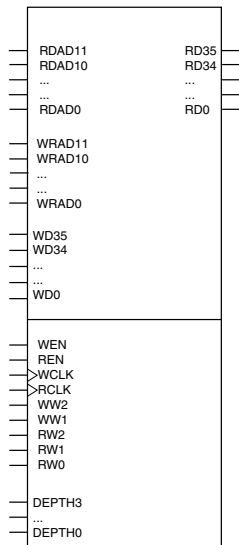
Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Family	Modules
	RAM
All listed	1



Input
RDAD11, ..., RDAD0
WRAD11, ..., WRAD0
WD35, ..., WD0,
WEN, REN, WCLK,
RCLK, WW2, WW1,
WW0, RW2, RW1, RW0,
DEPTH3, ..., DEPTH0

Output
RD35, ..., RD0

Function

Dual port completely independent fully synchronous RAM; the RAM blocks may be cascaded up to 16 by configuring the Depth3-0 ports.

Actel recommends you use ACTgen RAM blocks instead of RAM macros because ACTgen configures WW/RW to choose the best aspect ratio and cascades multiple blocks to achieve larger configurations.

For RAM64K36P, data appears on RD after 2 clock cycles on RCLK

Write Truth Table

WCLK	WEN	Action
1	1	WD written to WRAD
0	1	None
X	0	None

Read Truth Table

RCLK	REN	Action
1	1	RD is read from RDAD
0	1	RD is unchanged
X	0	Rd is unchanged

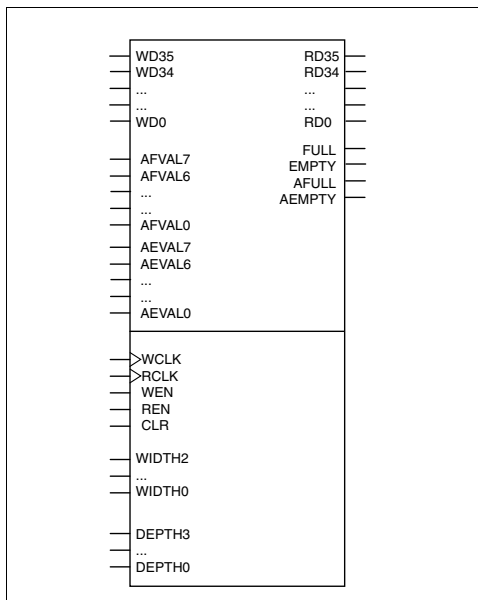
Family	Modules
	RAM
All listed	1

SRAM Port Aspect Ratios

Read/Write Depth	Read/Write Depth	Read/Write ADDR Bus	Read/Write Data Bus	RW/WW[2:0]
1	4096	ADDR[11:0]	DATA[0]	000
2	2048	ADDR[10:0]	DATA[1:0]	001
4	1024	ADDR[9:0]	DATA[3:0]	010
9	512	ADDR[8:0]	DATA[8:0]	011
18	256	ADDR[7:0]	DATA[17:0]	100
36	128	ADDR[6:0]	DATA[35:0]	101

FIFO64K36

Accelerator

**Input**

WD35, ..., WD0,
AFVAL7, ..., AFVAL0,
AEVAL7, ..., AEVAL0,
WCLK, RCLK, WEN,
REN, CLR,
WIDTH2, ..., WIDTH0
DEPTH3, ..., DEPTH0

Output

RD35, ..., RD0
FULL, EMPTY, AFULL,
AEMPTY

Function

Dual port completely independent fully synchronous FIFO

Write Truth Table

WCLK			Action

Read Truth Table

		Action

Family	Modules
	RAM
All listed	1

FIFO Aspect Ratios Table 1

Data Width	FIFO Depth	Read/Write Data Bus	Width[2:0]
1	4096	DATA[0]	000
2	2048	DATA[1:0]	001
4	1024	DATA[3:0]	010
9	512	DATA[8:0]	011
18	256	DATA[17:0]	100
36	128	DATA[35:0]	101

FIFO Aspect Ratios Table 2

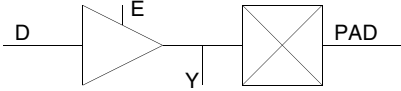
Depth	Cascaded Blocks	Full ^a	Address Bus WCNT/RCNT	AEVAL/AFVAL Step Size
00001	1	2^{12-W}	[15:W]	2^{8-W}
00011	2	2^{13-W}	[15:W]	2^{8-W}
00111	4	2^{14-W}	[15:W]	2^{8-W}
01111	8	2^{15-W}	[15:W]	2^{8-W}
11111	16	2^{16-W}	[15:W]	2^{8-W}

a. W = width in FIFO Aspect Ratios Table 1

I/O Macros

BIBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

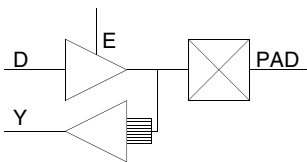
Input
D, E, PAD

Output
PAD, Y

Family	Modules	
	Seq	I/O
All		1

CLKBIBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX-A, 54SX-S

**Function**

Bidirectional with Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

Input
D, E, PAD

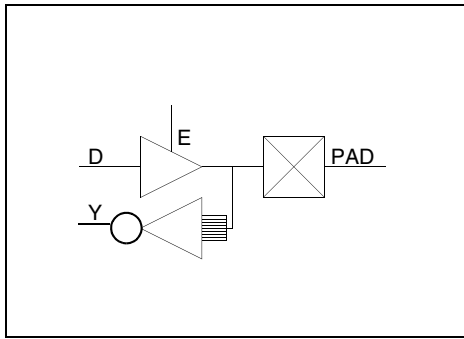
Output
PAD, Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to Actel's Databook for more Clock Network information.

CLKBIBUFI

54SX-A, 54SX-S

**Function**

Biderctional with inverted Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

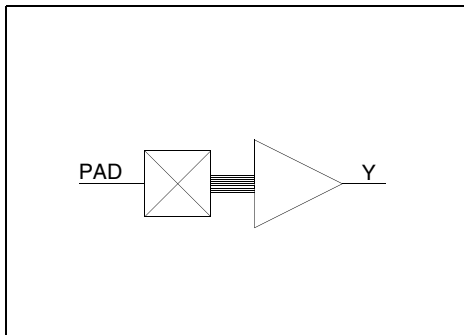
Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
54SX-A, 54SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

CLKBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator

**Function**

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input PAD	Output Y
---------------------	--------------------

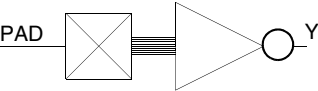
Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

CLKBUFI

54SX, 54SX-A, 54SX-S, eX



Function

Inverting Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	1
1	0

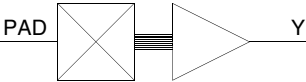
Input PAD	Output Y
--------------	-------------

Family	Modules	
	Seq	I/O
54SX, 54SX-A, 54SX-S, eX		1

NOTE 1: For an internal Clock net, refer to the CLKINT1 macro.
NOTE 2: Refer to Actel's Databook for more Clock Network information.

HCLKBUF

ACT 3, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Function

Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

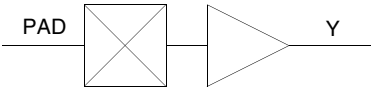
Input PAD	Output Y
--------------	-------------

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to Actel's Databook for more Clock Network information.

INBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Logic diagram of an Input Buffer (INBUF). The input is labeled PAD, and the output is labeled Y. The circuit consists of a buffer (square with an X) followed by an inverter (triangle).

Function

Input Buffer

Truth Table

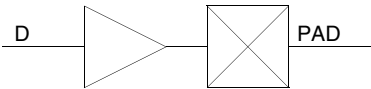
PAD	Y
0	0
1	1

Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All listed		1

OUTBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX, Axcelerator



Logic diagram of an Output Buffer (OUTBUF). The input is labeled D, and the output is labeled PAD. The circuit consists of an inverter (triangle) followed by a buffer (square with an X).

Function

Output Buffer, High Slew

Truth Table

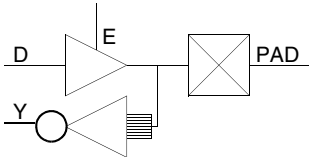
D	PAD
0	0
1	1

Input	Output
D	PAD

Family	Modules	
	Seq	I/O
All		1

QCLKBIBUFI

54SX-A, 54SX-S



Function
Biderctional with inverted Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

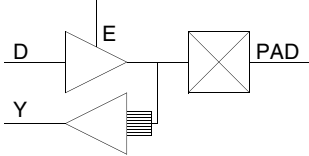
Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
54SX-A, 54SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

QCLKBIBUF

54SX-A, 54SX-S



Function
Biderctional with Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

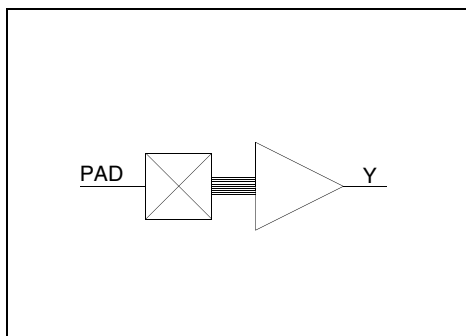
Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
54SX-A, 54SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

QCLKBUF

3200DX, 42MX, 54SX-A, 54SX-S

**Function**

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input PAD	Output Y
---------------------	--------------------

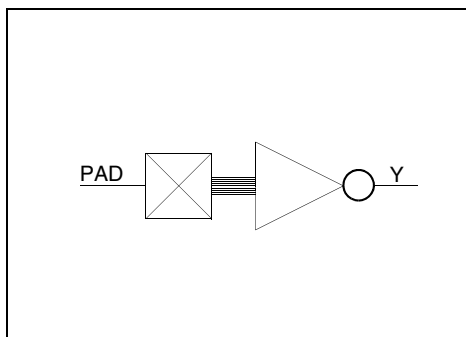
Family	Modules	
	Seq	I/O
All listed		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

QCLKBUF_I

54SX-A, 54SX-S

**Function**

Inverted Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	1
1	0

Input PAD	Output Y
---------------------	--------------------

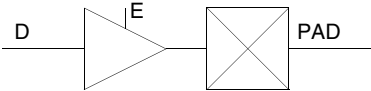
Family	Modules	
	Seq	I/O
54SX-A, 54SX-S		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

TRIBUFF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, 54SX-S, eX



Function

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

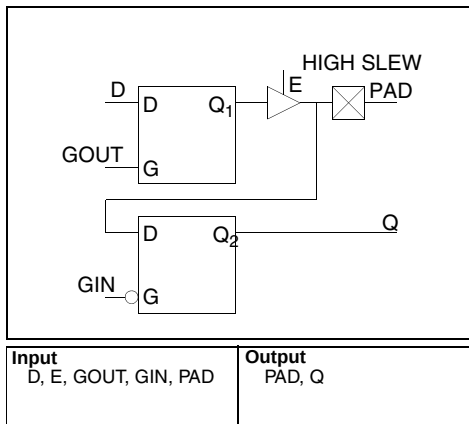
Input D, E	Output PAD
---------------	---------------

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

BBDLHS

ACT 2/1200XL, 3200DX, 42MX



Function

Bidirectional with Input Latch and Output Latch

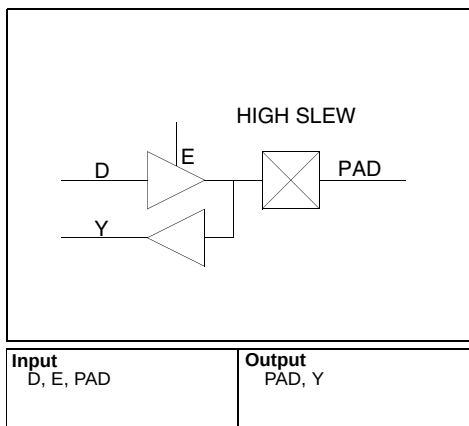
Truth Table

MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD _{n-1}	Q _{n-1}
	1	1	0	D	D
INPUT	0	X	1	X	Q _{n-1}
	0	X	0	X	PAD
TRISTATE	0	X	X	Z	X

Family	Modules	
	Seq	I/O
All listed		1

BBHS

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Bidirectional Buffer, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of BBHS we recommend that you use "BIBUF" on page 256.

IBDL

ACT 2/1200XL, 3200DX, 42MX

The diagram shows a logic macro. An input labeled 'PAD' is connected to a buffer (represented by a square with an 'X'). The output of the buffer is connected to the 'D' input of a D-type flip-flop. The flip-flop is clocked by an input labeled 'G' through an inverter (represented by a triangle with a bubble). The output of the flip-flop is labeled 'Q'.

Function
Input Buffer with Input Latch, with active low Clock

Truth Table

G	Q
1	Q_{n-1}
0	PAD

Input
G, PAD

Output
Q

Family	Modules	
	Seq	I/O
All listed		1

IR

ACT 2/1200XL, 3200DX, 42MX

The diagram shows a logic macro. An input labeled 'PAD' is connected to a buffer (represented by a square with an 'X'). The output of the buffer is connected to the 'D' input of a D-type flip-flop. The flip-flop is clocked by an input labeled 'CLK' through a D flip-flop symbol. The output of the flip-flop is labeled 'Q'.

Function
Input Register

Truth Table

CLK	Q
↑	PAD

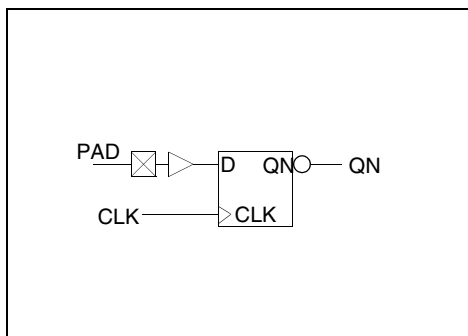
Input
PAD, CLK

Output
Q

Family	Modules	
	Seq	I/O
All listed	1	1

IRI

ACT 2/1200XL, 3200DX, 42MX



Function

Input register with active Low output

Truth Table

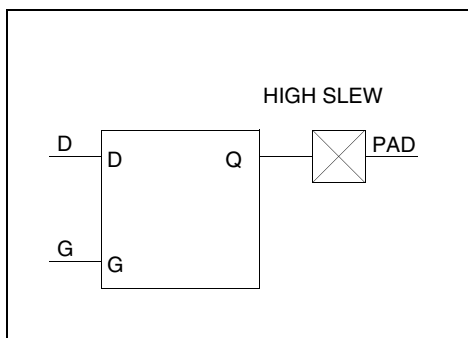
CLK	QN
↑	!PAD

Input PAD, CLK	Output QN
--------------------------	---------------------

Family	Modules	
	Seq	I/O
All listed	1	1

OBDLHS

ACT 2/1200XL, 3200DX, 42MX



Function

Output Buffer with Output Latch, High Slew

Truth Table

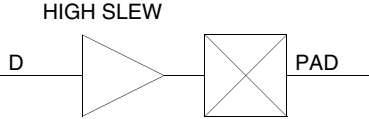
G	PAD
0	PAD _{n-1}
1	D

Input D, G	Output PAD
----------------------	----------------------

Family	Modules	
	Seq	I/O
All listed		1

OBHS

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

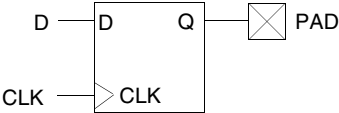
Input D	Output PAD
------------	---------------

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of OBHS we recommend that you use “OUTBUF” on page 259.

ORH

ACT 2/1200XL, 3200DX, 42MX



Function

Output Register, High Slew

Truth Table

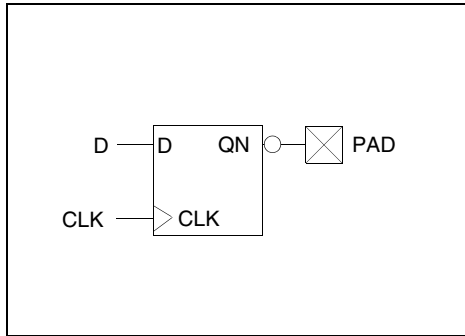
CLK	PAD _{n+1}
↑	D

Input D, CLK	Output PAD
-----------------	---------------

Family	Modules	
	Seq	I/O
All listed	1	1

ORIH

ACT 2/1200XL, 3200DX, 42MX



Function

Inverted Output Register, High Slew

Truth Table

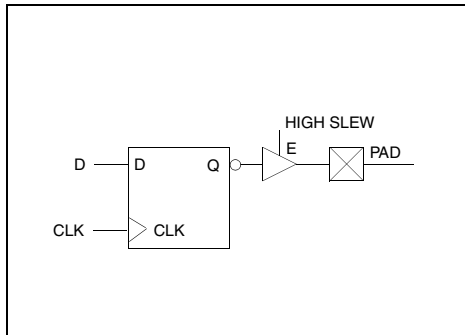
CLK	PAD _{n+1}
↑	ID

Input	Output
D, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

ORITH

ACT 2/1200XL, 3200DX, 42MX



Function

Inverted Output Register, Tristate Enable, High Slew

Truth Table

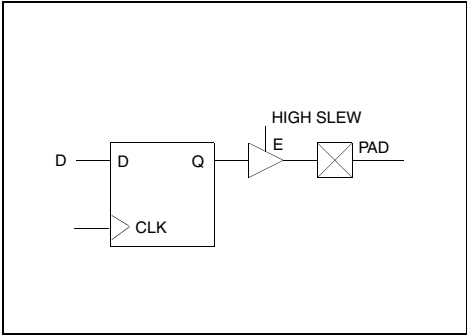
E	CLK	PAD _{n+1}
0	X	Z
1	↑	ID

Input	Output
D, E, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

ORTH

ACT 2/1200XL, 3200DX, 42MX



Function
Output Register, Tristate Enable, High Slew

Truth Table

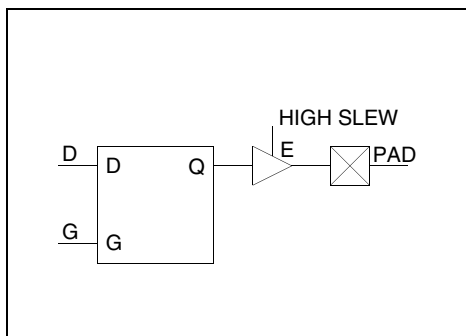
E	CLK	PAD _{n+1}
0	X	Z
1	↑	D

Input D, E, CLK	Output PAD
---------------------------	----------------------

Family	Modules	
	Seq	I/O
All listed	1	1

TBDLHS

ACT 2/1200XL, 3200DX, 42MX



Function

Tristate Output with Latch, High Slew

Truth Table

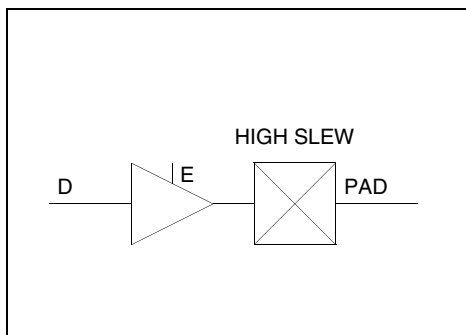
E	G	PAD
0	X	Z
1	1	D
1	0	PAD _{n-1}

Input	Output
D, E, G	PAD

Family	Modules	
	Seq	I/O
All listed		1

TBHS

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of TBHS we recommend that you use "TRIBUFF" on page 262.

BBHSA

ACT 3

Input
D, E, IDE, PAD

Output
PAD, Y

Function
Bidirectional buffer with AND gate, High Slew

Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Family	Modules	
	Seq	I/O
ACT 3		1

BBLSA

ACT 3

Input
D, E, IDE, PAD

Output
PAD, Y

Function
Bidirectional buffer with AND gate, Low Slew

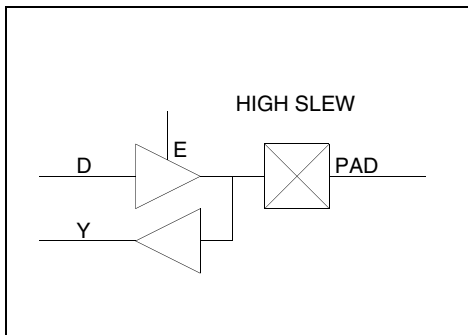
Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTH

ACT 3



Function

Bidirectional Buffer, Tristate Enable, High Slew

Truth Table

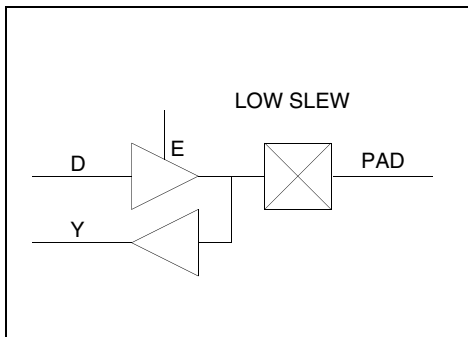
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTL

ACT 3



Function

Bidirectional Buffer, Tristate Enable, Low Slew

Truth Table

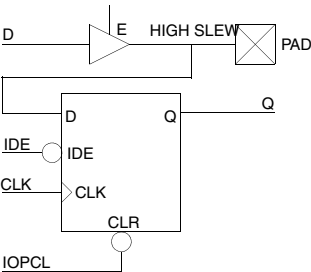
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTH

ACT 3



Input
D, E, IDE, CLK, IOPCL, PAD

Output
PAD, Q

Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

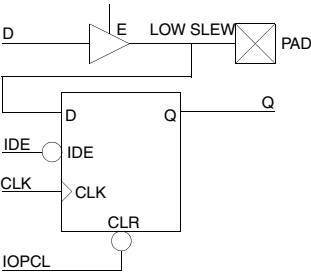
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTL

ACT 3



Input
D, E, IDE, CLK, IOPCL, PAD

Output
PAD, Q

Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

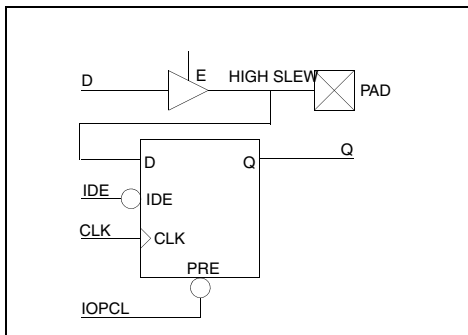
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPH

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Function

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, High Slew

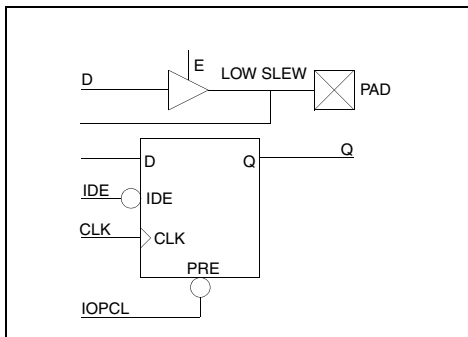
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTL

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Function

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTH

ACT 3

Input
D, E, ODE, CLK, IOPCL, PAD

Output
PAD, Y

Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTL

ACT 3

Input
D, E, ODE, CLK, IOPCL, PAD

Output
PAD, Y

Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

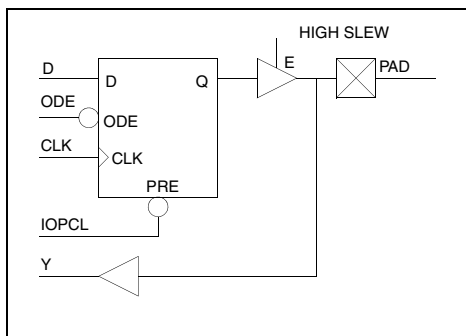
Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTH

ACT 3

**Function**

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input

D, E, ODE, CLK, IOPCL,
PAD

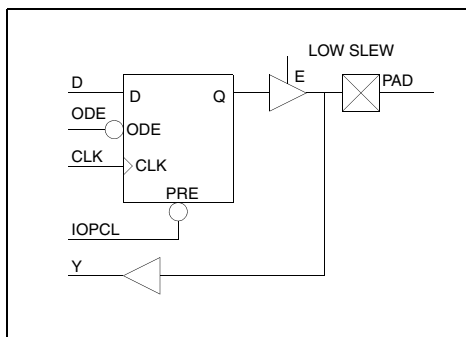
Output

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTL

ACT 3

**Function**

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input

D, E, ODE, CLK, IOPCL,
PAD

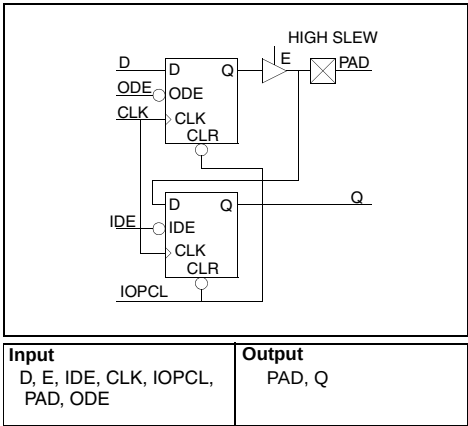
Output

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

DECETH

ACT 3



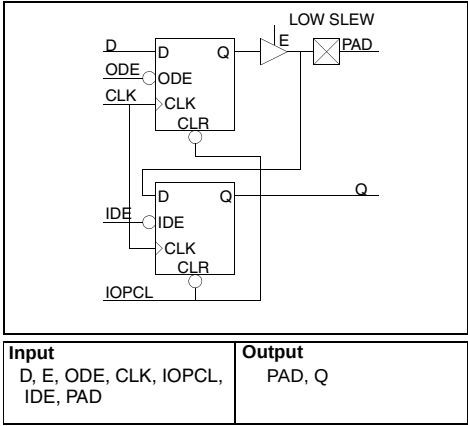
Family	Modules	
	Seq	I/O
ACT 3		1

Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table							
MODE	E	IOPL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q _{n-1}

DECETL

ACT 3



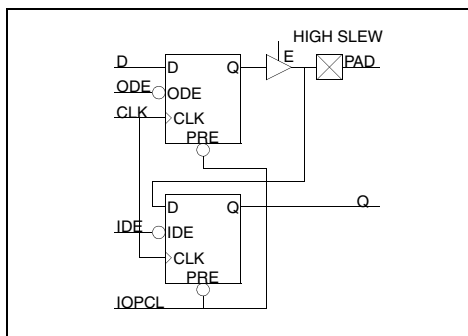
Family	Modules	
	Seq	I/O
ACT 3		1

Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table							
MODE	E	IOPL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q _{n-1}

DEPETH

ACT 3



Input
D, E, ODE, CLK, IOPCL,
IDE, PAD

Output
PAD, Q

Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

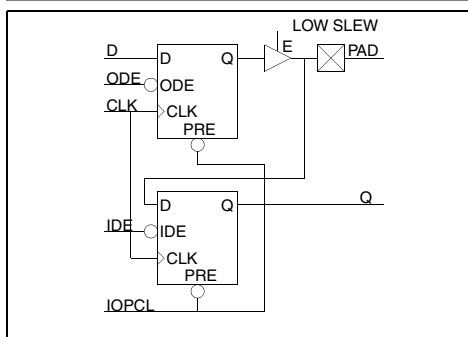
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETL

ACT 3



Input
D, E, ODE, CLK, IOPCL,
IDE, PAD

Output
PAD, Q

Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

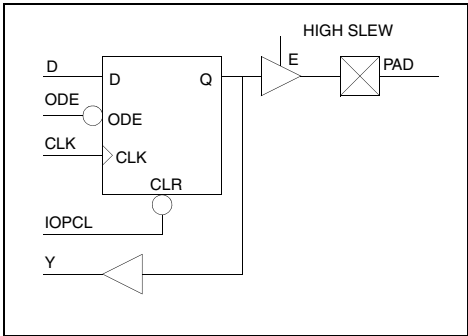
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

FECTH

ACT 3



Input	Output
D, E, ODE, CLK, IOPL, PAD	PAD, Y

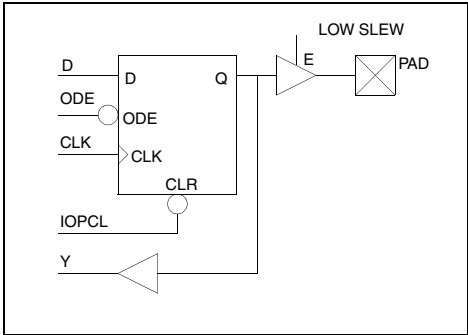
Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table					
E	IOPL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y _{n-1}	PAD _{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y _{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FECTL

ACT 3



Input	Output
D, E, ODE, CLK, IOPL, PAD	PAD, Y

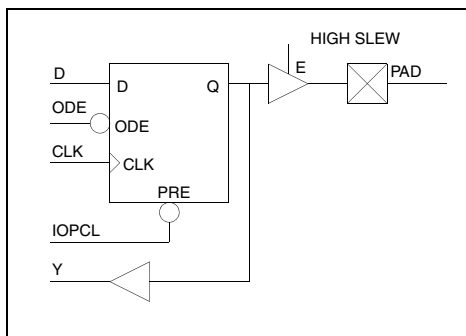
Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table					
E	IOPL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y _{n-1}	PAD _{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y _{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTH

ACT 3



Input
D, E, ODE, CLK,
IOPCL, PAD

Output
PAD, Y

Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

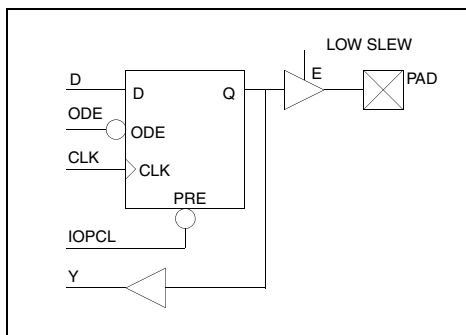
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTL

ACT 3



Input
D, E, ODE, CLK,
IOPCL, PAD

Output
PAD, Y

Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FECTMH

ACT 3

Input
D, E, ODE, CLK,
IOPCL, PAD, M

Output
PAD, Y

Function
Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FECTML

ACT 3

Input
D, E, ODE, CLK,
IOPCL, PAD, M

Output
PAD, Y

Function
Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

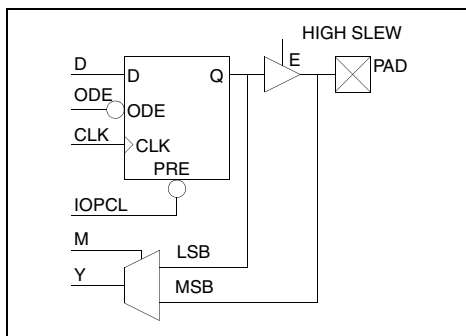
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTMH

ACT 3



Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table ¹

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

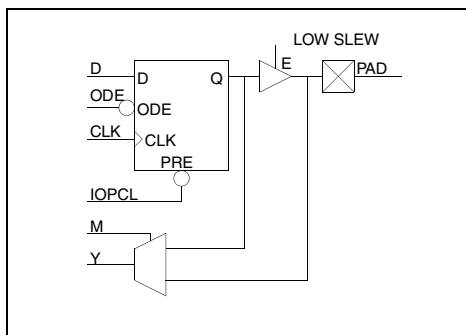
Family	Modules	
	Seq	I/O
ACT 3		1

1. NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTML

ACT 3



Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table ¹

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

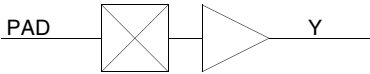
Family	Modules	
	Seq	I/O
ACT 3		1

1. NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

IBUF

ACT 3



Function
Input Buffer

Truth Table

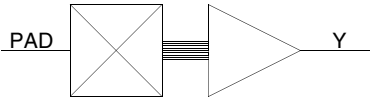
PAD	Y
0	0
1	1

Input PAD	Output Y
---------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

IOCLKBUF

ACT 3



Function
Dedicated I/O Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

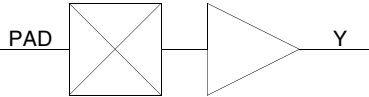
Input PAD	Output Y
---------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IOPCLBUF

ACT 3



Function

Dedicated I/O Preset Clear Buffer

Truth Table

PAD	Y
0	0
1	1

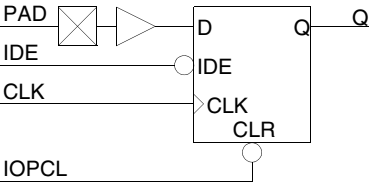
Input PAD	Output Y
---------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IREC

ACT 3



Function

Input Register, with Clear, Input Data Enable

Truth Table

IOPCL	IDE	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	PAD

Input PAD, IDE, CLK, IOPCL	Output Q
--------------------------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

IREP

ACT 3

Logic diagram of the IREP macro. It shows a D-type flip-flop with inputs PAD, IDE, CLK, and IOPCL. The output is Q. The PAD input is connected to the D input through a buffer. The IDE input is connected to the flip-flop's IDE input. The CLK input is connected to the flip-flop's CLK input. The IOPCL input is connected to the flip-flop's PRE input.

Function
Input Register, with Preset, Input Data Enable

Truth Table

IOPCL	IDE	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	PAD

Input
PAD, IDE, CLK, IOPCL

Output
Q

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTH

ACT 3

Logic diagram of the OBUFTH macro. It shows a buffer with inputs D and E. The output is PAD. The D input is connected to the buffer's input. The E input is connected to the buffer's enable input. The output of the buffer is connected to the PAD output.

Function
Output Buffer, Tristate Enable, High Slew

Truth Table

D	E	PAD
X	0	Z
0	1	0
1	1	1

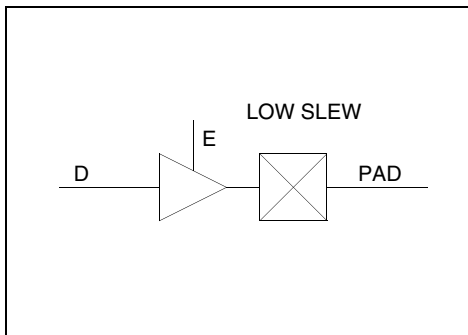
Input
D, E

Output
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTL

ACT 3



Function

Output Buffer, Tristate Enable, Low Slew

Truth Table

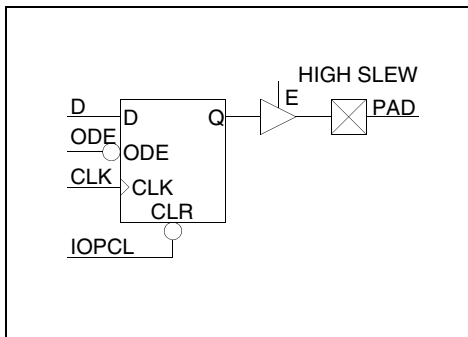
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTH

ACT 3



Function

Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTL

ACT 3

LOW SLEW

Function
Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input
D, ODE, CLK, IOPCL, E

Output
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTH

ACT 3

HIGH SLEW

Function
Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input
D, ODE, CLK, IOPCL, E

Output
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTL

ACT 3

Logic diagram of the OREPTL macro. It features a D-type flip-flop with inputs D, ODE, CLK, and PRE. The output Q is connected to a buffer labeled "LOW SLEW" which then connects to the PAD pin. The IOPCL pin is connected to the PRE input of the flip-flop.

Function

Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

Axcelerator Input IO Macros

Names for the input buffers are composed of up to 4 parts:

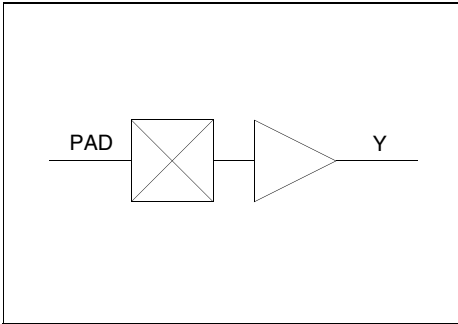
- A base name indicating the type of buffer :INBUF
- IO Technology like LVCMOS
- An optional number code 33,25,18 or 15 indicating a 3.3, 2.5, 1.8 OR 1.5 voltage level.
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- INBUF_LVCMOS25U - An input LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor.
- INBUF_PCIX - An input PCIX buffer

INBUF_X

Axcelerator



Input
PAD

Output
Y

Function
Global Input Buffer

Truth Table

PAD	Y
0	0
1	1

Family

Family	Modules	
	Seq	I/O
All listed		1

Available INBUF_X Macro Types

Name	Description
INBUF_LVCMOS25	LVCMOS Input buffer with 2.5 CMOS voltage level
INBUF_LVCMOS25U	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS25D	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-down resistor
INBUF_LVCMOS18	LVCMOS Input buffer with 1.8 CMOS voltage level
INBUF_LVCMOS18U	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-up resistor
INBUF_LVCMOS18D	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-down resistor
INBUF_LVCMOS15	LVCMOS Input buffer with 1.5 CMOS voltage level
INBUF_LVCMOS15U	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS15D	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-down resistor
INBUF_PCI	PCI Input buffer
INBUF_PCIX	PCIX Input buffer
INBUF_GTL25	GTLP Input buffer with 3.3 CMOS voltage level
INBUF_GTL33	GTLP Input buffer with 2.5 CMOS voltage level
INBUF_HSTL_I	HSTL Class I Input buffer
INBUF_SSTL2_I	SSTL2 Class I Input buffer
INBUF_SSTL2_II	SSTL2 Class II Input buffer
INBUF_SSTL3_I	SSTL3 Class I Input buffer
INBUF_SSTL3_II	SSTL3 Class II Input buffer

Bi-Directional IO Macros

Names for the bi-directional buffers are composed of up to 4 parts:

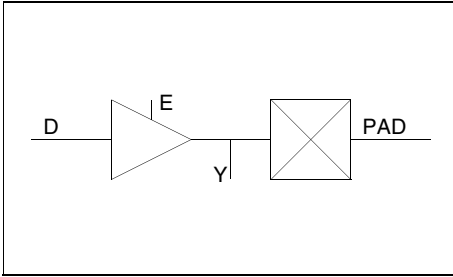
- A base name indicating the type of buffer :BIBUF
- Optional IO Technology like LVC MOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- BIBUF_LVCMOS25 - A bi-directional LVC MOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- BIBUF_S_8- A bi-directional buffer with low slew and 1x drive strength

BIBUF_X

Axcelerator

**Function**

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Family

Family	Modules	
	Seq	I/O
All		1

Input
D, E, PAD

Output
Y, PAD
Available BIBUF_X Macro Types

Name	Description
BIBUF_LVCMOS25	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_LVCMOS25U	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS25D	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS18	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level
BIBUF_LVCMOS18U	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS18D	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS15	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level
BIBUF_LVCMOS15U	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS15D	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level, pull-down resistor
BIBUF_PCI	PCI Bi-directional buffer
BIBUF_PCIX	PCIX Bi-directional buffer
BIBUF_GTL25	GTLP Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_GTL33	GTLP Bi-directional buffer with 3.3 CMOS voltage level
BIBUF_F_8	Bi-directional buffer with high slew and 1x drive strength
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-up resistor
BIBUF_F_8D	Bi-directional buffer with high slew and 1x drive strength, pull-down resistor
BIBUF_F_12	Bi-directional buffer with high slew and 2x drive strength
BIBUF_F_12U	Bi-directional buffer with high slew and 2x drive strength, pull-up resistor
BIBUF_F_12D	Bi-directional buffer with high slew and 2x drive strength, pull-down resistor
BIBUF_F_16	Bi-directional buffer with high slew and 3x drive strength
BIBUF_F_16U	Bi-directional buffer with high slew and 3x drive strength, pull-up resistor
BIBUF_F_16D	Bi-directional buffer with high slew and 3x drive strength, pull-down resistor
BIBUF_F_24	Bi-directional buffer with high slew and 4x drive strength
BIBUF_F_24U	Bi-directional buffer with high slew and 4x drive strength, pull-up resistor
BIBUF_F_24D	Bi-directional buffer with high slew and 4x drive strength, pull-down resistor
BIBUF_S_8	Bi-directional buffer with low slew and 1x drive strength
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-up resistor
BIBUF_S_8D	Bi-directional buffer with low slew and 1x drive strength, pull-down resistor
BIBUF_S_12	Bi-directional buffer with low slew and 2x drive strength
BIBUF_S_12U	Bi-directional buffer with low slew and 2x drive strength, pull-up resistor
BIBUF_S_12D	Bi-directional buffer with low slew and 2x drive strength, pull-down resistor
BIBUF_S_16	Bi-directional buffer with low slew and 3x drive strength
BIBUF_S_16U	Bi-directional buffer with low slew and 3x drive strength, pull-up resistor
BIBUF_S_16D	Bi-directional buffer with low slew and 3x drive strength, pull-down resistor
BIBUF_S_24	Bi-directional buffer with low slew and 4x drive strength
BIBUF_S_24U	Bi-directional buffer with low slew and 4x drive strength, pull-up resistor
BIBUF_S_24D	Bi-directional buffer with low slew and 4x drive strength, pull-down resistor

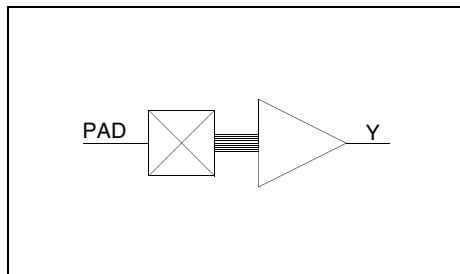
Clock Buffers

Names for the input buffers are composed of up to 3 parts:

- A base name indicating the type of buffer :CLKBUF
- IO Technology like LVCMOS
- An optional number code 33,25,18 or 15 indicating a 3.3,2.5, 1.8 OR 1.5 voltage level

CLKBUF_X

Axcelerator



Function

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input

PAD

Output

Y

Family

Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

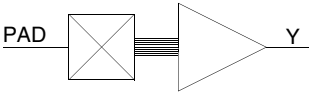
Available CLKBUF_X Macro Types

Name	Description
CLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level
CLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
CLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
CLKBUF_PCI	PCI Clock buffer
CLKBUF_PCIX	PCIX Clock buffer
CLKBUF_GTL25	GTL25 Clock buffer with 2.5 CMOS voltage level
CLKBUF_GTL33	GTL33 Clock buffer with 3.3 CMOS voltage level
CLKBUF_HSTL_I	HSTL Class I Clock buffer
CLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
CLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
CLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
CLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

HClock Buffers

Naming convention is identical to the naming for Clock Buffers.

HCLKBUF_XAxcelerator



Function
Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

Family

Family	Modules	
	Seq	I/O
All		1

NOTE 1: Refer to Actel's Databook for more Clock Network information.

Input
PAD

Output
Y

Available HCLKBUF_X Macro Types

Name	Description
HCLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level
HCLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
HCLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
HCLKBUF_PCI	PCI Clock buffer
HCLKBUF_PCIX	PCIX Clock buffer
HCLKBUF_GTLP25	GTLP Clock buffer with 2.5 CMOS voltage level
HCLKBUF_GTLP33	GTLP Clock buffer with 3.3 CMOS voltage level
HCLKBUF_HSTL_I	HSTL Class I Clock buffer
HCLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
HCLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
HCLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
HCLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

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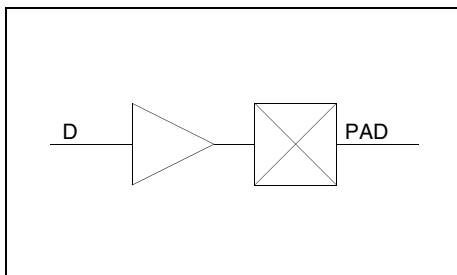
Output Buffers

Names for the bi-directional buffers are composed of up to 4 parts:

- A base name indicating the type of buffer :OUTBUF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew

OUTBUF_X

Axcelerator



Function

Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

Family

Family	Modules	
	Seq	I/O
All		1

Input
D

Output
PAD

Available OUTBUF_X Macro Types

Name	Description
OUTBUF_LVCMOS25	LVCMOS Output buffer with 2.5 CMOS voltage level
OUTBUF_LVCMOS18	LVCMOS Output buffer with 1.8 CMOS voltage level
OUTBUF_LVCMOS15	LVCMOS Output buffer with 1.5 CMOS voltage level
OUTBUF_PCI	PCI Output buffer
OUTBUF_PCIX	PCIX Output buffer
OUTBUF_GTL25	GTL Output buffer with 2.5 CMOS voltage level
OUTBUF_GTL33	GTL Output buffer with 3.3 CMOS voltage level
OUTBUF_F_8	Output buffer with high slew and 1x drive strength
OUTBUF_F_12	Output buffer with high slew and 2x drive strength
OUTBUF_F_16	Output buffer with high slew and 3x drive strength
OUTBUF_F_24	Output buffer with high slew and 4x drive strength
OUTBUF_S_8	Output buffer with low slew and 1x drive strength
OUTBUF_S_12	Output buffer with low slew and 2x drive strength
OUTBUF_S_16	Output buffer with low slew and 3x drive strength
OUTBUF_S_24	Output buffer with low slew and 4x drive strength

Tri-State Buffer Macros

Names for the bi-directional buffers are composed of up to 4 parts:

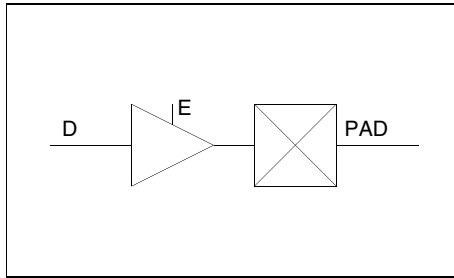
- A base name indicating the type of buffer :BIBUF
- Optional IO Technology like LVC MOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- BIBUF_LVC MOS25 - A bi-directional LVC MOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- BIBUF_S_8- A bi-directional buffer with low slew and 1x drive strength

TRIBUFF_X

Axcelerator

**Function**

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Family

Family	Modules	
	Seq	I/O
All		1

Input
D, E

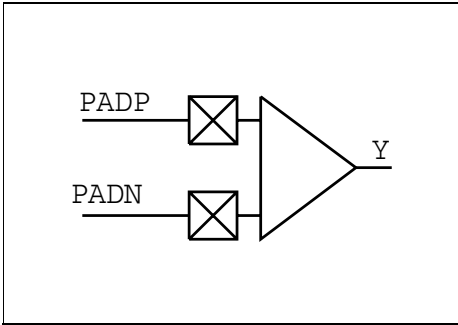
Output
PAD
Available TRIBUFF_X Macro Types

Name	Description
BIBUF_LVCMOS25	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_LVCMOS25U	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS25D	LVC MOS Bi-directional buffer with 2.5 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS18	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level
BIBUF_LVCMOS18U	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS18D	LVC MOS Bi-directional buffer with 1.8 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS15	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level
BIBUF_LVCMOS15U	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS15D	LVC MOS Bi-directional buffer with 1.5 CMOS voltage level, pull-down resistor
BIBUF_PCI	PCI Bi-directional buffer
BIBUF_PCIX	PCIX Bi-directional buffer
BIBUF_GTL P25	GTLP Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_GTL P33	GTLP Bi-directional buffer with 3.3 CMOS voltage level
BIBUF_F_8	Bi-directional buffer with high slew and 1x drive strength
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-up resistor
BIBUF_F_8D	Bi-directional buffer with high slew and 1x drive strength, pull-down resistor
BIBUF_F_12	Bi-directional buffer with high slew and 2x drive strength
BIBUF_F_12U	Bi-directional buffer with high slew and 2x drive strength, pull-up resistor
BIBUF_F_12D	Bi-directional buffer with high slew and 2x drive strength, pull-down resistor
BIBUF_F_16	Bi-directional buffer with high slew and 3x drive strength
BIBUF_F_16U	Bi-directional buffer with high slew and 3x drive strength, pull-up resistor
BIBUF_F_16D	Bi-directional buffer with high slew and 3x drive strength, pull-down resistor
BIBUF_F_24	Bi-directional buffer with high slew and 4x drive strength
BIBUF_F_24U	Bi-directional buffer with high slew and 4x drive strength, pull-up resistor
BIBUF_F_24D	Bi-directional buffer with high slew and 4x drive strength, pull-down resistor
BIBUF_S_8	Bi-directional buffer with low slew and 1x drive strength
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-up resistor
BIBUF_S_8D	Bi-directional buffer with low slew and 1x drive strength, pull-down resistor
BIBUF_S_12	Bi-directional buffer with low slew and 2x drive strength
BIBUF_S_12U	Bi-directional buffer with low slew and 2x drive strength, pull-up resistor
BIBUF_S_12D	Bi-directional buffer with low slew and 2x drive strength, pull-down resistor
BIBUF_S_16	Bi-directional buffer with low slew and 3x drive strength
BIBUF_S_16U	Bi-directional buffer with low slew and 3x drive strength, pull-up resistor
BIBUF_S_16D	Bi-directional buffer with low slew and 3x drive strength, pull-down resistor
BIBUF_S_24	Bi-directional buffer with low slew and 4x drive strength
BIBUF_S_24U	Bi-directional buffer with low slew and 4x drive strength, pull-up resistor
BIBUF_S_24D	Bi-directional buffer with low slew and 4x drive strength, pull-down resistor

Differential IO Macros

INBUF_LVDS; INBUF_LVPECL

Axcelerator



Input
PADP; PADN

Output
Y

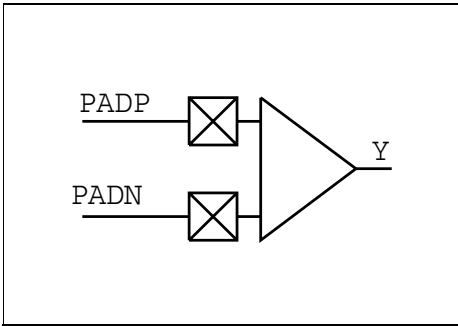
Function
INBUF_LVDS and INBUF_LVPECL

Available Differential Macro Types

Name	Description
INBUF_LVDS	
INBUF_LVPECL	

CLKBUF_LVDS; CLKBUF_LVPECL

Axcelerator



Input
PADP; PADN

Output
Y

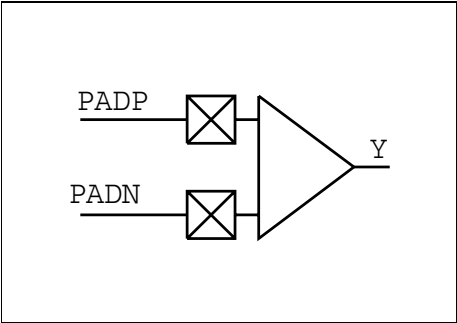
Function
CLKBUF_LVDS and CLKBUF_LVPECL

Available Differential Macro Types

Name	Description
CLKBUF_LVDS	
CLKBUF_LVPECL	

HCLKBUF_LVDS; HCLKBUF_LVPECL

Axcelerator



Function
HCLKBUF_LVDS and HCLKBUF_LVPECL

Input
PADP; PADN

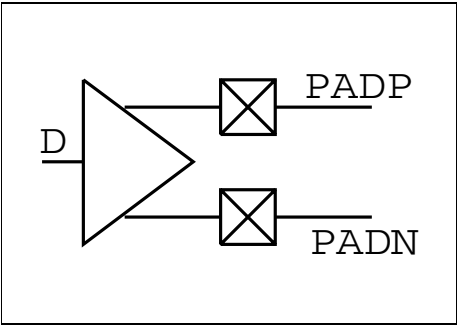
Output
Y

Available Differential Macro Types

Name	Description
HCLKBUF_LVDS	
HCLKBUF_LVPECL	

OUTBUF_LVDS; OUTBUF_LVPECL

Axcelerator



Function
OUTBUF_LVDS and OUTBUF_LVPECL

Input
A

Output
PADP, PADN

Available Differential Macro Types

Name	Description
OUTBUF_LVDS	
OUTBUF_LVPECL	

IOFIFO (PerPin FIFO) Macros

IOFIFO (PerPin FIFO)

Axcelerator

Diagram of the IOFIFO (PerPin FIFO) block. It has six inputs: REN (active low), RCLK, WD, WEN (active low), WCLK, and CLR (active low). It has one output: RD.

Function

64x1 PerPin FIFO with Synchronous falling write and read, with active low write and read enables; please refer to the Axcelerator datasheet for more information on the IOFIFO

Truth Table

WCLK	RCLK	WEN	REN	ACTION
↓	X	0	X	WD written to the current FIFO location
↓	X	1	X	None
↓	↓	X	0	Contents of the current FIFO location appear at RD
↓	↓	X	1	RD is unchanged

Input

WD, WCLK, RCLK, WEN, REN, CLR

Output

RD

IOFIFOCTL

Axcelerator

Diagram of the IOFIFOCTL block. It has 16 inputs: AFVAL5, AFVAL4, AFVAL3, AFVAL2, AFVAL1, AFVAL0, AEVAL5, AEVAL4, AEVAL3, AEVAL2, AEVAL1, AEVAL0, WEN, REN, RCLK, and WCLK. It has 7 outputs: FULL, AFULL, EMPTY, AEMPTY, BWEN, BREN, and BCLR. There is also a CLR input at the bottom.

Function

Embedded PerPin FIFO controller with Almost Full and Almost Empty flags; please refer to the Axcelerator datasheet for more information on the Embedded Pin FIFO Controller.

NOTE: Each Embedded PerPin FIFO controller can control a maximum of 26 Per-Pin FIFOs depending on the location of the PerPin FIFOs on the die. BWEN needs to be connected to the WEN of the PerPin FIFOs. BREN needs to be connected to REN and BCLR to CLR.

Input

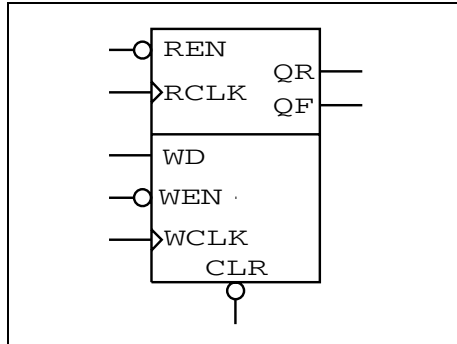
AFVAL5, ..., AFVAL0
AEVAL5, ..., AEVAL0
WCLK, RCLK, WEN, REN, CLR

Output

FULL, EMPTY, AFULL, AEMPTY, BWEN, BREN, BCLR

DDR_FIFO

Axcelerator

**Input**WD, WCLK, RCLK,
WEN, REN, CLR**Output**

QR, QF

Function

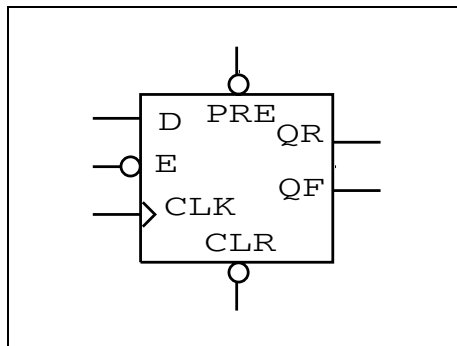
64X1 Dual Data Rate (DDR), PerPin FIFO with Synchronous write and read, with active low write and read enables; please refer to the Axcelerator datasheet for more information on the DDR_FIFO

Truth Table

WCLK	RCLK	WEN	REN	ACTION
↓↑	X	0	X	WD written to the current FIFO location
↓↑	X	1	X	None
X	↓	X	0	Contents of the current FIFO location appear at QF
X	↑	X	0	Contents of the current FIFO location appear at QR
X	↓↑	X	1	QR/QF is unchanged

DDR_REG

Axcelerator

**Input**

D, CLK, E, PRE, CLR

Output

QR, QF

Function

DDR (DDR) Register with active low write and read enables; please refer to the Axcelerator datasheet for more information on the DDR_REG

Truth Table

CLR	PRE	E	CLK	QR(n+1)	QF(n+1)
0	X	X	X	0	0
1	0	X	X	1	1
1	1	1	X	QR(n)	QF(n)
1	1	0	↑	D(↑)	X
1	1	0	↓	X	D(↓)

Carry Chain Macros

ADD1

Axcelerator

A

B

FCI

S

FCO

Input

A, B, FCI

Output

S, FCO

Function

1 Bit Adder

Truth Table

A	B	FCI	S	FCO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Family	Modules
	COMB
All listed	1

SUB1

Axcelerator

A

B

FCI

S

FCO

Input

A, B, FCI

Output

S, FCO

Function

1 Bit Subtractor

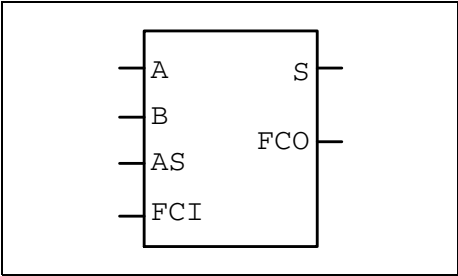
Truth Table

A	B	FCI	S	FCO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Family	Modules
	Comb
All listed	1

ADDSUB1

Axcelerator



Input
AS, B, A, FCI

Output
S, FCO

Function
1 Bit Add Sub macro

Truth Table

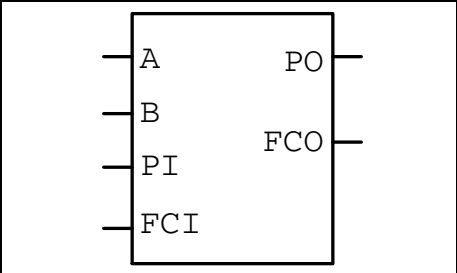
AS	B	A	FCI	S	FCO
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

Family

Family	Modules
	Comb
All listed	2

MULT1

Axcelerator



Input
A, B, PI, FCI

Output
PO, FCO

Function
1 Bit Multiplier

Truth Table

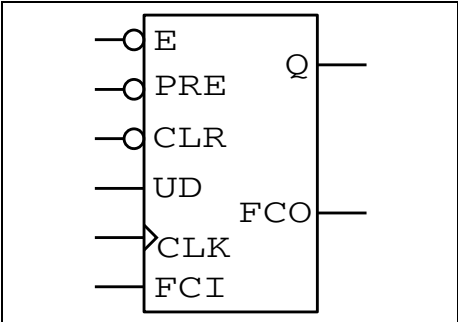
A	B	PI	FCI	PO	FCO
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

Family

Family	Modules
	Comb
All listed	1

ARCNTECP1

Axcelerator



Input
FCI, CLK, PRE, CLR,
UD

Output
Q, FCO

Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q _{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	O _n
See Equations		1	1	0	↑	See Equations	

$Q_{n+1} = FCI \wedge UD \wedge O_n$

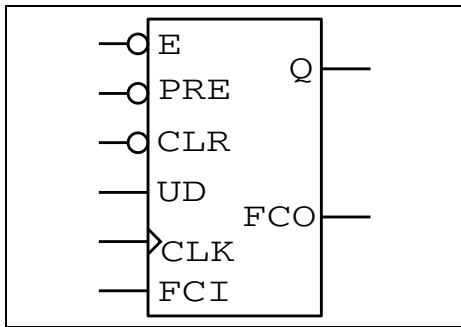
$FCO = FCI.UD + FCI.O_n + UD.O_n$

Family

Family	Modules	
	Comb	Seq
All listed	1	

ARCNTECP1

Axcelerator



Function
1 Bit counter

Truth Table

FCl	UD	PRE	CLR	E	CLK	FCO	Q _{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	O _n
See Equations		1	1	0	↑	See Equations	

Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

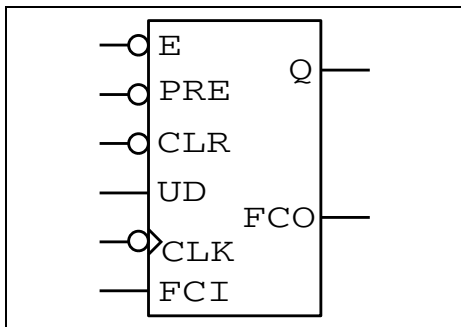
$$Q_{n+1} = FCI \wedge UD \wedge O_n$$
$$FCO = FCI.UD + FCI.O_n + UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

AFCNTECP1

Axcelerator



Function
1 Bit counter

Truth Table

FCl	UD	PRE	CLR	E	CLK	FCO	Q _{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	O _n
See Equations		1	1	0	↓	See Equations	

Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

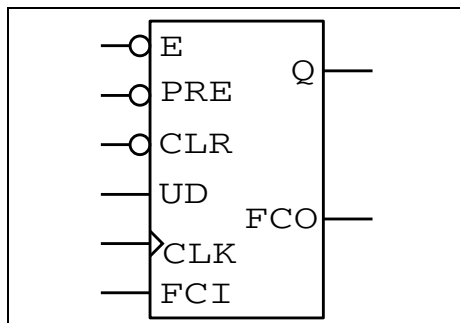
$$Q_{n+1} = FCI \wedge UD \wedge O_n$$
$$FCO = FCI.UD + FCI.O_n + UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

SRCNTECP1

Axcelerator



Input
FCI, CLK, PRE, CLR,
UD

Output
Q, FCO

Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	O_n
See Equations		1	1	0	↑	See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge O_n$$

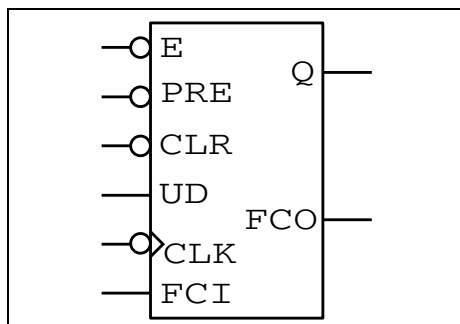
$$FCO = FCI.!UD + FCI.O_n + !UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

SFCNTECP1

Axcelerator



Input
FCI, CLK, PRE, CLR,
UD

Output
Q, FCO

Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	O_n
See Equations		1	1	0	↓	See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge O_n$$

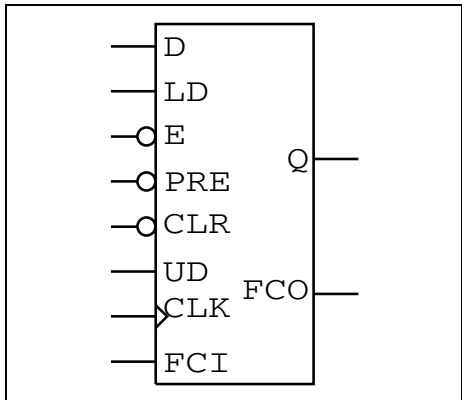
$$FCO = FCI.!UD + FCI.O_n + !UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

ARCNTELDCP1

Axcelerator



Input
 FCI, CLK, PRE, CLR, E,
 LD, D, and UD

Output
 Q, FCO

Family

Family	Modules	
	Comb	Seq
All listed	2	1

Function
1 Bit counter

Truth Table

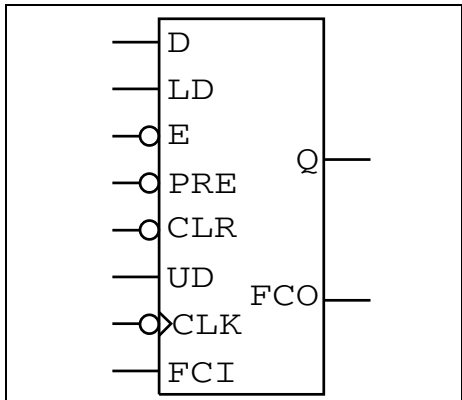
FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	O_n
X	X	1	1	0	1	0	↑	X	0
X	X	1	1	0	1	1	↑	X	1
See Equations		1	1	0	0	X	↑	See Equations	

$$Q_{n+1} = FCI \wedge UD \wedge O_n$$

$$FCO = FCI.UD + FCI.O_n + UD.O_n$$

AFCNTELDCP1

Axcelerator



Input
 FCI, CLK, PRE, CLR, E,
 LD, D, and UD

Output
 Q, FCO

Family

Family	Modules	
	Comb	Seq
All listed	2	1

Function
1 Bit counter

Truth Table

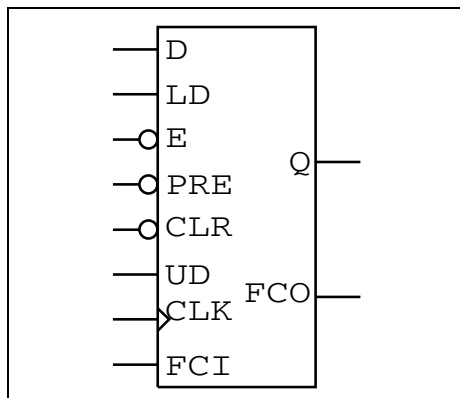
FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	O_n
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

$$Q_{n+1} = FCI \wedge UD \wedge O_n$$

$$FCO = FCI.UD + FCI.O_n + UD.O_n$$

SRCNTELDCP1

Accelerator



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q _{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	O _n
X	X	1	1	0	1	0	↑	X	0
X	X	1	1	0	1	1	↑	X	1
See Equations		1	1	0	0	X	↑	See Equations	

Input

FCI, CLK, PRE, CLR, E, LD, D, and UD

Output

Q, FCO

$$Q_{n+1} = FCI \wedge !UD \wedge O_n$$

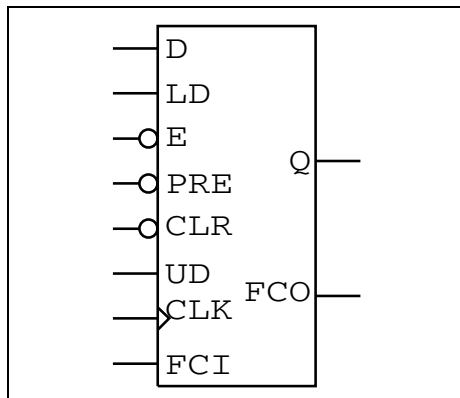
$$FCO = FCI!UD + FCI.O_n + !UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

SFCNTELDCP1

Accelerator



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q _{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	O _n
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

Input

FCI, CLK, PRE, CLR, E, LD, D, and UD

Output

Q, FCO

$$Q_{n+1} = FCI \wedge !UD \wedge O_n$$

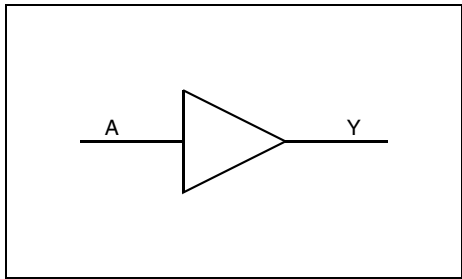
$$FCO = FCI!UD + FCI.O_n + !UD.O_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

FCEND_BUFF

Axcelerator



Input
A

Output
Y

Function
Buffer, driven by the FCO pin of the last macro in the Carry-Chain

Truth Table

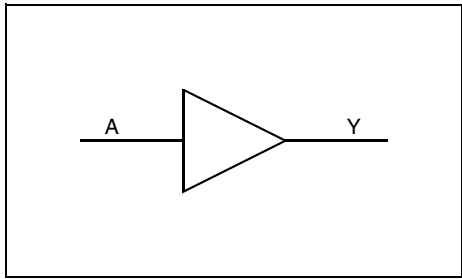
A	Y
0	0
1	1

Family

Family	Modules	
	Seq	COMB
All		1

FCEND_INV

Axcelerator



Input
A

Output
Y

Function
Inverter with Active Low output; driven by the FCO pin of the last macro in the Carry-Chain

Truth Table

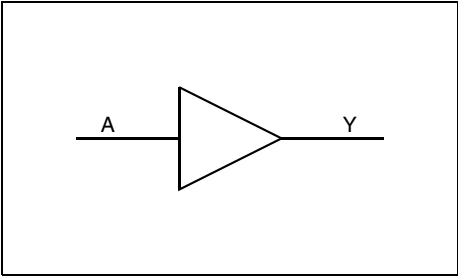
A	Y
0	1
1	0

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_BUFF

Axcelerator



Input
A

Output
Y

Function
Buffer, used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

Truth Table

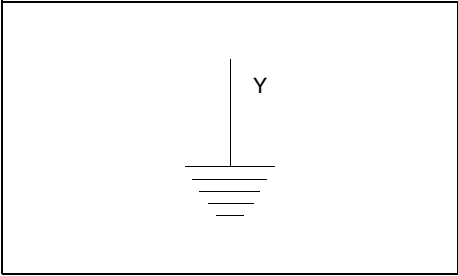
A	Y
0	0
1	1

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_GND

Axcelerator



Input

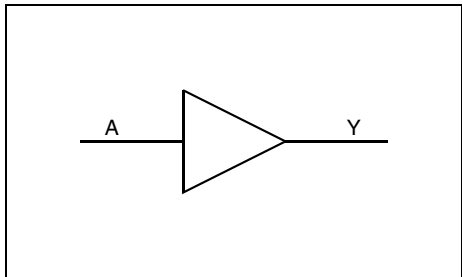
Output
Y

Function
Ground; used to initialize the FCI pin of the first macro in the Carry-Chain to GND

NOTE: Ground does not use any modules

FCINIT_INV

Axcelerator



Input
A

Output
Y

Function
Inverter with Active Low output; used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

Truth Table

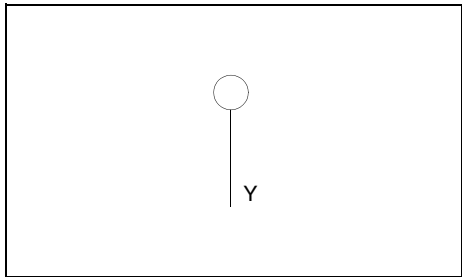
A	Y
0	1
1	0

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_VCC

Axcelerator



Input
A

Output
Y

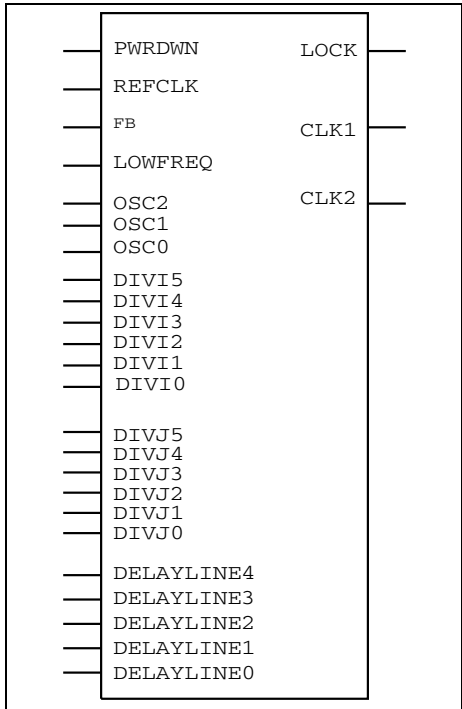
Function
Power; used to initialize the FCI pin of the first macro in the Carry-Chain to VCC

NOTE: VCC does not use any modules

PLL Macros

PLL; PLLFB

Axcelerator



Function
PLL: PLL with internal feedback; PLLFB: PLL with external feedback.
NOTE: PLL and PLLFB are identical except for the FB pin; if you wish to use internal feedback, use the regular PLL.

Actel recommends that you use ACTgen to generate your PLLs; ACTgen calculates the settings for all the pins in the PLL for the required input-output frequency combinations.

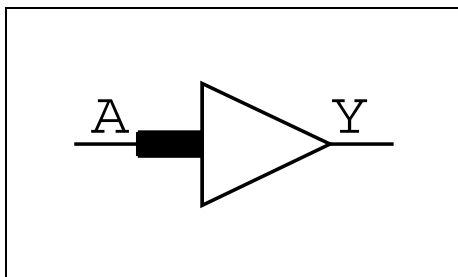
Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

Input
PWRDWN, REFCLK,
LOWFREQ, OSC2, OSC1,
OSC0, DIVI5, DIVI4,
DIVI3, DIVI2, DIVI1,
DIVI0, DIVJ5, DIVJ4,
DIVJ3, DIVJ2, DIVJ1,
DIVJ0, DELAYLINE4,
DELAYLINE3,
DELAYLINE2,
DELAYLINE1,
DELAYLINE0

Output
LOCK, CLK1, CLK2

PLLINT

Axcelerator

**Input**

A

Output

Y

Function

PLL Int

Truth Table

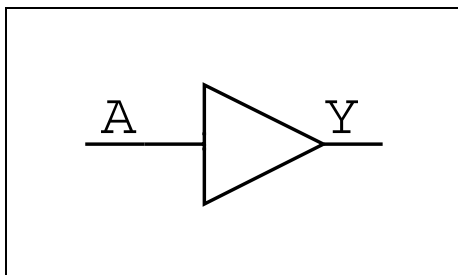
A	Y
0	0
1	1

Connect only to the REFCLK input of PLL when the PLL is driven by a pad other than the one in the same super cluster.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

PLLOUT

Axcelerator

**Input**

A

Output

Y

Function

PLL OUT

Truth Table

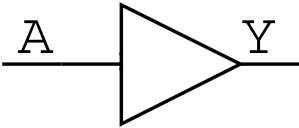
A	Y
0	0
1	1

Connect only to the CLK output of PLL when the PLL is driving a net other than the HCLK/RCLK networks.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

PLLHCLK

Axcelerator



Function
PLL HCLK

Truth Table

A	Y
0	0
1	1

Connect only to the CLK output of the PLL; use it to drive the HCLK network.

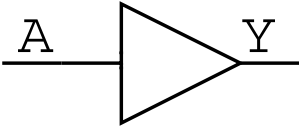
Input
A

Output
Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

PLLCLK

Axcelerator



Function
PLL RCLK

Truth Table

A	Y
0	0
1	1

Connect only to the CLK output of the PLL; use it to drive the RCLK network.

Input
A

Output
Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.