PLD World Korea 2001

Excalibur-Nios Embedded Software Processor Core

Enter a New Realm of Technology...

System-On-a-Programmable-Chip Solutions

ALTERA® MJL®

Agenda

- Quartus II Limited Edition
- PCI32 Nios Target
- Nios Ethernet Development Kit (NEDK)
- Microtronix Linux Development Kit (LDK)
- Nios 2.0
- Competitive Landscape

Quartus II
Limited Edition

Quartus II Limited Edition

- Provides device compilation for Nios Development Kit customers
- Feature set based on Quartus II Web Edition, with some extra features to support Nios
  - TCL scripting
  - LeonardoSpectrum synthesis for Nios core
  - Development kit-specific devices:
    - EP20K200EFC484 – Used in NDK
    - EP20K200EBC652
    - EP20K100EQC240
  - See https://go.altera.com/extranet2001/products/literature/mb_2001/mb_411.doc for QII Web edition details.
- Provided to all Nios customers, starting in September
  - Shipped to all current Nios customers
  - Shipping today with all new Excalibur Nios Development Kits

Quartus II LE Key Points

- **Current Quartus II subscribers do *not* need to install QII LE**
- Obtaining License Files
  - Altera sends an email that includes a new license file for QII LE to all current Nios customers.
    - Quartus II v1.1 enabled through October 31, 2001
    - Quartus II Limited Edition enabled to eternity
  - The QII LE shipment also includes explicit instructions how to obtain a license online.
- NOTE: LogicLock is not enabled in QII LE
  - May affect customers with high performance needs
- "Where do I download a copy of QII LE?"
  - Answer: You don't.
    - Quartus II LE is *shipped* with the Nios Development Kit or upgrades only

Nucleus PLUS by ATI

- Nucleus PLUS Evaluation CD included in Quartus II LE shipment
- Popular embedded RTOS
  - Used in thousands of applications
- Small memory footprint and minimal CPU overhead
- Source code
- No royalties
- More information:
  - www.acceleratedtechnology.com

KROS by Shugyo Design Technologies

- KROS “Preview” CD included in Quartus II LE shipment
  - Full release in October
- Embedded RTOS
  - Supports POSIX API
- Very small memory footprint
- Source code
- No royalties
- $5000 Per-product license
- More information:
  - www.shugyodesign.com

Arriba! By Viosoft

- Evaluation CD included in Quartus II LE shipment
- Complete Integrated Development Environment (IDE)
  - Edit, Compile, Download, Run ,Debug
  - Fully integrated mixed-mode, source-level C/C++ debugger
  - First vendor to support Nios 2.0 On-Chip Debug
- For more information:
  - www.viosoft.com

PCI32 Nios Target MegaCore Function

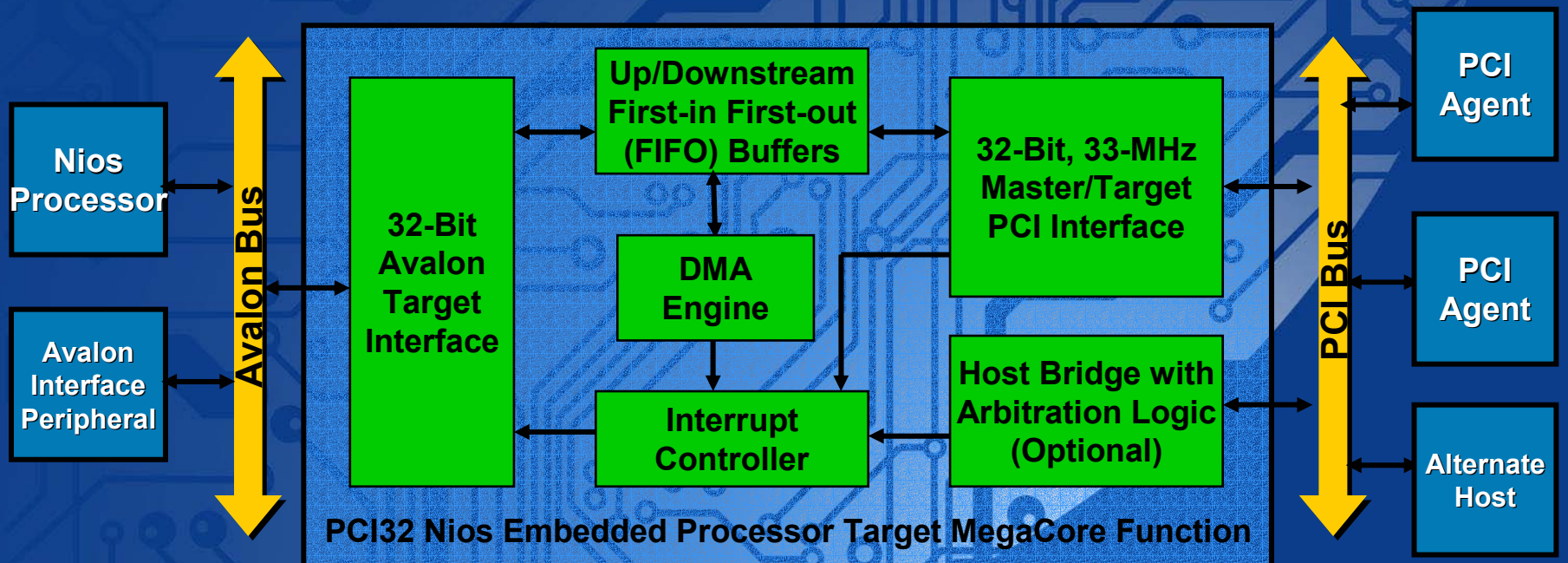
Ver 1.0

PCI32 Nios Target MegaCore® Function

- PCI Interface to Nios via Avalon™ Bus Bridge
- Nios System Builder Interface
- Behavioral Simulation Models
- PCI Testbench for PCI32 Nios Target Core
- Low-Level Driver Routines in C Source Code for Nios Embedded Processor
- Reference Design for Use with Nios Embedded Processor
- Complete Documentation
- List Price: $2,495
- Available: Oct 2001

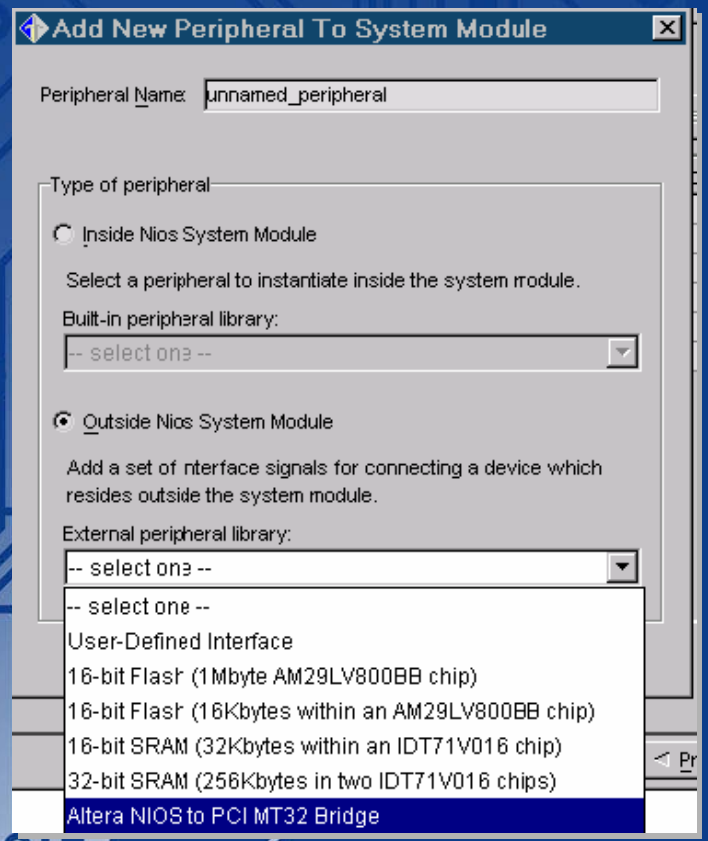
PCI32 Nios Target Architecture

- Simple, Integrated Bridge Solution
- Includes Optional PCI Host Bridge Capability
- Implemented as External Peripheral to Nios Processor
- Approximately 3,000 Logic Elements (LEs)



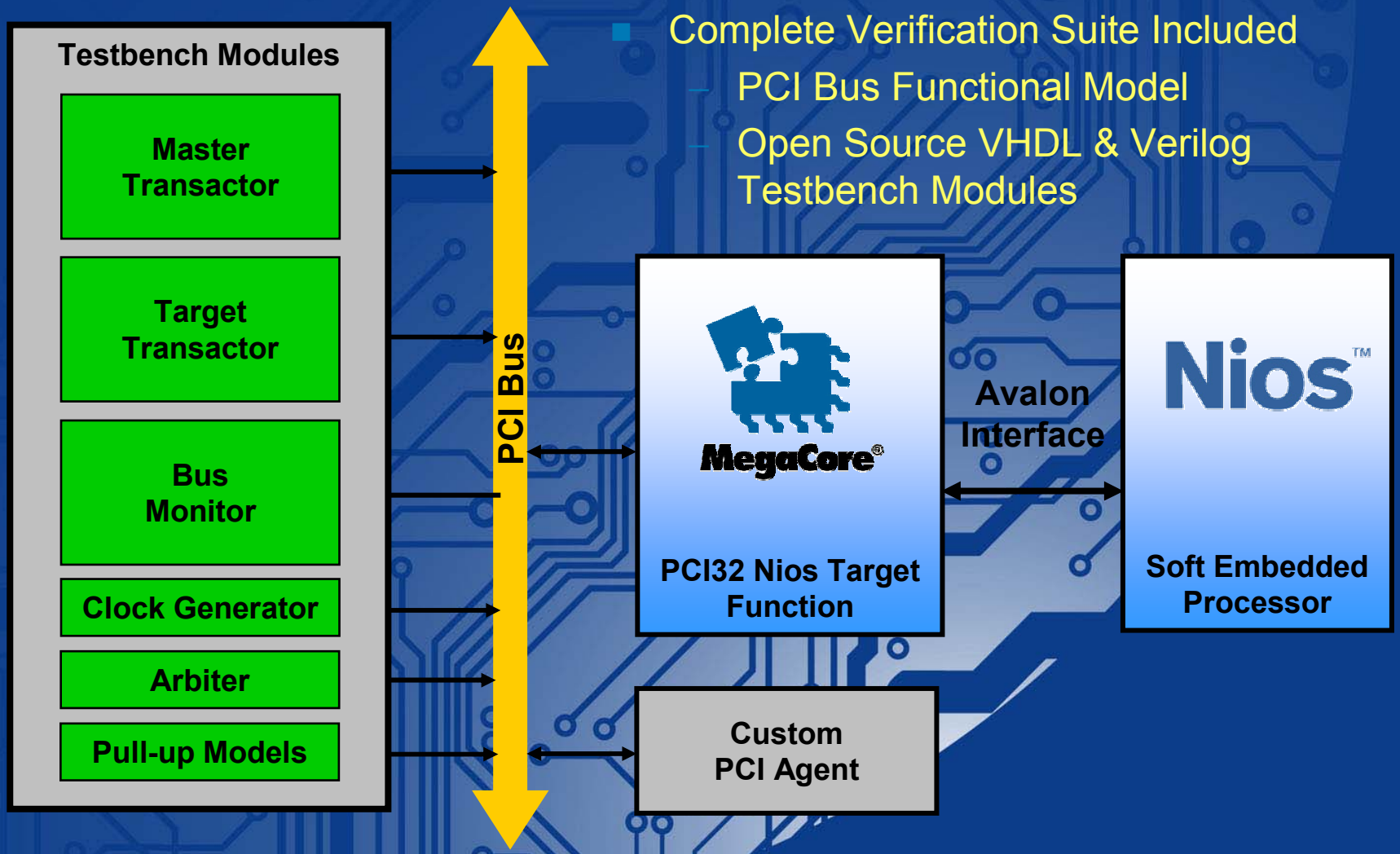
Nios System Builder

- Simple, Integrated Design Entry
- Steps to Instantiate PCI32 Nios Target
  1. Download the PCI32 Nios Target From the IP MegaStore™ Site
     http://www.altera.com/IPmegastore
  2. Start the Nios System Builder
  3. Select PCI32 Nios Bridge from Drop-Down Menu
  4. Parameterize PCI Bridge Options
  5. Specify Avalon Address Space & Interrupts
  6. Connect Core to Avalon System Block
  7. Compile Project in Quartus® II Software



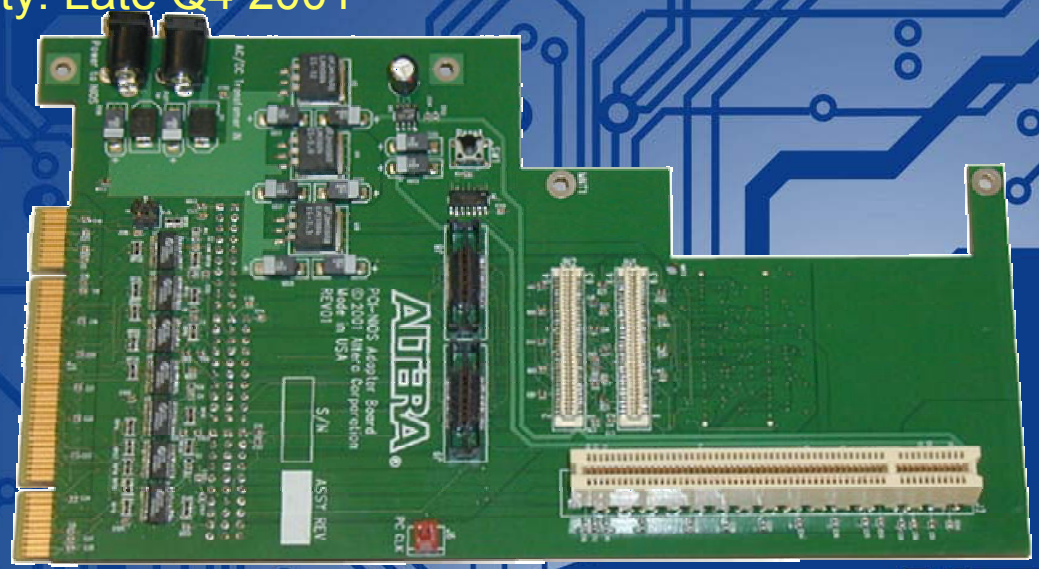
PCI32 Nios Target Testbench

- Complete Verification Suite Included
  - PCI Bus Functional Model
  - Open Source VHDL & Verilog Testbench Modules



PCI32 Nios Target Add-On Kit

- Kit Contents
  - PCI32 Nios Target MegaCore Function
  - PCI Daughter Card for Nios Development Board
    - Universal 32-bit Edge Connector & 5V PCI Slot
    - PMC Connectors to Nios Board
  - Hardware Reference Design
  - Price: $2,795
  - Availability: Late Q4 2001



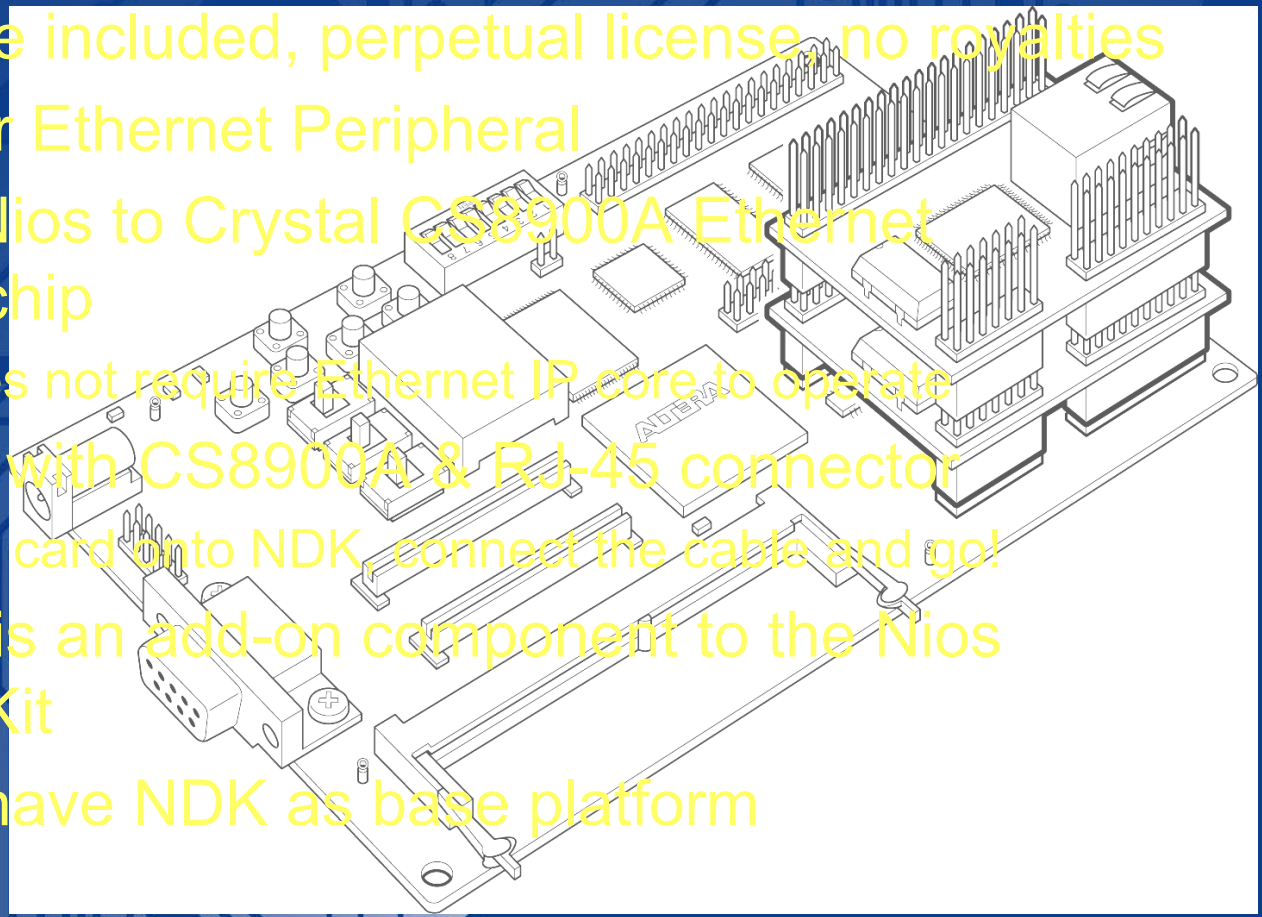
PCI Core Comparison

- PCI/MT32 (32-bit, 66-Mhz PCI)
  - Fully compliant “general purpose” PCI core
  - Master/Target PCI
  - Parameterizable
  - Host bridge functionality
  - Testbench included
  - Behavioral models included
  - Support for up to five (5) base address registers (BARs)
  - Complete access to all local-side signals
  - $8,995
- PCI32 Nios Target (32-bit, 33-Mhz PCI)
  - Fully compliant “Nios-only” PCI core
  - Master/Target PCI
  - Parameterizable
  - Host bridge functionality
  - Testbench included
  - Behavioral models included
  - Support for one (1) base address register (BAR)
  - Access to PCI through Avalon bus only
  - $2,495

Nios Ethernet Development Kit (NEDK)

Nios Ethernet Development Kit

- C-language network protocol library
  - Source code included, perpetual license, no royalties
- System Builder Ethernet Peripheral
  - Interfaces Nios to Crystal CS8900A Ethernet MAC/PHY chip
    - NEDK does not require Ethernet IP core to operate
- Daughter card with CS8900A & RJ-45 connector
  - Plug daughter card onto NDK, connect the cable and go!
- ***NOTE***: NEDK is an add-on component to the Nios Development Kit
  - User must have NDK as base platform

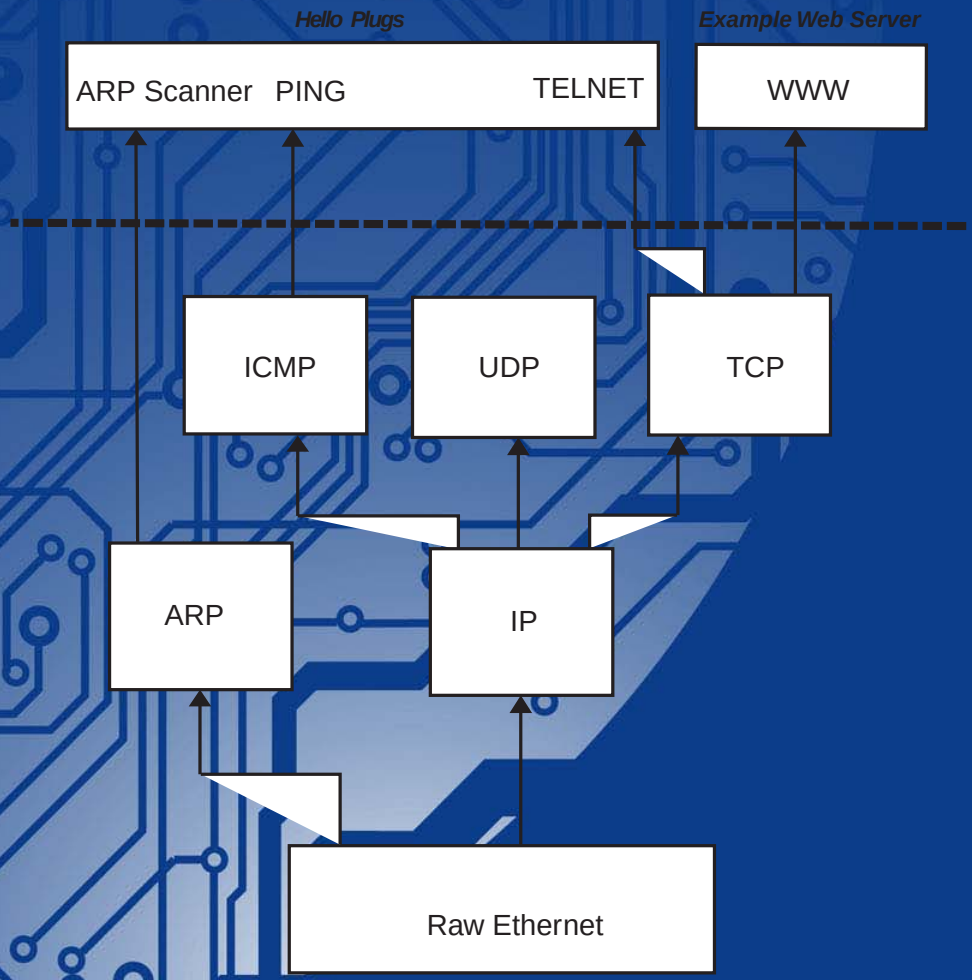


Features - Basics

- **C libraries to implement network protocols for embedded systems**
  - OS not required
- **Compact memory and processor requirements**
  - 20KB of memory for code
  - 8KB of memory for data
  - Nios timer peripheral
- **Parameters to easily configure network feature set**
  - Optimize code size
  - Optimize run-time memory requirements

Features – Protocol Support

- **Support for the following protocols:**
  - Raw Ethernet
  - Address resolution protocol (ARP)
  - Internet protocol (IP)
  - Internet control message protocol (ICMP)
  - User datagram protocol (UDP)
  - Transmission control protocol (TCP)
- **Similar functionality to UNIX "sockets" C routines**
  - User can open connections and send data with only a few lines of C code



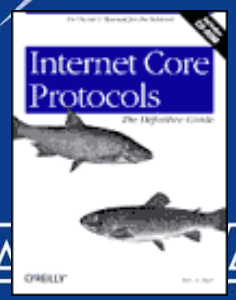
PLUGS LIBRARY

Plugs

- "Plugs" is the library of C network functions that ships with NEDK
- Very similar to UNIX "Sockets" functions
  - Provides all the necessary tools to communicate data over Ethernet
  - There is not a one-to-one relationship between Plugs and Sockets functions
- These functions are not compatible with any other Ethernet protocol tools

What do you get in the box?

- Hardware:
  - NEDK Daughter Card. Mounts on NDK Dev Board.
  - Ethernet **cable** & **cross-over adapter**
    - Support for both NEDK-to-LAN and NEDK-to-PC connection
- Installer CD-ROM
  - Software tools: System Builder **Nios Ethernet Peripheral**
  - Embedded software: **Network Protocol Libraries**
    - C Source Code
  - **Software reference application**: Web Server
  - **Hardware reference design**: Nios CPU platform
    - Networked Nios platform functions straight out of the box
- Documentation:
  - ***Nios Ethernet Development Kit User Guide***
    - http://www.altera.com/literature/ug/ug_niosedk.pdf
  - O'Reilly ***Internet Core Protocols Manual***



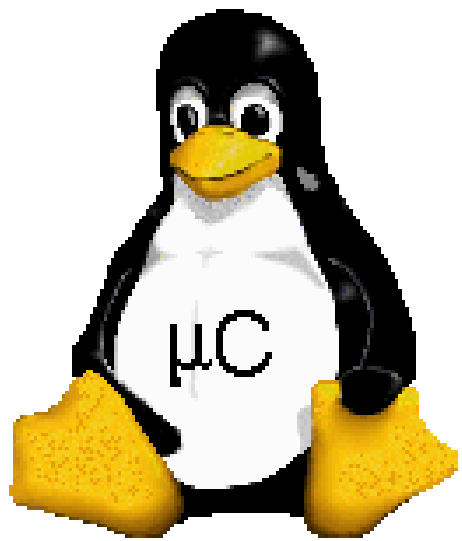
Potential NEDK customers

- Designers of simple, networked devices
  - Want network connectivity, but don't want the overhead of Linux for network functions
    - OS not required
  - NEDK is perfect to enable a Nios system to communicate system data over a network
- Systems that require remote programming over network
  - Reprogram flash (including Nios design!) and MAX devices in the field without physical human interaction
    - Altera can give out reference design & source code
- Systems that require a faster interface than a standard serial cable
  - In general, Ethernet is a means of high-speed communication
    - Ex: GERMS monitor over Ethernet allows much faster data download to the Nios Development Board

Ordering Information & Support

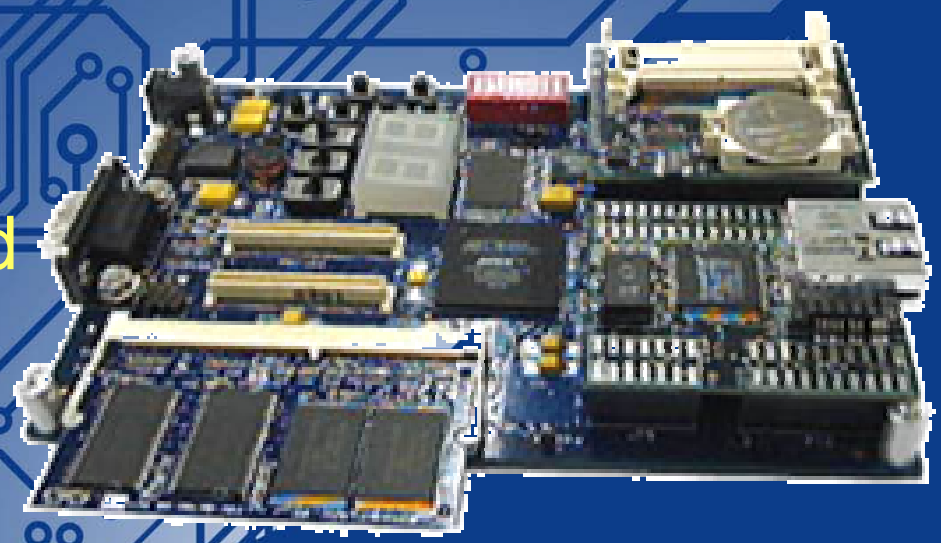
- **NIOS-EDKX**
  - $495
  - Available ***NOW***
- **For support:**
  - Altera Applications
    - Apps is first point of contact. May be referred to Excalibur Apps
    - Provides install & basic “getting started” support
    - Design support for Altera devices
  - Excalibur Applications
    - Support for in-depth Nios development issues with Ethernet

Linux Development Kit, by Microtronix



Nios Linux Development Kit (LDK)

- Linux for Nios!
  - μCLinux ported to the Nios processor
- Complete hardware and software platform that enables Linux development straight out of the box
  - A Linux prompt in 30 minutes, or the source code is free!
- **Not** a "Linux for Dummies" platform
- Designed & Produced by Microtronix



µCLinux ("You See Linux")

- Derivative of the Linux 2.0 kernel
- Developed for microcontrollers without Memory Management Units (MMUs)
- Offers the traditional benefits of Linux:
  - Stability, built-in network capability, file system support, large community of Linux developers
- Small memory footprint (…*for a Linux system*)
  - Runtime memory required for Kernel + Application
    - As low as 1 MByte
    - Large compared to typical embedded applications, but small for Linux
- Internet-ready embedded OS
  - Network protocols built in
- Open Source. No licensing fees. No Royalties.

Microtronix

- Established design and consulting firm for software and hardware
- ACAP Partner
- Extensive experience in telecom hardware design and embedded Linux
- Provide in depth support and consulting
  - Device driver development
  - PLD design, specializing in Altera
  - Embedded Linux development
  - Kernel - level development
  - Application design and development
  - Real-time embedded support
  - Telephony voice and data
  - Analog and Digital expertise
  - Legacy systems integration
  - VOIP convergence, XDSL, Sonet
- Offer flexible support programs

What do you get in the LDK box?

- uCLinux kernel source code
- Three daughter boards to enable Linux development on NDK board
  - **Memory Expansion**: SDRAM & flash
  - **OS Support**: Real-time Clock & IDE interface (IDE interface support coming soon)
  - **Ethernet Connectivity**: Same card as NEDK daughter card with CS8900A & RJ-45
  - Serial Y-cable for debug
  - ***NOTE***: LDK *Requires* NDK dev board as base platform!
- Software & reference application
  - Web server
  - Linux command shell
  - uCLibC & Kernel open source
- Hardware reference design
  - Linux works out of the box, no Quartus compile necessary

Potential LDK Customers

- Embedded Linux system developers
- Customers creating network-enabled products
- Customers who traditionally use a home-grown OS
  - They probably *don't* want to keep supporting a proprietary OS
  - They're used to having access to source code
    - Won't get it with VxWorks or other closed-source OS
  - They're used to bugs being fixed immediately
- "Penny pinchers"
  - VxWorks is expensive stuff
  - No Royalties for Linux
- Mention Nios & uCLinux to anyone who asks
  - "We can do Linux" is a strong validation for the Nios platform
  - Not everyone needs to do Linux, but everyone wants to know you can

Who probably *doesn't* need LDK?

- Tiny embedded systems with little memory
  - uCLinux needs at least 1MByte
- Designers who want to install and have a working system on the same day
  - Combining the perfect Linux kernel feature set is not a trivial task
    - Design services are available from Microtronix
  - In general, Linux involves a learning curve
- Developers who need an RTOS
  - Linux is *not* an RTOS
    - Some real time kernel extensions *could be* designed – Contact Microtronix for consulting

Ordering Information

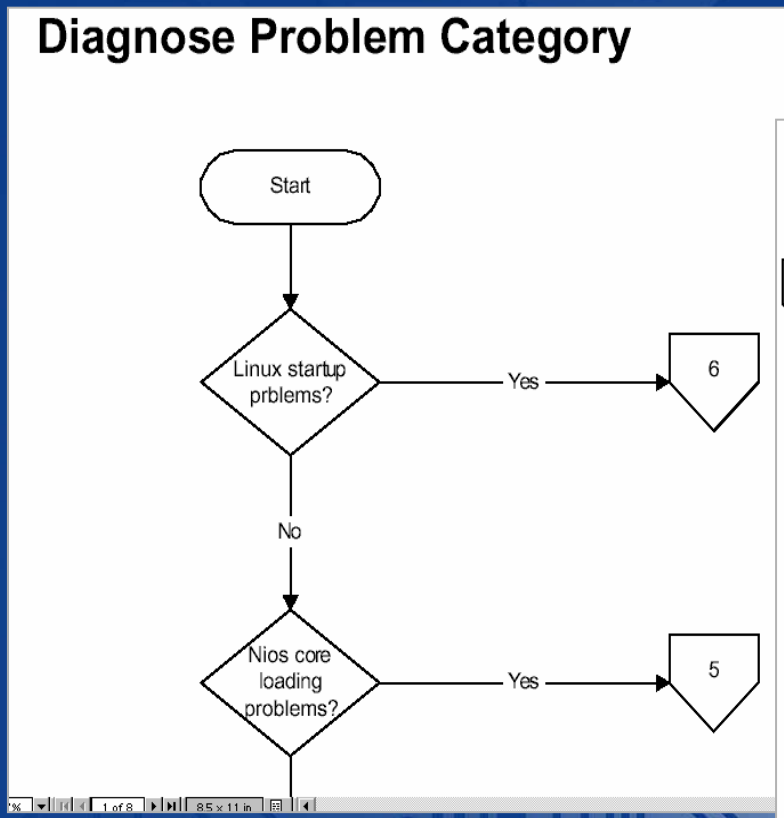
- NIOS-LINUX-KIT
  - $2,495
  - Shipping ***NOW***

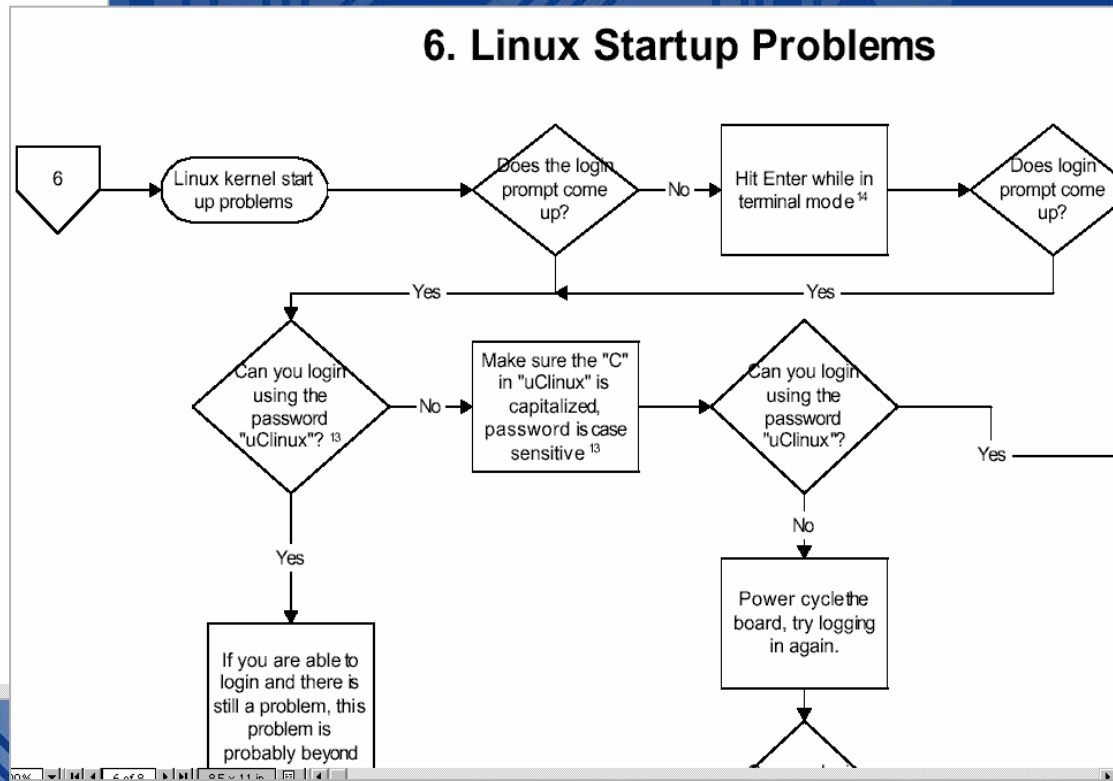
Support

- **Altera Applications**
  - Apps is the front line of support for LDK
  - Apps will provide install & basic “getting started” support
    - Altera supports LDK to the point a user gets a Linux prompt
  - Support for Altera devices
- **Microtronix**
  - 30 days install support
    - Go through Altera Applications first. May be referred to Microtronix.
  - Microtronix supports Linux design & development
    - $4750 for 12 months of Standard Support
      - **$4000 if purchase within 30 days of LDK**
      - Unlimited email support, next business day response
      - Six phone support incidents, next business day response
      - GNUPro Support
      - Upgrade Subscription – Linux and driver upgrades/patches
    - Other support options available

Support Flow

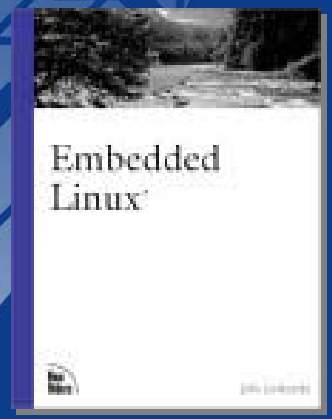
- There is a detailed support flow to guide Apps Engineers to a proper solution, or to pass customer on to Microtronix





uCLinux / Linux Resources

- www.linuxdevices.com
  - *Up-to-date, embedded-focused Linux info*
- www.uclinux.org
  - *Official uCLinux homepage, but a little out-of-date*
- www.oreilly.com
  - Offers a full range of Linux-related books
- *Embedded Linux* by John Lombardo - Good intro to embedded Linux issues for beginners
- "Three reasons why Linux will trounce the embedded market"
  - Article released on IBM developerWorks web site
    - http://www-106.ibm.com/developerworks/linux/library/l-emb.html?dwzone=linux



Simple OS Comparison

	ATI Nucleus	uCLinux	KROS
Price	$12,000 for Basic OS; Accessories (networking, etc) cost more.	$2,495 for LDK & source	$5,000
Business Model	Per-product license fee. Source code. No royalties.	Open source. No royalties. Cost of LDK is not for the OS. Linux profit model is based on service & support.	Per-product license fee. Source code. No royalties.
Real Time	Yes	No	Yes
Memory Requirements	20 KB and up	1 MB and up	7 KB and up
Support	Accelerated Technology Inc	Altera for install support only. Microtronix or 3rd party Linux Consulting for Linux design & devel support.	Shugyo Design Technologies

Glossary

- **MMU** – Memory Management Unit
  - A hardware block in complex microprocessors. Helps the CPU manage complex memory addressing schemes (Mapping virtual memory addresses to physical addresses)
  - Enables multiple programs to execute at the same time, and protects against illegal memory accesses. Especially helpful in OS-based systems.
  - Nios doesn't have an MMU. uCLinux is developed for MMU-less architectures.
- **RTOS** – Real Time Operating System
  - An operating system that can process "mission critical" tasks within a guaranteed maximum turn around time. (VxWorks)
    - Ex application: Car braking system, or industrial machinery motor control
- **Kernel** – "Linux kernel"
  - The lowest level software that runs on a processor. Interfaces directly with the hardware. Implementation is hardware dependent.
  - Provides a consistent, platform-independent interface to higher-level software
    - Ex: The application programmer doesn't have to think about how to operate a display device, a file system, or a network interface. They just work, thanks to the OS kernel.
- **DMA** – Direct Memory Access
  - Specialized circuitry or a dedicated microprocessor that transfers data from memory to memory (or from memory to a peripheral) without using the CPU. DMA may periodically "steal" cycles from the CPU, because both the CPU and the DMA cannot access the system bus at the same time. However, data is transferred much faster than using the CPU for every byte of transfer.
- **Nios** –
  - Nios is not an acronym. Gotcha!

Nios 2.0

Nios 2.0

- Optimized Data Processing
  - Custom CPU Instructions
  - >2X Acceleration (e.g. MAC, MP3, Bit Swap)
- Optimized Data Flow
  - Simultaneous Multi-master Bus Capability
  - Gbps Throughput
- On-chip Debug & Hardware Trace
- Smaller, Faster Nios CPU
- All existing Nios customers will get Nios 2.0
  - “Thank you” to our Nios early adopters
  - For all users present and future, 1 year Nios subscription starts from Nios 2.0 release

Custom Instructions

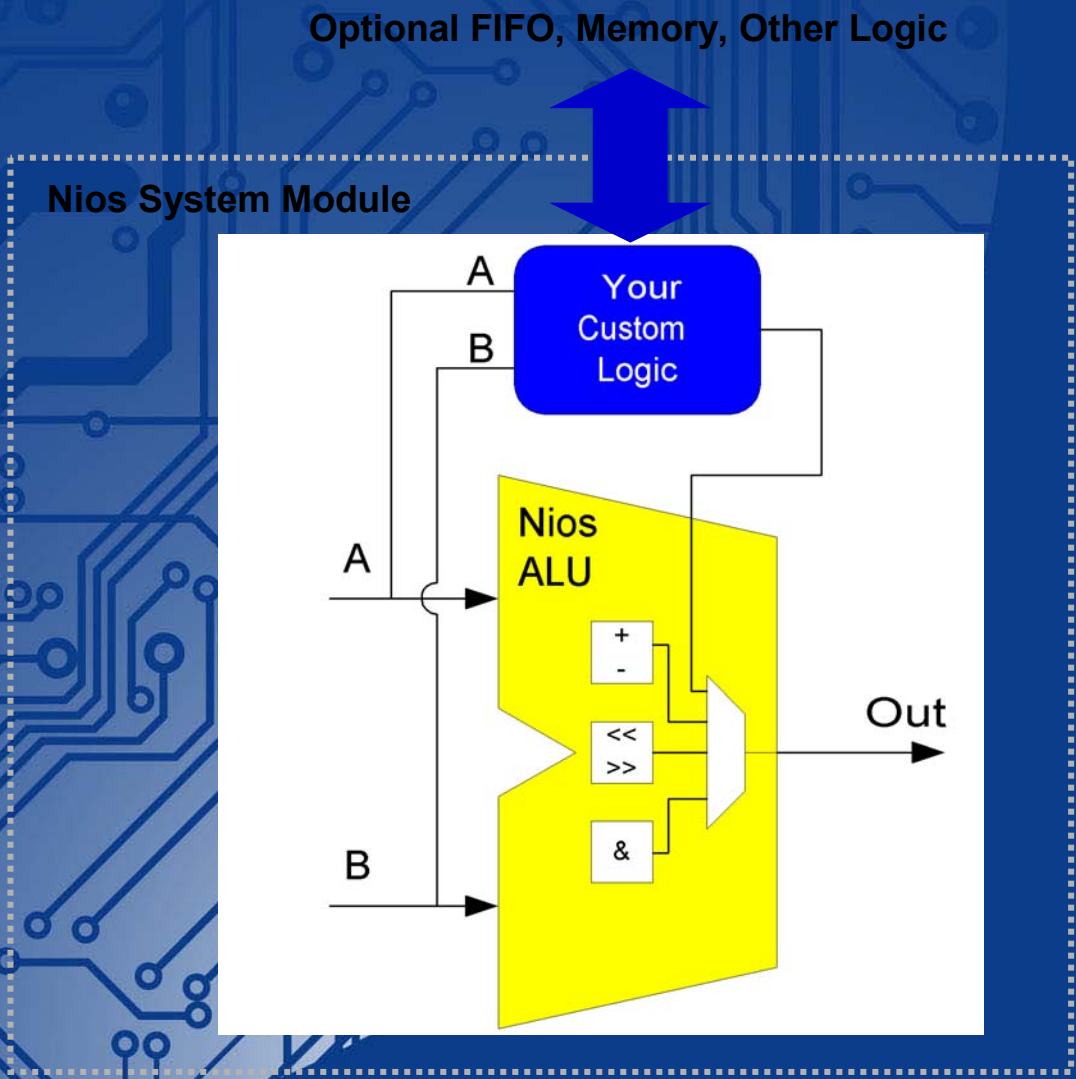
Optimized Data Processing

Custom Instructions

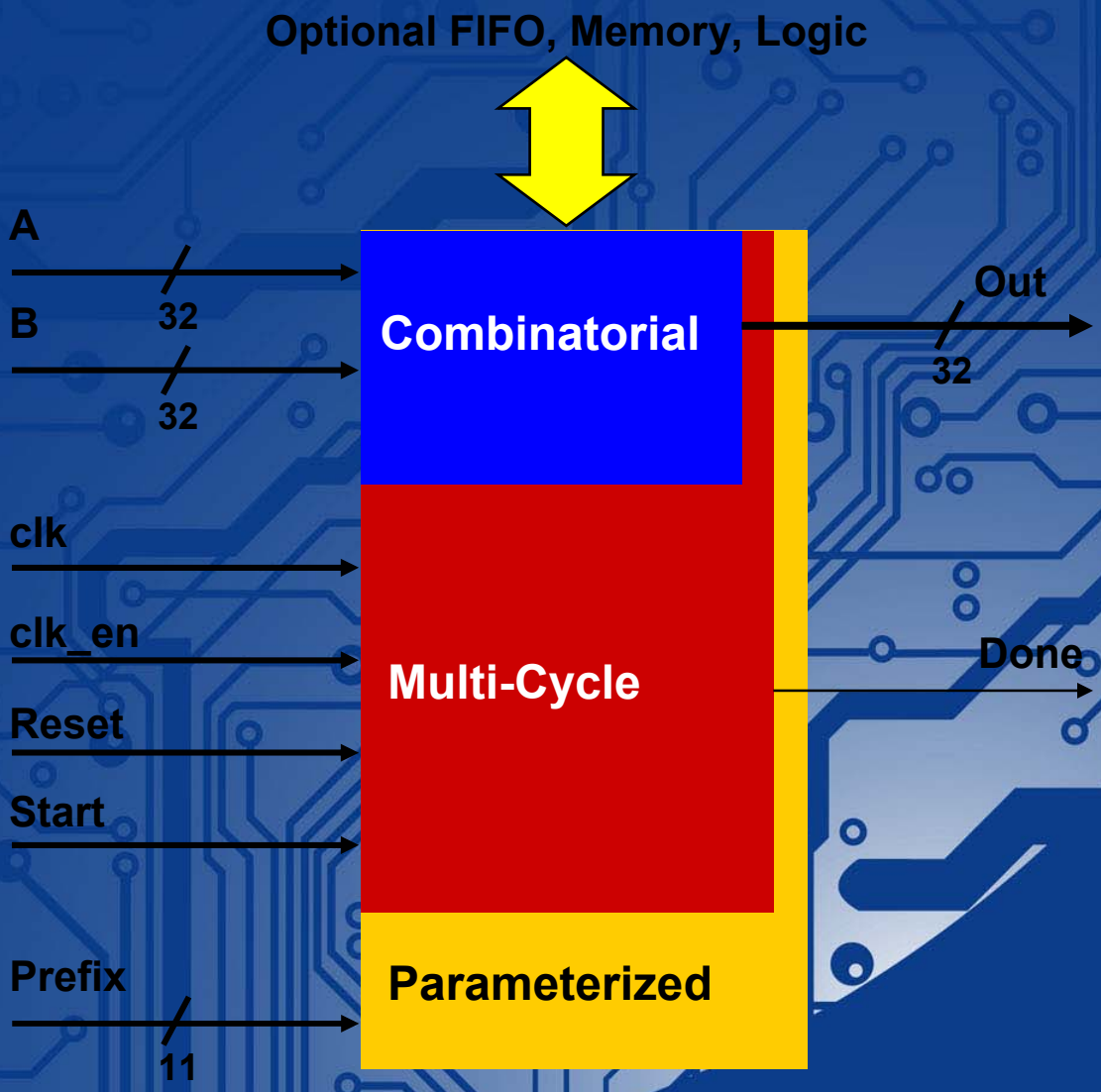
- Custom Instructions Augment Nios Instruction Set
- Integrated Into Nios Development Tools
  - System Builder Design Tool Handles Op-code Assignment
  - Generates C and Assembly-language Macros
- Application Examples
  - Data Stream Processing (E.G. Network Applications)
  - Application Specific Processing (E.G. MP3 Audio Decode)
  - Software Inner Loop Optimization

Custom Instruction Block Diagram

- Extends Nios Instruction Set
  - Up to 5 Instructions
- System Builder:
  - Adds User Logic to Nios ALU
  - Assigns Op-Code
  - Generates C & Assembly Macros



Three Levels of Customization



Real Custom Instruction Examples

- MP3 Audio Decode
  - Nios MP3 reference application implemented a crucial MP3 multiply-shift function in Custom Instruction
    - Enabled real-time MP3 decode at 33MHz
  - Achieved >2x increase in actual performance at 33MHz
- Endian Conversion
  - Swaps byte order in 32-bit word
    - `[DD CC BB AA]` to `[AA BB CC DD]`
  - Commonly required when transferring data between systems
  - 1 cycle using custom instruction, 20-40 cycles using normal RISC instructions

Custom instruction *always* reduces code size

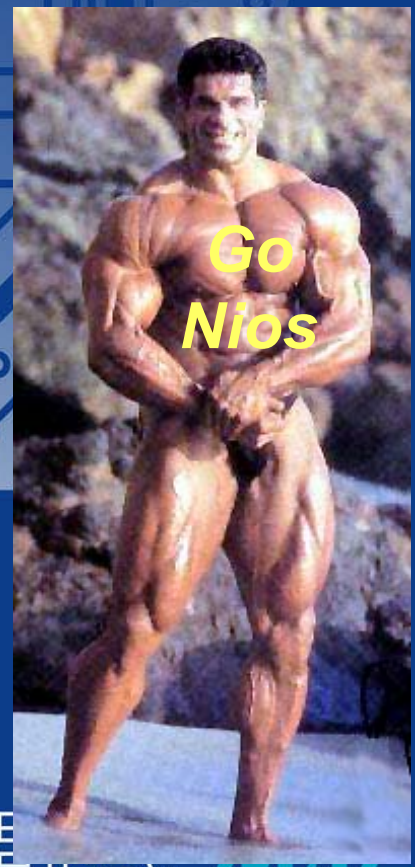
Custom instruction can dramatically increase system performance, ***regardless*** of Fmax

Simultaneous Multi-Master Bus

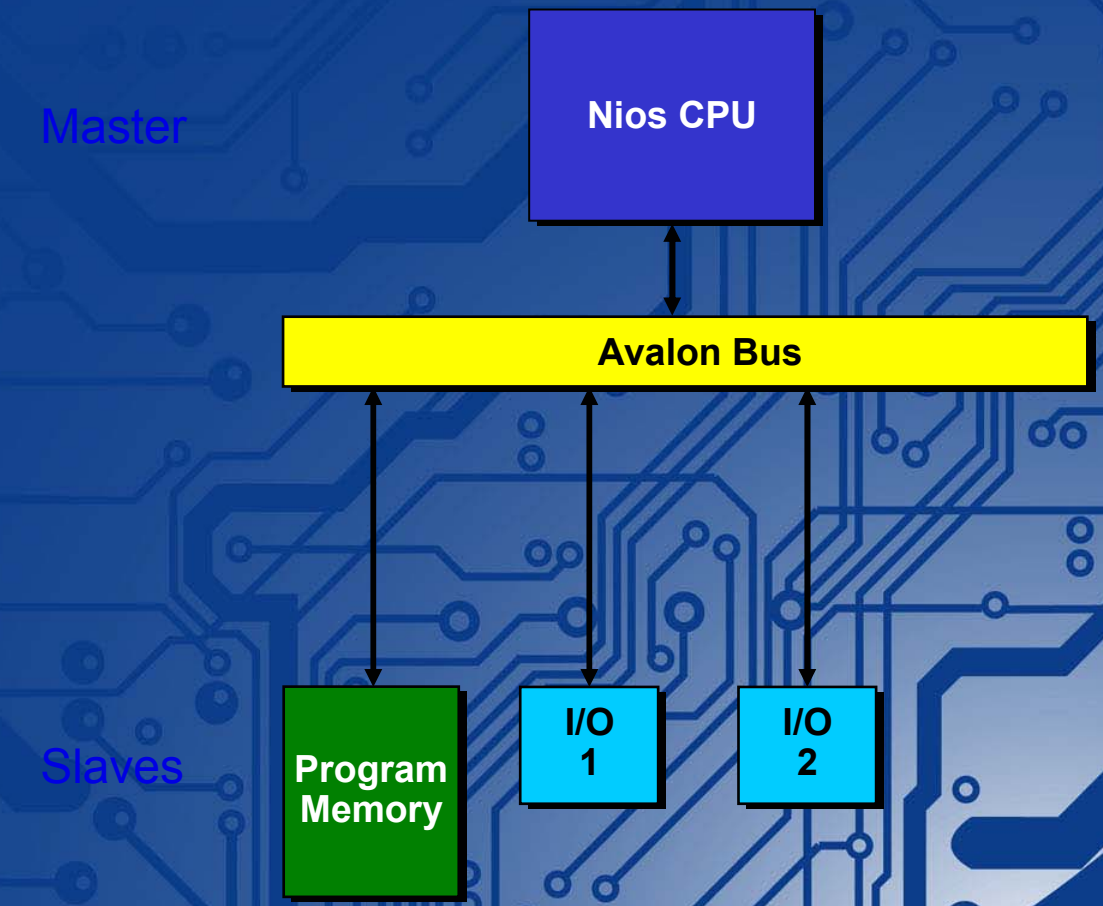
Optimizing Data Flow

Simultaneous Multi-Master Bus

- Allows multiple masters on a single Avalon bus
  - "Unlimited" Number of Bus Masters
- Masters can be active simultaneously as long as they don't access the same slave - "Slave side arbitration"
  - Only possible in PLD processors!
- "DMA on Steroids"
  - Simultaneous CPU & DMA Operation
  - New DMA Peripheral Converts Slaves To Masters
- High-Performance Data Flow
  - Peripherals Get Direct Access to Memory
  - Nios Performs Traffic Management
- Easy to Build
  - System Builder Generates Multi-Master Bus

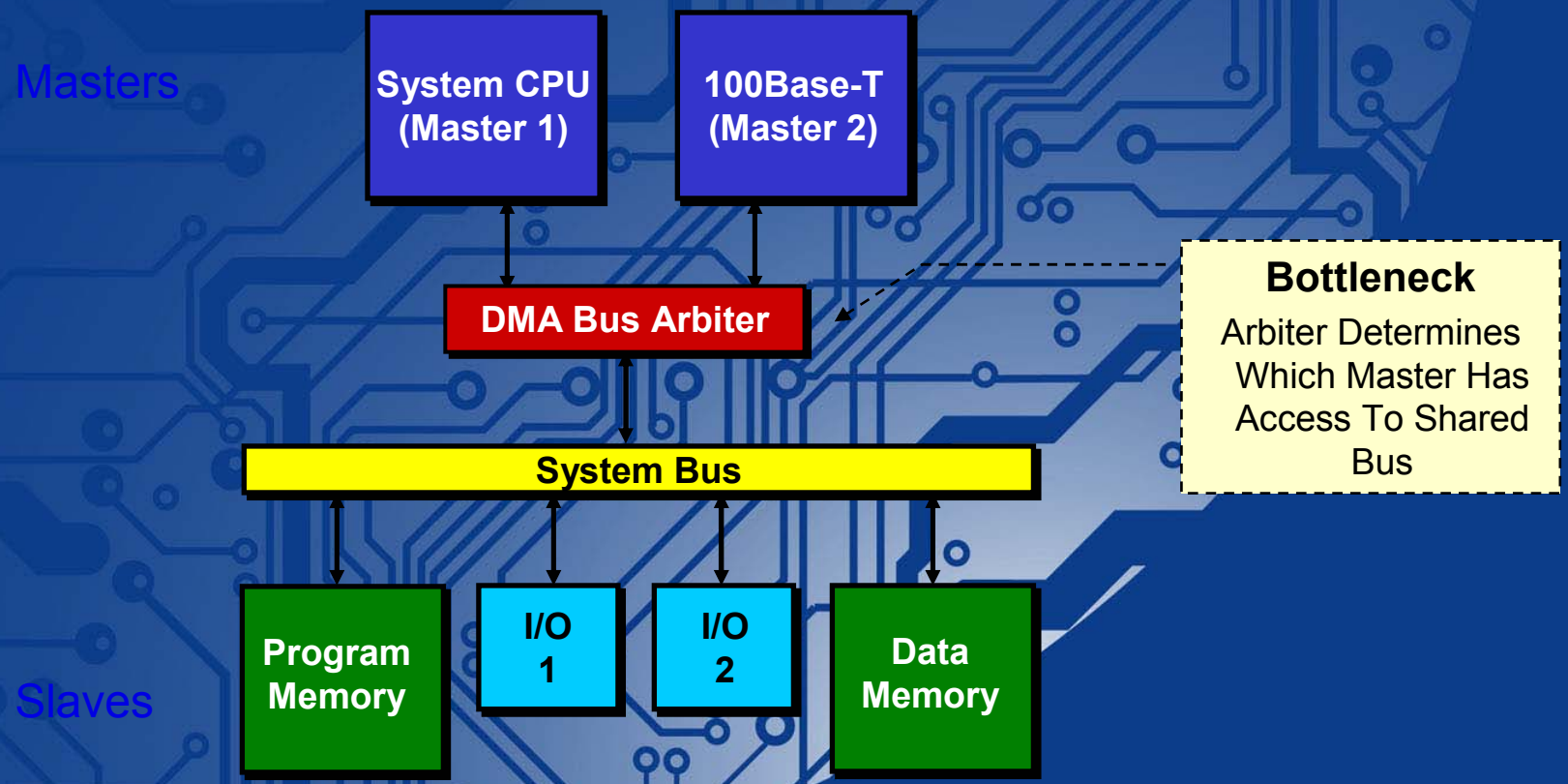


Nios 1.0 Bus Architecture

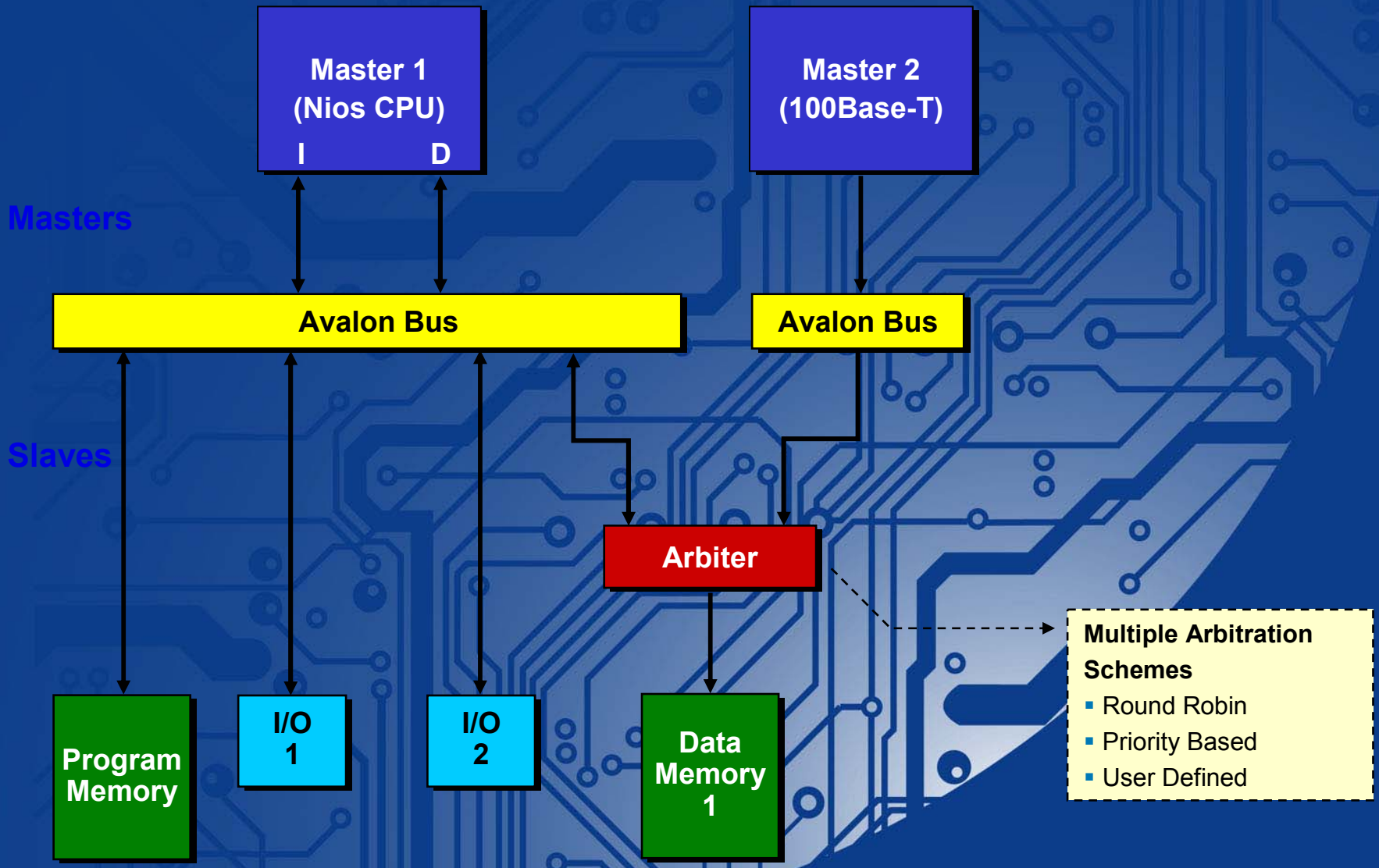


Traditional Data Flow for Multi-Masters

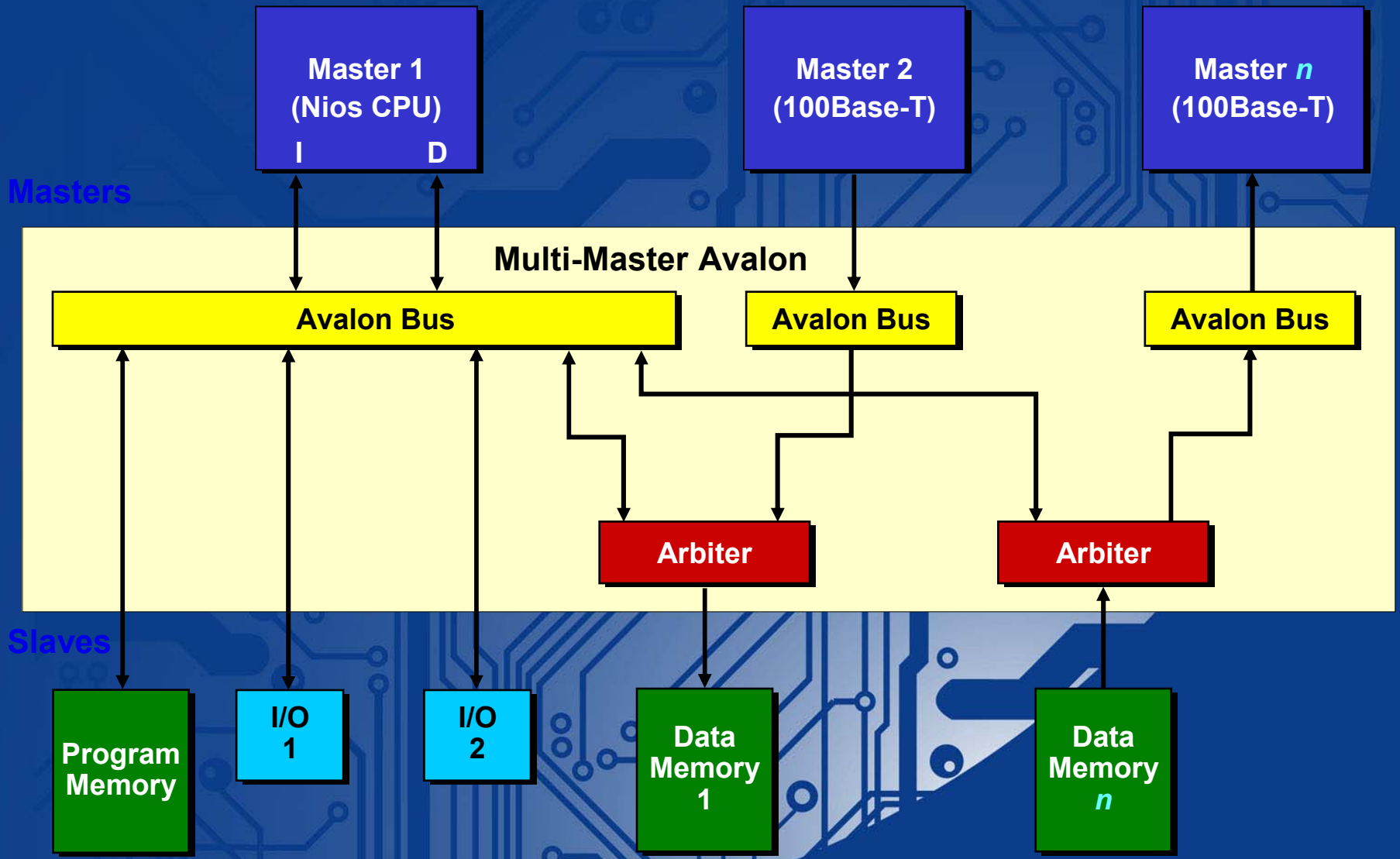
- Direct Memory Access (DMA)
  - Processor Waits For Bus During DMA



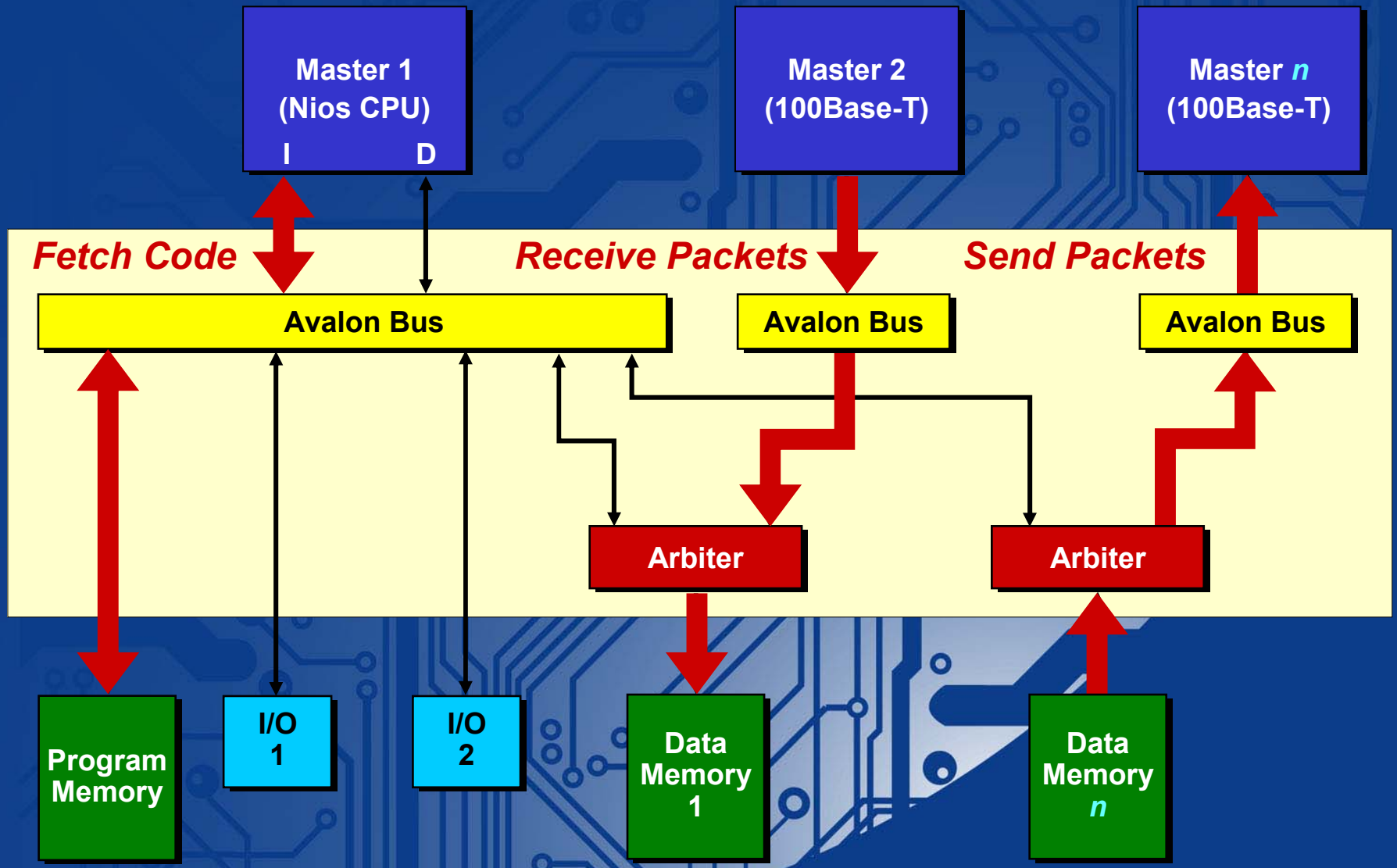
Simultaneous Multi-Master Avalon Bus



Simultaneous Multi-Master Bus

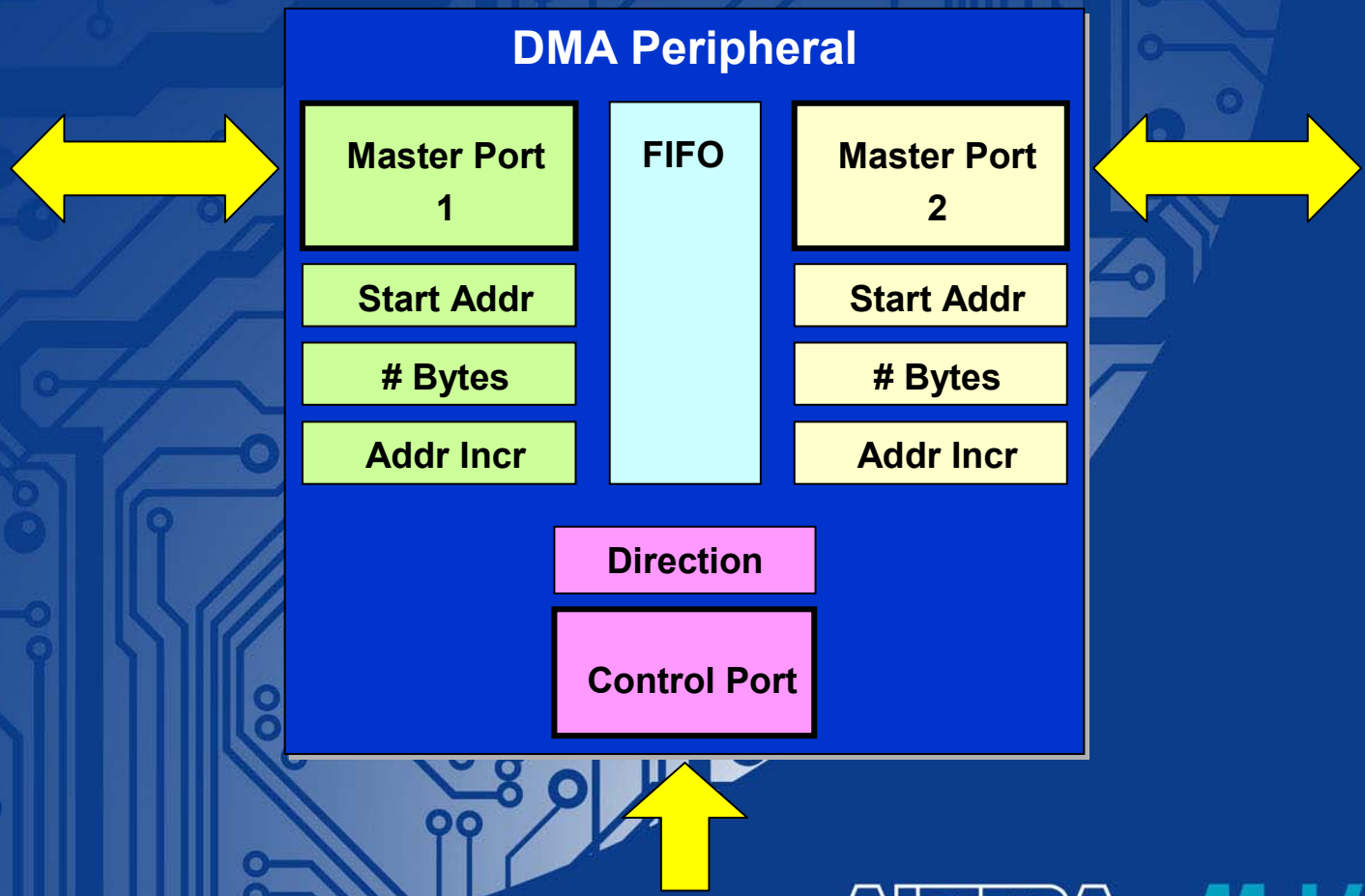


Simultaneous Multi-Master Bus

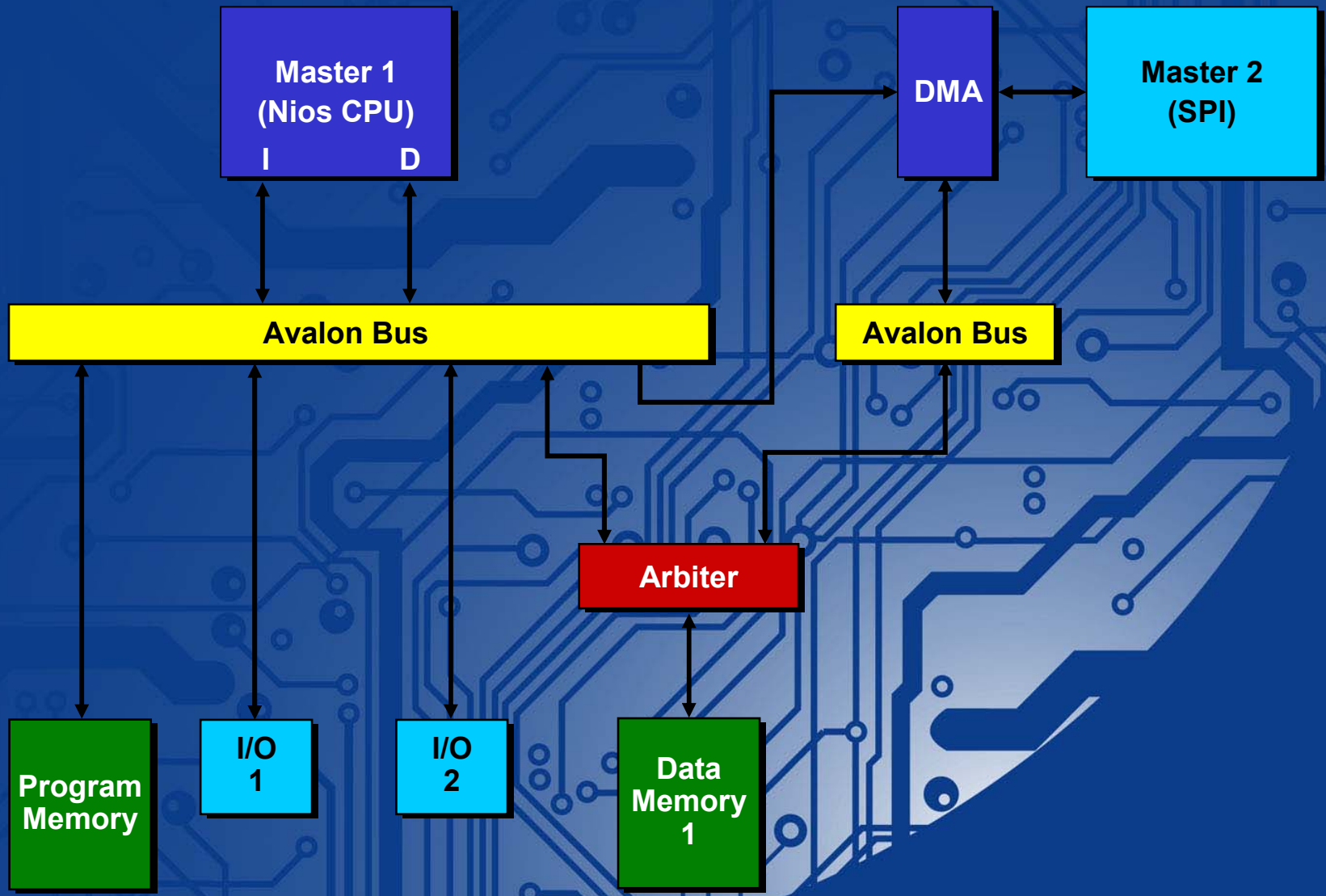


DMA Peripheral

- Provide Bus Master Capability to Any Nios Peripheral

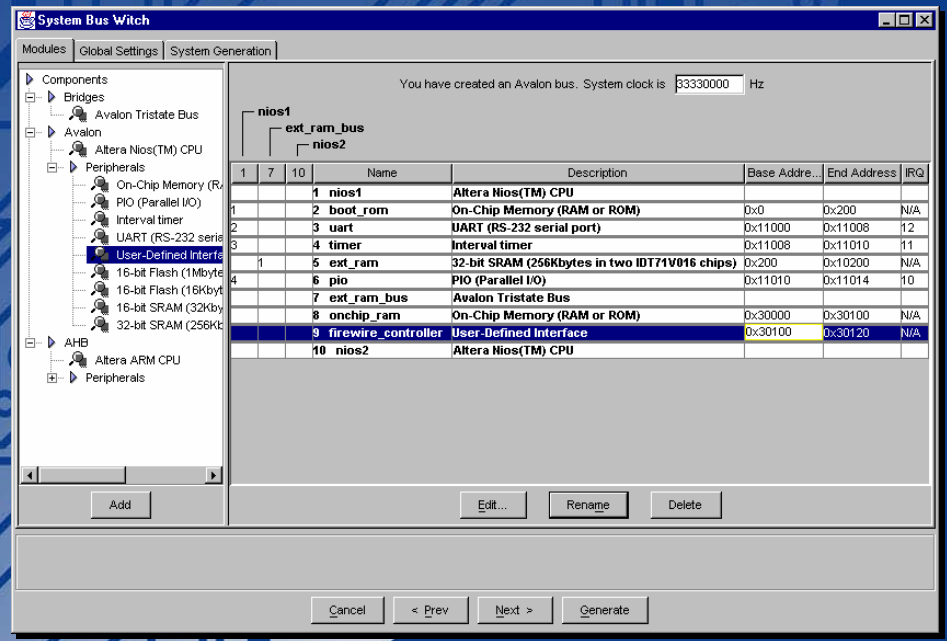


DMA Peripheral



System Builder Tool

- Automatically Configures System
  - Processor
  - Peripherals
  - Memory
- Builds Custom Bus
  - Master / Slave
  - Arbitration Priorities
  - Unlimited Number of Bus Masters
- Generates System
  - VHDL or Verilog



Price & Availability

- Price:
  - All Nios Users Get Upgrade at No Cost
  - Nios 2.0 Features Included in $995 Kit

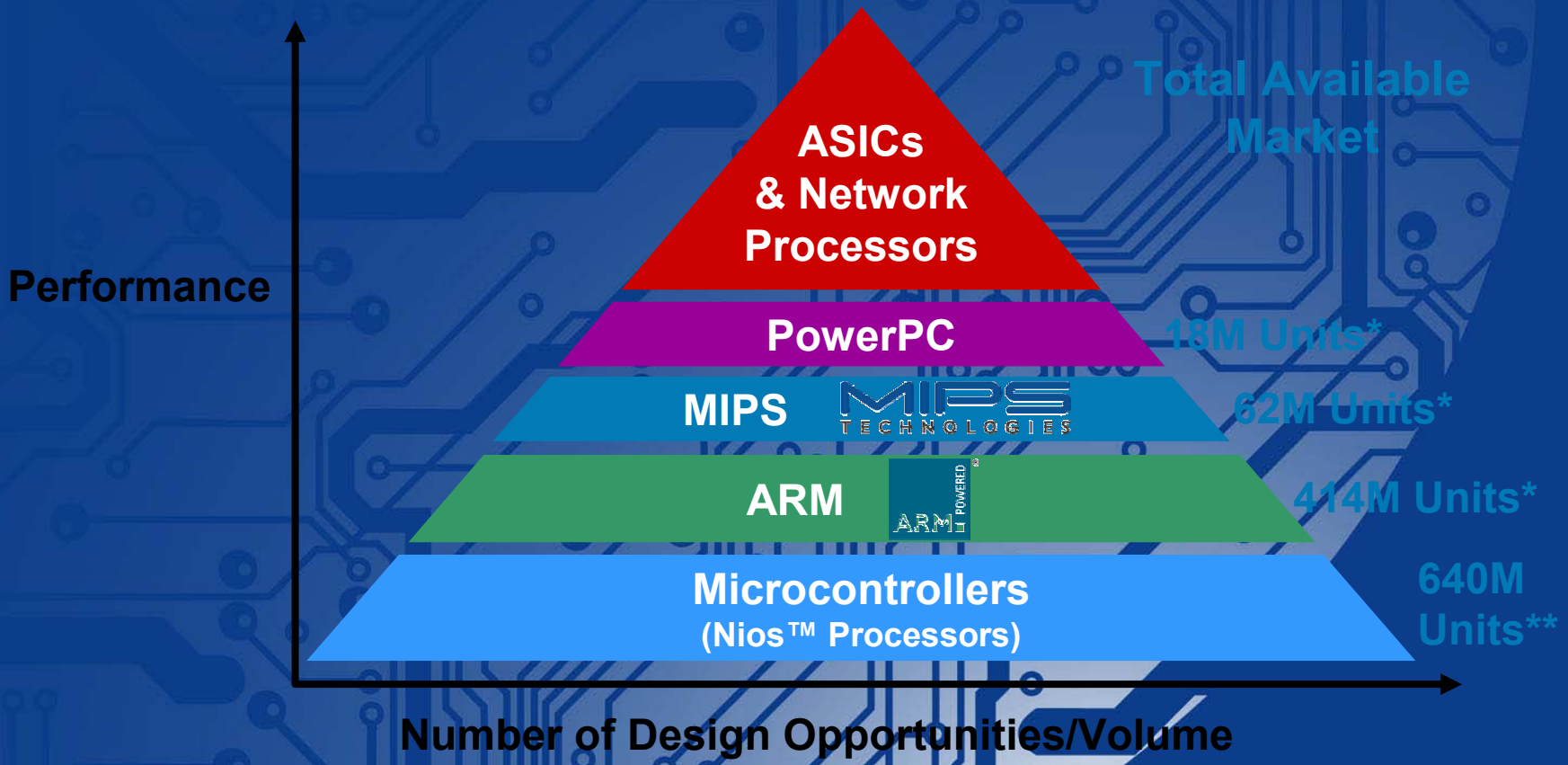
- Availability:
  - Alpha (to FAEs) – October 22
  - Beta (to Limited Customers) – November 21
  - Upgrade Posted on FTP Site – December 6
  - Upgrade to Customers – December 17

Competitive Comparison

Microcontroller Competition

- Companies Now Using Nios Formerly Used Products Such as:
  - Motorola (68000, 683XX, MPC8XX, 68HCXX)
  - Intel (i960, StrongARM)
  - Hitachi (SHX, HX)
  - Philips (XA)
  - Zilog (Z80)
  - Many (8051)

Embedded Market Overview



*2000 Shipments, Microprocessor Report
**2000 16-Bit & 32-Bit MCU Shipments, Instat

ARM estimates 30M to 40Mu of Year 2000 shipments will be in networking / telecom applications

Microcontroller Market Drivers

Microcontrollers
(Nios™ Processors)

640M Units**

- In rank order *
  - Software Development Tools
  - Price
  - Available I/O (Peripherals)
  - Speed

*** 2000 Embedded Systems Programming Subscriber Study**

Microcontroller Landscape

32 Bit

32-Bit Microcontrollers					
Nios -32	Hitachi SHX	Intel i960	Motorola 683XX	Motorola M-CORE	Motorola PowerPC 8XX
$4 - $42	$25-$100	$10-$50	$5-$100	$10-$25	$50-$100
33 to 80	60 to 200	10 to 100	33	10 to 33	40 to 80

16 Bit

16-Bit Microcontrollers					
Nios -16	Hitachi H8S	Motorola 68HC12	Motorola 68HC16	Philips XA	Siemens 80C166/167
$4 - $42	$10-$25	$10-$25	$5-$50	$2.5-$10	$2.5 to $25
33 to 80	20 to 25	8.5	16 to 25	33	26 to 25

8 Bit

8-Bit Microcontrollers					
Nios -16	Hitachi H8	Microchip PIC 16	Microchip PIC 17	Motorola 68HC11	Philips 80XX, 80CXX
$4 - $42	$5-$10	$1-$5	$5-$10	$2.5-$10	$2.5-$5
33 to 80	8 to 16	20	33	2 to 4	33

Microcontroller Feature Set

	Data Path	SDRAM	SSRAM	Flash	ROM	DMA	Chip Select	Ext Interrupts	UART	SPI	I2C	CAN	IR	Ethernet	HDLC	GPIO	IDE	ISA	PCI	Centronis	LCD	PWM	Clock out	PLL	MAC	Timers	Counters	Watchdog	RTC
Nios	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
Hitachi SHX	32 √	√	√	√	√	√	√	√	√	√						√			√		√			√	√	√	√	√	√
Intel I960	32	√	√	√	√	√		√			√		√						√								√	√	
Motorola 683XX	32 √	√	√	√	√	√	√	√	√	√			√	√	√	√					√	√	√	√		√	√		√
Motorola M-Core	32 √		√	√	√		√	√	√	√			√			√						√	√	√		√	√	√	√
Motorola PPC	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√			√		√			√	√	√	√	√	
Hitachi H8S	16	√			√	√				√		√	√			√						√				√		√	√
Motorola 68HC12	16		√		√	√	√	√	√	√		√				√					√	√		√		√	√	√	√
Motorola 68HC16	16		√		√	√	√	√	√	√						√						√		√	√	√	√	√	√
Philips XA	16	√	√	√	√	√	√	√	√		√					√							√				√	√	√
Siemens 80C166	16						√	√	√	√	√	√				√						√		√		√	√	√	√

Memory IF | Serial I/O | Parallel I/O | Special Purpose | Timers

ALTERA® MJL®

Configurable Processor Comparison

- ARC and Tensilica
  - Processors Optimized for ASIC Implementation
  - Very Large and Slow When Implemented in PLDs
- Nios Is Optimized for Use in Altera PLDs
- Nios Is 2.5X to 7X Smaller

	ARC Core w/2KB I-cache Altera EP20K400E	Tensilica core w/cache/RAM/ROM Altera EP20K400E	Nios core 32-bit version Altera EP20K400E
Logic Elements (LE's)	3,400	9,000	1,250
% of Device	20%	54%	7.6%
ESB's/RAM	26Kb	37Kb	-
Typ. Freq.	35 MHz	40 MHz	42 MHz

Other Competitive Soft Cores

- Leon 2
  - Open source CPU
  - Not PLD friendly
  - No Megawizards
  - Who supports it?
  - Patent Issues?
    - Based on Sun SPARC
  - Info:
    - www.gaisler.com/leon.html
- MicroBlaze
  - Xilinx
  - Beta Release

Technology	Area	Timing
UMC 0.25 CMOS std-cell	35K gates + RAM	130 MHz (pre-layout)
Atmel 0.25 CMOS std-cell	33K gates + RAM	140 MHz (pre-layout, log file)
Atmel 0.35 CMOS std-cell	2 mm2 + RAM	65 MHz (pre-layout, log file)
Xilinx XCV300E-8	4,800 LUT + block RAM	45 MHz (post-layout)
Xilinx XCV800-6	4,800 LUT + block RAM	35 MHz (post-layout, log1, log2)
Altera 20K200C-7	5,700 LCELLs + EAB RAM	49 MHz (post-layout) log file
Altera 20K200E-1X	6,700 LCELLs + ESB RAM	37 MHz (post-layout) log file

Example Design – A Typical CPU

Design Component	32-Bit	16-Bit
Registers	256	128
Data Bits	32	16
Address Bits	21	16
Shifter	7-Bit	3-Bit
H/W Multiplier	None	N/A

Example Design - Peripherals

Peripheral	Configuration
LCD	PIO: 11-Bit Output
LED	PIO: 2-Bit Bi-Directional
7-Segment LED	PIO: 16-Bit Output
Buttons	PIO: 12-Bit Input
Timer	32-Bit
UART	Fixed Baud 115200
Memory	32-Bit / 16-Bit SRAM (256K/32K)
Memory	16-Bit Flash (1MB / 16K)
On-Chip ROM	1K with Boot Monitor

Example Design – Size / Speed

Device Family	32-Bit		16-Bit	
	LE	Fmax	LE	Fmax
Mercury	2602	59.08	1784	70.51
APEX II	3046	55.44	2144	59.34
APEX 20KC	3022	53.15	2124	54.09
APEX 20KE XA	3035	43.26	2151	44.50
FLEX 10KE	3029	32.47	2103	38.82
ACEX 1K	3042	31.35	2119	38.31

Soft-Core Competition - Xilinx

Nios

- 16-Bit Instruction Set
  - Small Code Size
  - Uses Popular 16-Bit Flash
- Device Support
  - ACEX & FLEX 10KE
  - APEX, APEX 20KC, APEX II
  - Mercury
  - Excalibur ARM
  - MPLD
- ASIC License Available

MicroBlaze

- 32-Bit Instruction Set
  - Large Code Size
  - Requires two 16-Bit Flash Devices
- Device Support
  - Virtex-E, Virtex-II
  - Spartan-II
- ASIC License ?

Soft-Core Competition - Xilinx

Nios

- Windowed Register File
  - Configurable to 512 Registers
  - Fast Context Switching
- Interrupts
  - Integrated Controller
  - 64 Vectored Interrupts
- Peripherals:
  - UART
  - Ethernet
  - PWM
  - IDE
  - SRAM
  - Flash
  - DMA
  - SPI
  - Timer
  - PIO
  - User-Defined
  - SDRAM
  - Compact Flash
  - OCD

MicroBlaze

- 32 Registers
  - Stack Overhead for Subroutine Calls
- Interrupts
  - External Add-On Peripheral
- Peripherals:
  - UART
  - Timer/Counter
  - PIO
  - Arbiter
  - Flash, SRAM
  - Interrupt Controller

Soft-Core Competition - Xilinx

Nios

- Customization Instruction
  - Up to 5 Per Processor
    - Combinatorial
    - Sequential
    - Parameterized
  - Supports External Interface
    - FIFO, Memory
    - External Logic
  - Generates Software
    - Assembly Macro
    - C Macro

MicroBlaze

- Custom Instruction
  - *None*

Soft-Core Competition - Xilinx

Nios

- Development Kit
  - Complete Kit ($995)
    - Processor & Peripherals
    - Development Board
    - Compiler, Assembler
    - Debugger
    - Quartus II Limited Edition
    - Download Cable
    - Documentation
    - Reference Designs
    - Tutorial

MicroBlaze

- Development Kit
  - Kit 1 ($495)
    - Processor & Peripherals
    - Compiler, Assembler
    - Debugger
  - Kit 2 ($?)
    - Processor & Peripherals
    - Compiler, Assembler
    - Debugger
    - Development Board
    - Xilinx ISE

Soft-Core Competition - Xilinx

Nios

- Operating System Support
  - ATI Nucleus
  - Linux
  - KROS
- Software IDE
  - Viosoft Arriba!
    - Edit
    - Compile
    - Download
    - Run
    - Debug
    - Hardware Breakpoints
    - Software Trace

MicroBlaze

- Operating System Support
  - *None*
- Software IDE
  - *None*

Customer Feedback - MicroBlaze

- Competitive Situation
  - XA10 With Four 32-Bit Nios I/O Processors
  - Evaluating MicroBlaze
    - Excited About 125MHz Spec
- Customer Comments
  - Disappointed in MicroBlaze
  - Nios Has Better Complier Solution
  - Realized Xilinx Speed Claims Are Marketing Hype
    - 125MHz Requires *Internal* Program Memory

3rd Party Developer Momentum

- Microtronix Linux Development Kit
- ATI Nucleus
  - Popular embedded RTOS & Development environment
- Shugyo KROS
  - RTOS with very small memory footprint
- Viosoft Arriba!
  - Complete Integrated Development Environment (IDE)
    - First vendor to support Nios 2.0 On-Chip Debug
- 3rd party software & tool vendors give validity to the Nios platform

Nios Positioning

- Nios is in 2nd generation, and ***1 year*** in the lead
- Xilinx MicroSmoke is just out of the starting gate (not even)
- Hardware alone does not a system make
  - Peripherals, documentation & reference designs are crucial pieces of a microprocessor solution – And Altera has it
- Custom instruction capability
  - Even a mid-performance 32-bit Nios can be a processing powerhouse
    - MIPS & Fmax become meaningless
  - Nios now offers “advanced configurable processor” features
    - Look out Arc and Tensilica
    - And we can license for ASIC too
- Simultaneous Multi-Master Avalon Bus
  - Even a mid-performance 32-bit Nios can be a Gbps throughput powerhouse
    - MIPS & Fmax become meaningless
    - Traditional PLD features (configurable routing) offer *real* advantages in embedding a processor in an SOPC

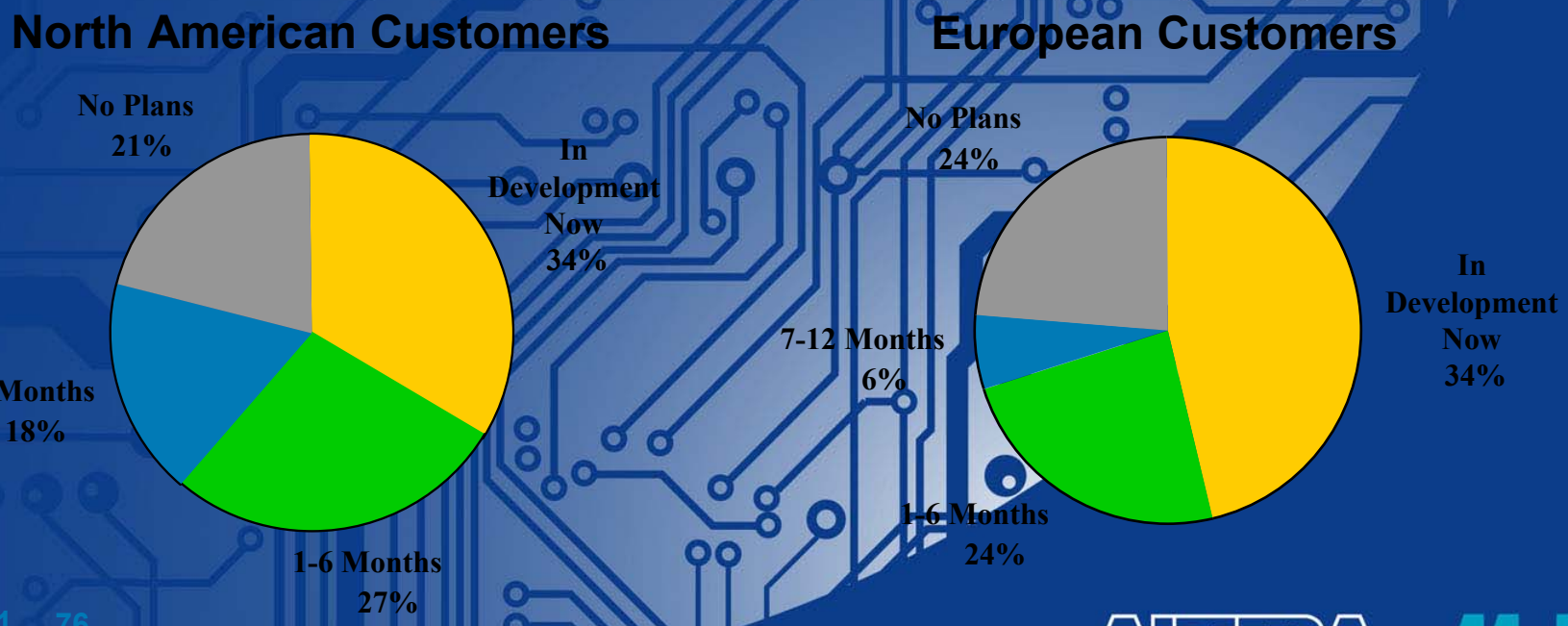
Summary

- Quartus II Limited Edition is shipping to all Nios customers
- PCI32 Nios Target ships in October 2001
- Ethernet Development Kit is shipping today
- Linux Development Kit is shipping today
- Custom Instruction enables optimized data processing
  - >2x performance and smaller code
- Simultaneous Multi-master enables optimized data flow
  - Nios becomes a throughput powerhouse regardless of Fmax
- Nios' primary competition is standard microcontrollers
- Nios has a 1 year lead on MicroBlaze
  - 3rd party software & tools momentum, reference applications, documentation, experience
- MicroBlaze is nothing but MicroSmoke until it releases
  - Preliminary analysis suggests MicroBlaze will have no significant advantage over Nios

Design Examples

Nios Is Winning Designs Today

- First 10 Months
  - Over 2500 Development Kits Sold
- Customer Survey Results
  - Active Designs



Nios Kit Customers (Partial List)

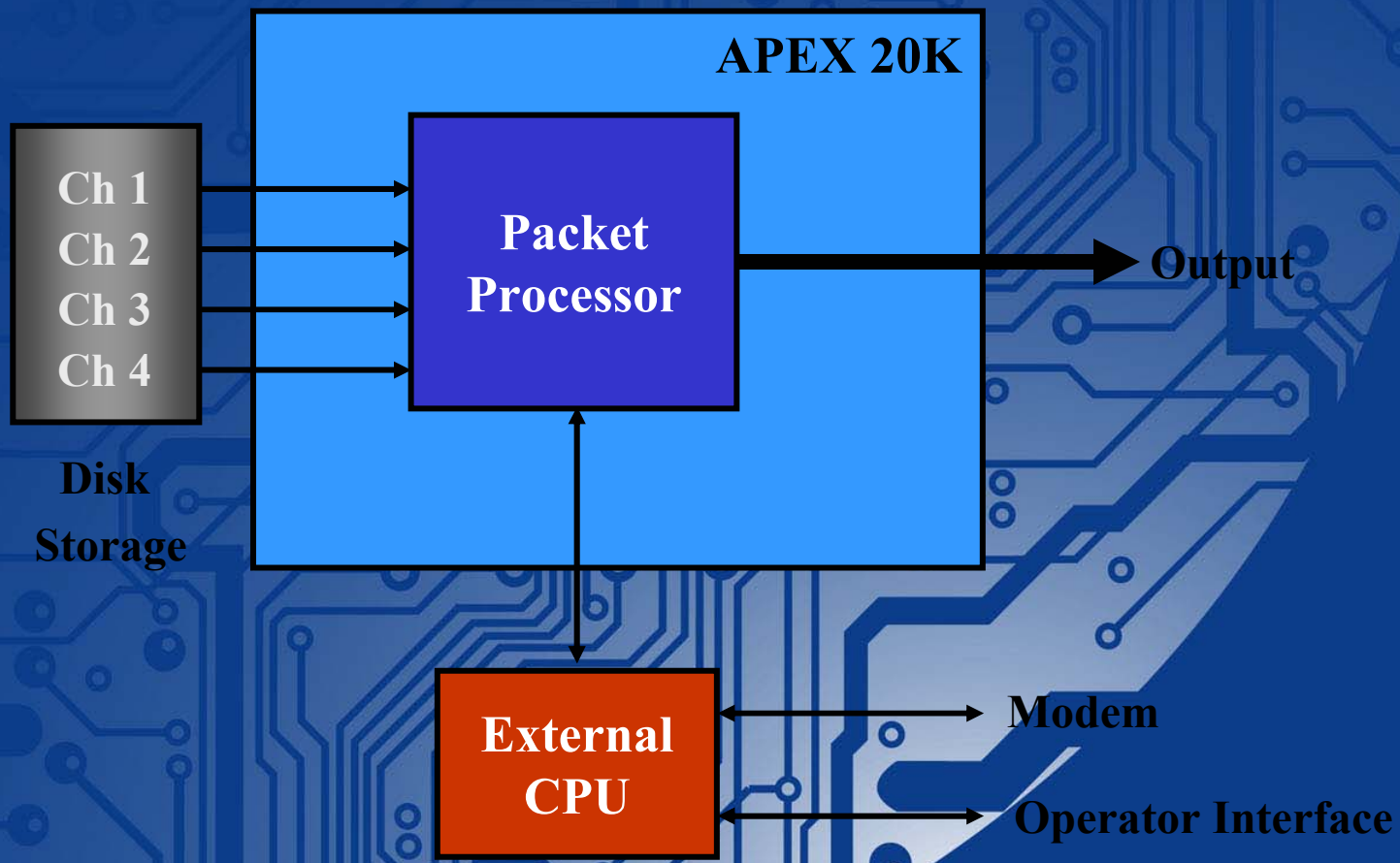
- Agilent
- Boeing
- Bosch
- Canon
- Casio
- Cisco Systems
- Eastman Kodak
- EMC
- Fujitsu
- General Instrument
- Hewlett Packard
- Hitachi
- IBM
- LM Ericsson
- Lucent Technologies SAS
- Matsushita
- Matsushita Communications
- Motorola
- Motorola Communications
- NEC
- Nintendo
- Nokia Telecommunications
- Nortel
- Philips Research
- Philips Business Communications
- Philips Multimedia
- Rockwell
- Sanyo
- Sharp
- Siemens
- Siemens Information & Communications
- Sony
- Thomson
- Toshiba

Why Customers Use Nios

- Technical Issues
  - Easy to Implement Complex State-Machine
  - Provide General Housekeeping/Management Functions
  - I/O Processing
  - Off-Load Existing Processor
  - Remote PLD Configuration (e.g. Internet Reconfiguration)
- Business Issues
  - Save Cost by Reducing System Chip Count (System-on-a-Programmable Chip)
  - Allocation-Proof Processor
  - Feature Upgrades Extend Product Life

Commercial Entertainment System

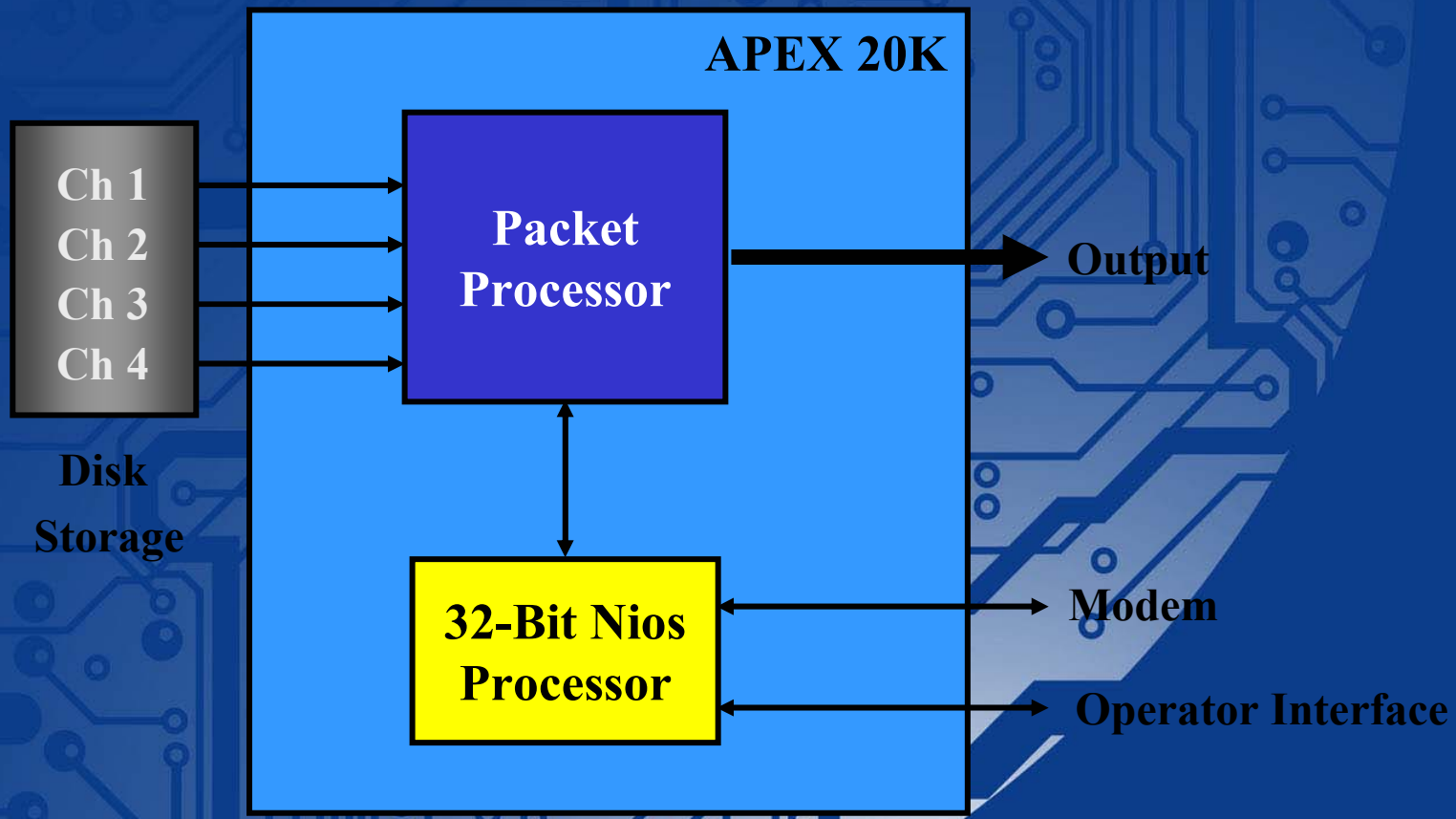
Before Nios



Expensive External Processor

Commercial Entertainment System

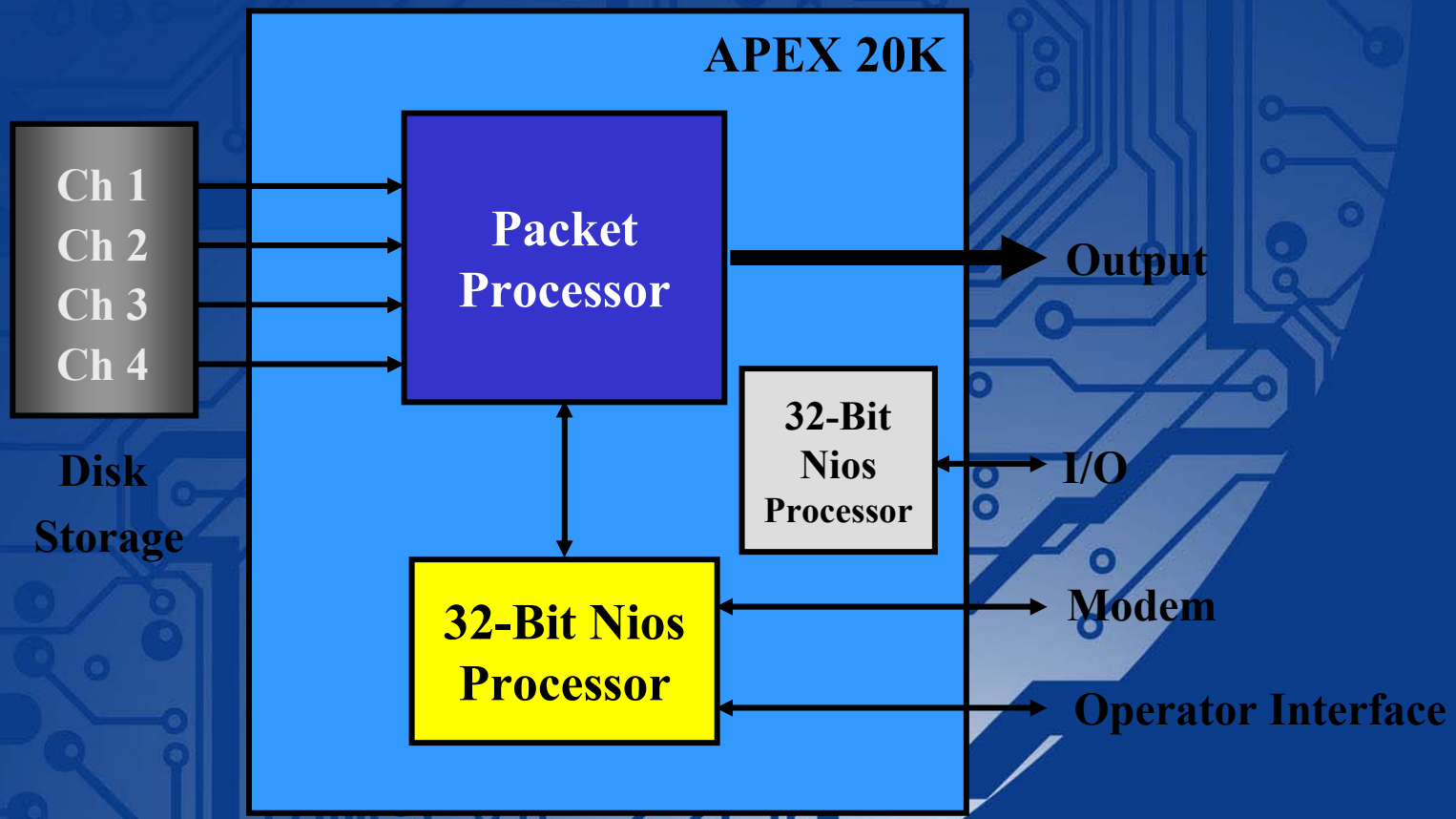
After Nios



Replaced External CPU, Lowered Production Cost

Commercial Entertainment System

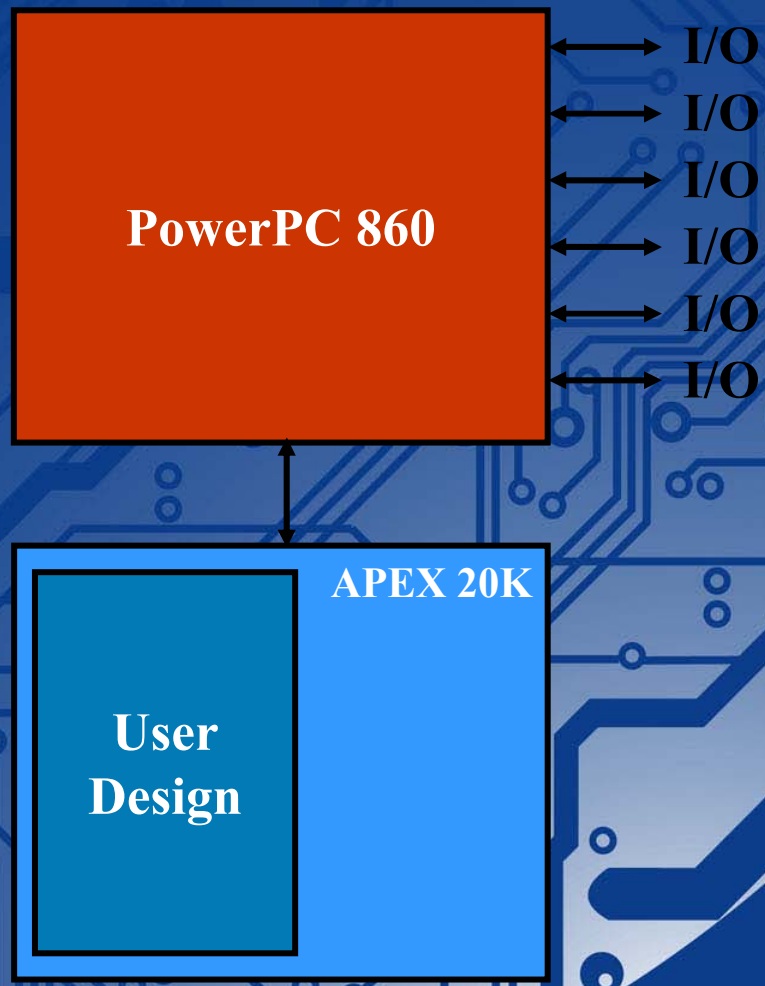
After Nios



Scalable Performance, Extended Product Life

Network Communication System

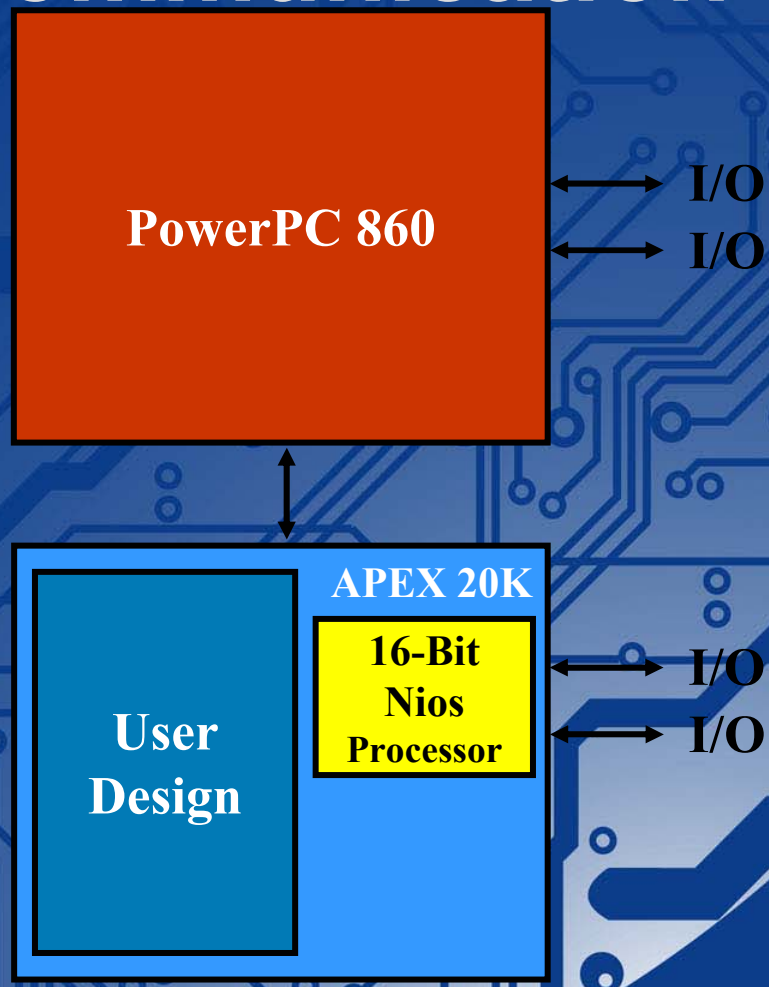
Before Nios



Processor Performance Limited by I/O Processing

Network Communication System

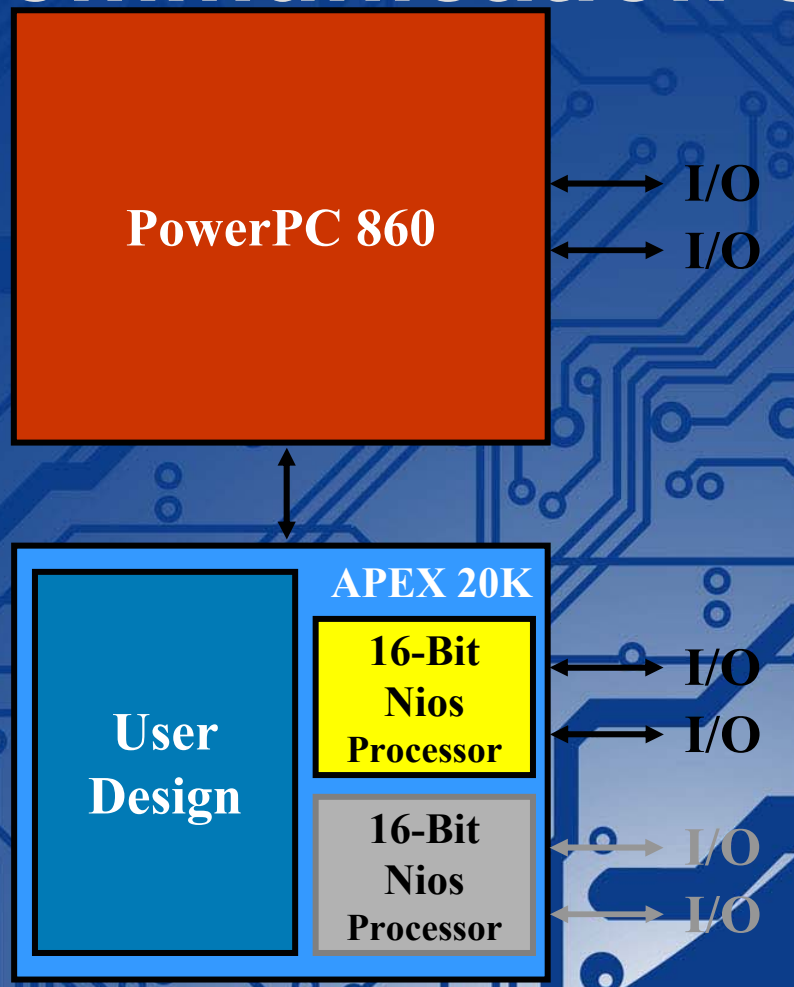
After Nios



Offload Existing Processor with Nios "IO Processor"

Network Communication System

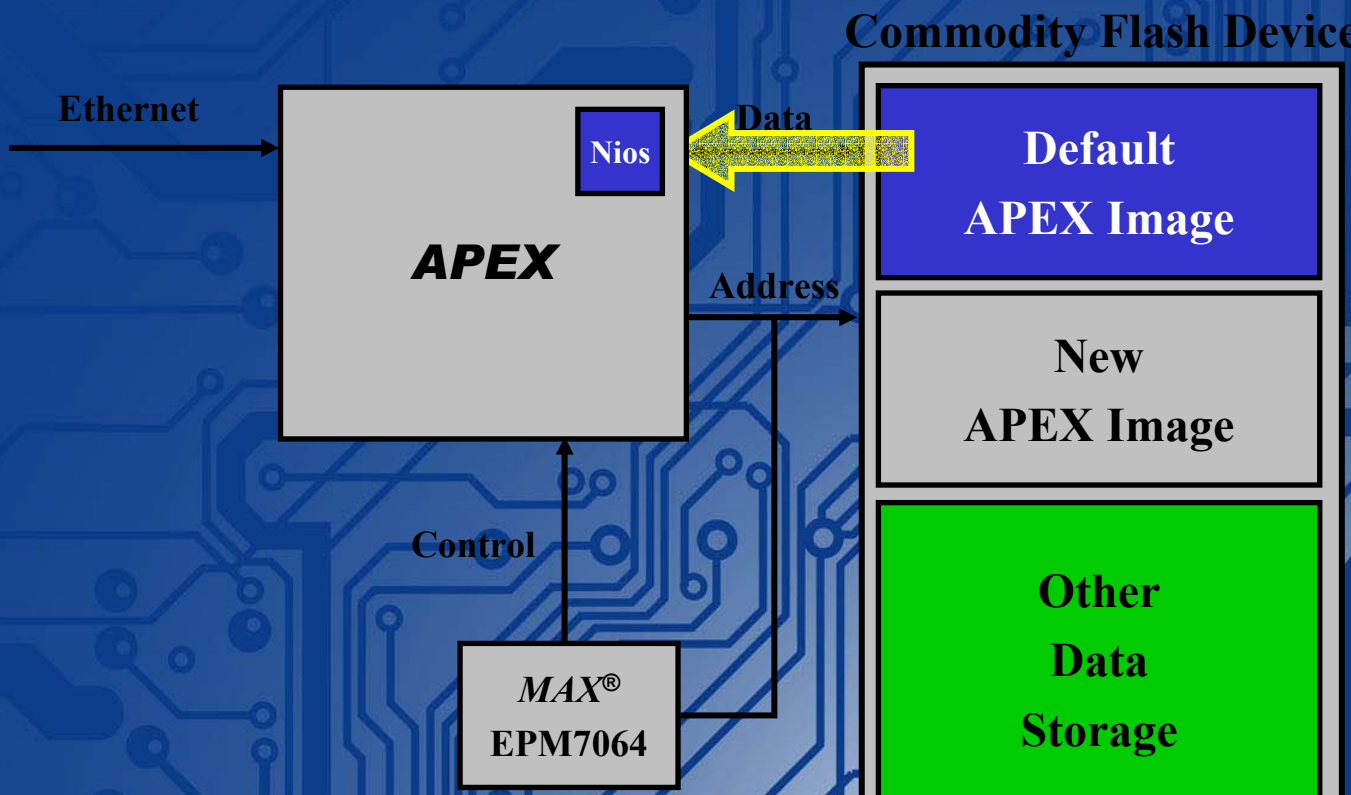
After Nios



Scalable Performance, Add I/O Processors As Needed

Remote Reconfiguration

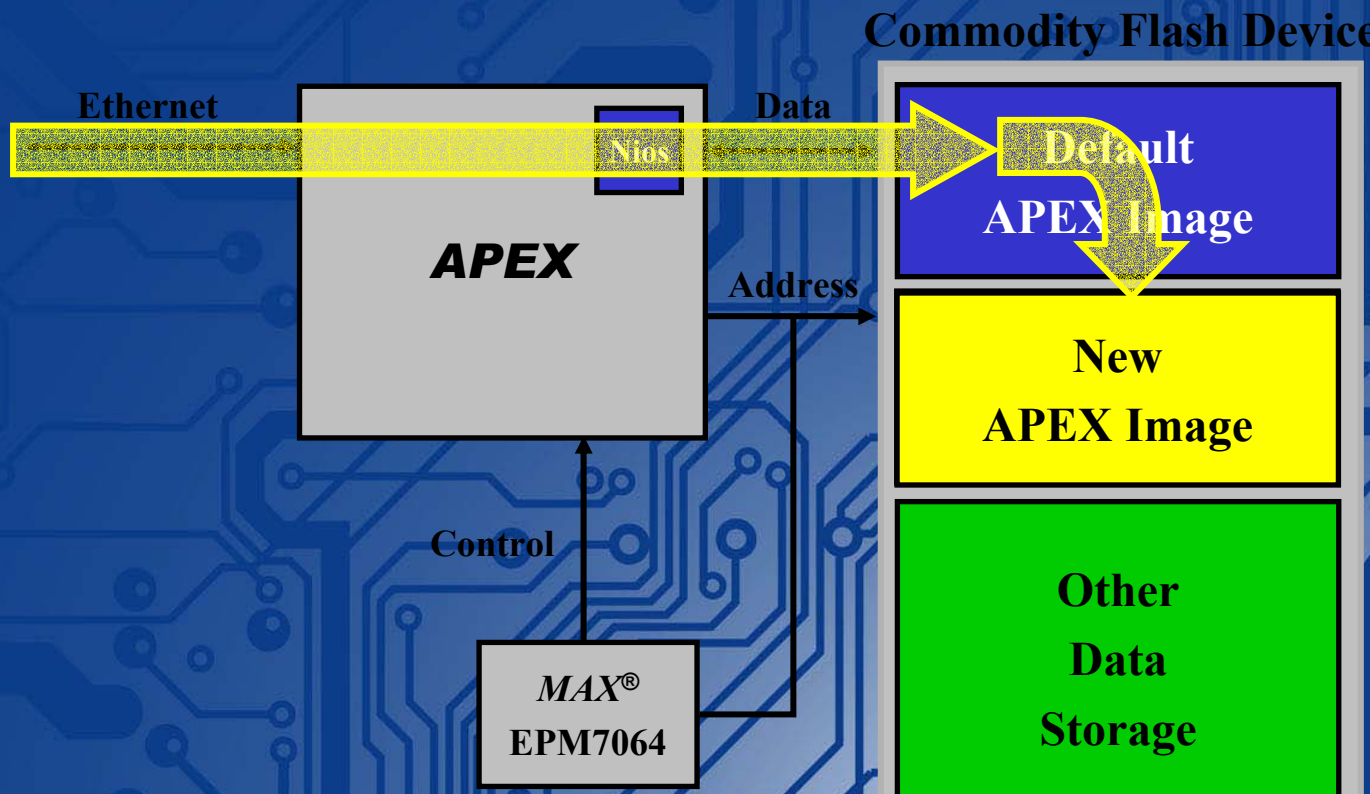
On Power Up



"Default APEX Image" Configured from Commodity Flash

Remote Reconfiguration

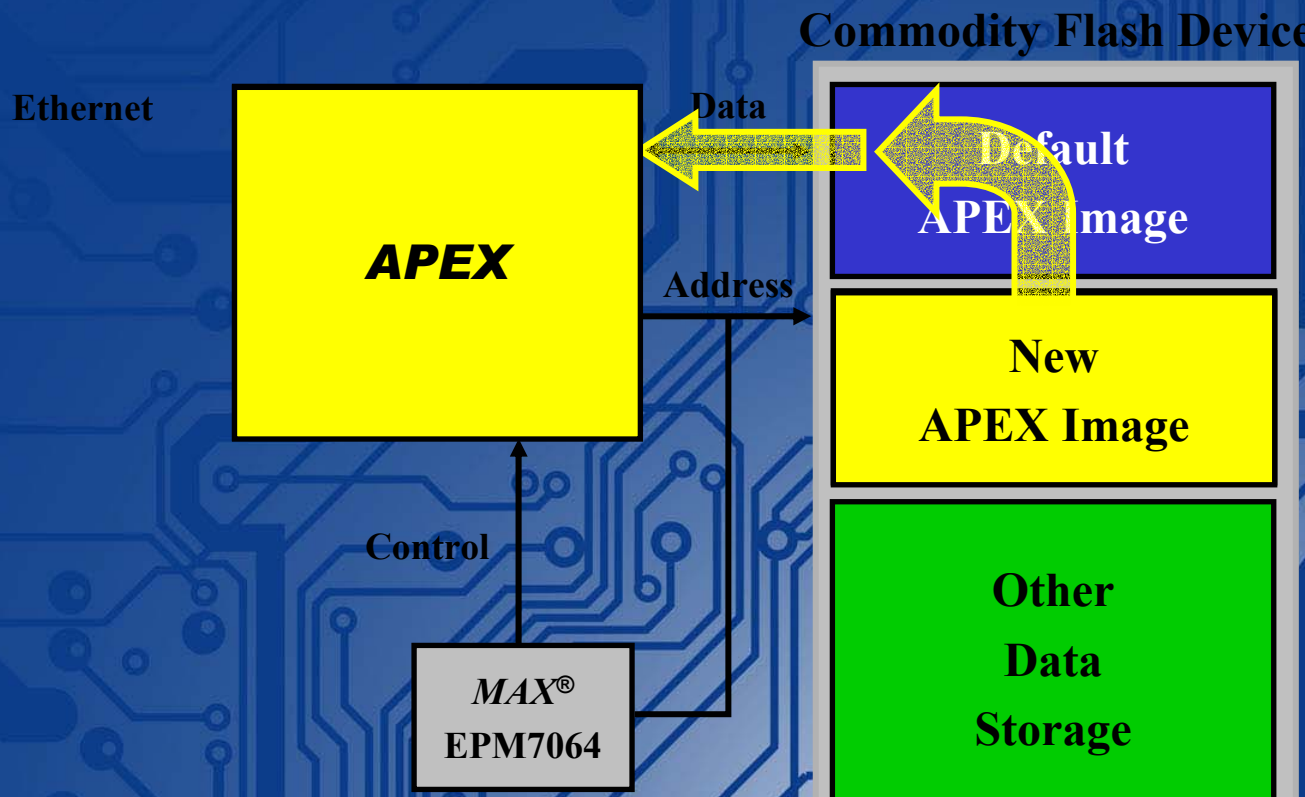
Download New Configuration



Nios Processor Burns "New APEX Image" in Flash

Remote Reconfiguration

Nios Initiated Reconfiguration



Configures from "New APEX Image"

Configures from "Default APEX Image" If Failure (Corrupt Image)

Early Look at Xilinx MicroBlaze

Source Material

- Xilinx Homepage
  - Not much help. No details (and no CPU!) available
- Circuit Cellar online article
  - Early look at MicroBlaze Architecture & Instruction Set

CIRCUIT CELLAR ONLINE

SILICON UPDATE

Tom Cantrell

Core War

Whether it's in the courtroom or in the

key, I suppose.

Sometimes I wonder if either party really has any interest in finally settling the matter. After all, as we saw in the good old days of the Cold War, while the heavyweights are circling, the lightweights (i.e., anyone else who dares to stick their hand into the programmable gate array cookie jar) keep their heads down.

GUNS BLAZING

Naturally, the Xilinx and Altera tit-for-tat extends beyond the courtroom to the product front. The religious war over who has the better FPGA architecture rivals the RISC versus CISC hyperbole of yore. Following the analogy, it's no surprise that as progress marches on, both sides' parts look more alike, calling for more finely parsed nit-picking by each camp's well-entrenched troops.

MicroBlaze Block Fudagram

Only 31 Registers. Mostly dedicated functionality. Result: Waste a lot of instructions moving data into and out of registers.

Advertised performance assumes usage of internal memory only

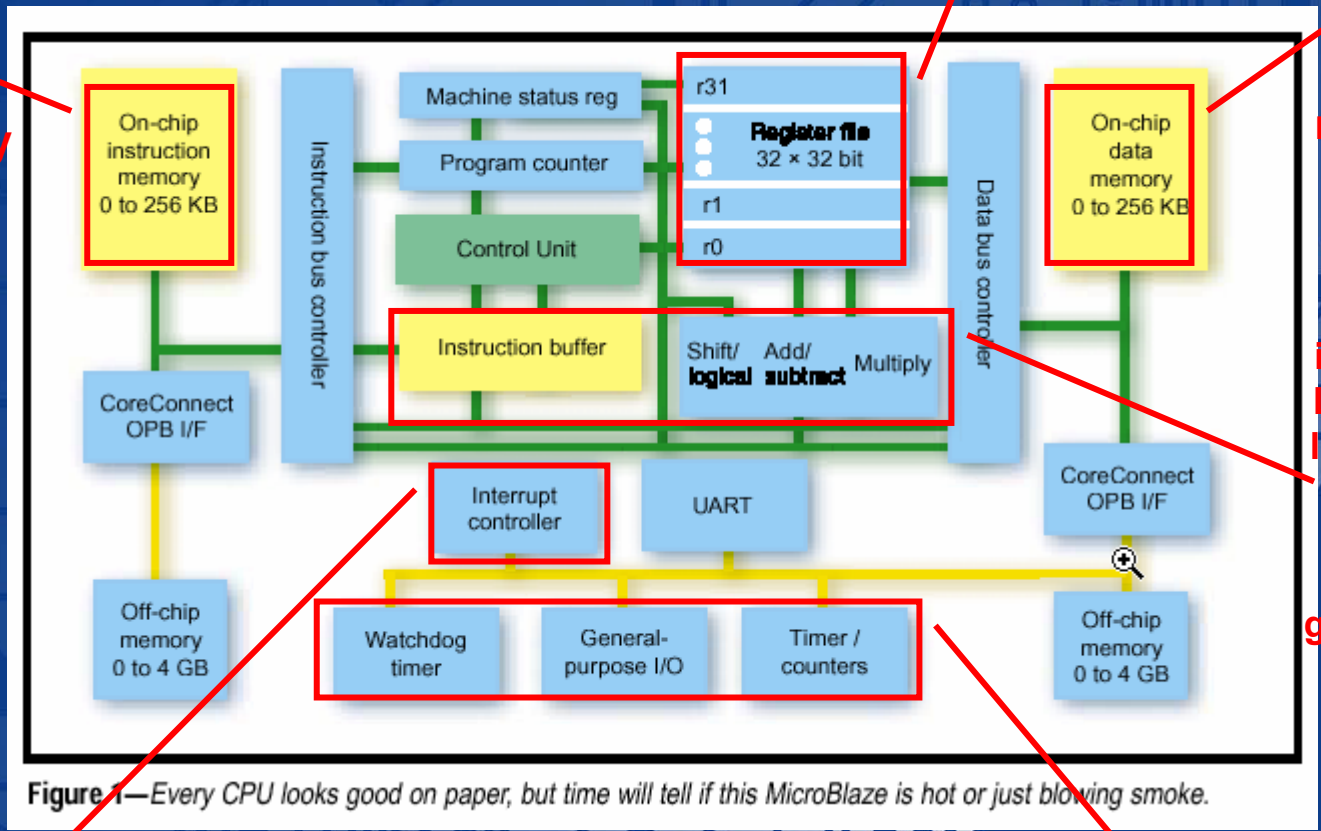


Figure 1—*Every CPU looks good on paper, but time will tell if this MicroBlaze is hot or just blowing smoke.*

Advertised performance assumes usage of internal memory only

Very small instruction set. Limited math & logic functions. Result: More instructions required for a given operation, thus bloated code size.

As advertised, MicroBlaze does *not* include Interrupt Controller Priority Logic

Not clear how many / which peripherals will be included with MicroBlaze kit

MicroBlaze Instruction Set

- 32-bit only microprocessor
  - Requires larger, wider RAM
- Very few, simple instructions
  - More instructions required per operation
  - Instruction variants (e.g. ADD, ADDC, ADDK, ADDKC, ADDI) require a set-up instruction
- One bit per shift only; No left shift operator
  - Requires more cycles for multi-bit shift operations
  - Use ADD for 1-bit left shift
  - *Could use* full multiplier circuit for multi-bit shift
    - Eats hardware resources
    - Device specific optimization
- No Custom Instruction

Opcode	Destination register	Source register A	Source register B	0 0 0 0 0 0 0 0 0 0 0	
0	6	11	16	21	31
Opcode	Destination register	Source register A	Immediate value		
0	6	11	16		31

Table 2—*With only two opcode formats, MicroBlaze pays more than lip service to the concept of a reduced instruction set.*

Addition	Subtract	Multiplication	Sign extend	Logic	Condition branch	Uncondition branch	Load/Store	Special
ADD	RSUB	MUL	SEXT8	AND	BEQ	BR	LBU	IMM
ADDC	RSUBC	MULI	SEXT	16 ANDI			BEQD	BRA
LBUI	MFS							
ADDK	RSUBK			ANDN	BEQI	BRD	LHU	MTS
ADDKC	RSUBKC			ANDNI	BEQID	BRD	LHUI	
ADDI	RSUBI			OR		BRLD	LW	
ADDIC	RSUBIC			XOR	BGED	BRALD	LWI	
ADDIK	RSUBIK			XORI	BGEI	BRI	SB	
ADDIKC	RSUBIC			SRA	BGEID	BRAI	SBI	
				SRC	BGT	BRID	SH	
				SRL	BGTD	BRAID	SHI	
					BGTI	BRLID	SW	
					BGTID	BRALID	SWI	
					BLE	BRK		
					BLED	BRKI		
					BLEI	RTID		
					BLEID	RTSD		
					BLT			
					BLTD			
					BLTI			
					BLTID			
					BNE			
					BNED			
					BNEI			
					BNEID			

Table 3—*The MicroBlaze instruction set is even simpler than it looks, with multiple variants of a single instruction. For instance, the Branch Greater Than instruction (BGT) has delayed (BGTD), immediate (BGTI), and delayed immediate (BGTID) versions.*

MicroBlaze Register File

- Only 31 registers
  - C compiler uses most registers for dedicated function
  - R0 is all zeroes
- Extra instructions are needed to store/load registers to memory
  - Required when all spare registers fill up
  - Slows execution
  - Bloats code size

Register	Type	Purpose
R0	Dedicated	Value 0
R1	Dedicated	Stack pointer
R2	Dedicated	Read-only small data pointer
R3–R4	Volatile	Return values
R5–R10	Volatile	Passing parameters/temporaries
R11–R12	Volatile	Temporaries
R13	Dedicated	Read-write small data pointer
R14	Dedicated	Return address for interrupt
R15	Dedicated	Return address for sub-routine
R16	Dedicated	Return address for trap (debug)
R17	Dedicated	Return address for exceptions
R18	Dedicated	Reserved for assembler
R19–R31	Nonvolatile	Must be saved across function calls

Table 1—*The GNU C compiler maps certain conventions on top of the general-purpose registers. Note the use of R2 and R13 to point at a small (64-KB) data area, fully reachable by the 16-bit offset accommodated in the 32-bit instructions.*

MicroBlaze FUD Busting

- FUD: “MicroBlaze is faster”
  - Fmax is higher, but so is the number of instructions required for a given operation (side effect = Big code & lower performance)
  - Advertised performance assumes memory is on-chip – unrealistic for real systems
  - They’re using Virtex II’s fastest speed grade
- FUD: “MicroBlaze is smaller”
  - MicroBlaze’s advertised size is probably for the CPU logic *only*
    - Nios LE count includes the Avalon bus, Interrupt Generation Logic
    - LE count is all FUD until Xilinx releases the product
  - Strict RISC core may be smaller, but at the expense of code size
- FUD: “MicroBlaze is a full 32-bit processor. Nios has 16-bit instructions”
  - So?
  - Wider instructions require more memory to store them
  - Most microcontroller applications don’t want big memory

How we see it

- Our *Real* Competition is Microcontroller Market (33MHz – 80MHz)
  - Motorola, Hitachi, Intel, Philips, etc.
- Xilinx MicroBlaze
  - Large Code Requirements
    - 32-bit Instructions
    - Few General Purpose Registers
    - Simplistic Instruction Set
  - Fmax Based on On-Chip Memory
    - Expensive, Impractical
  - No Synchronous External Memory Interface
    - They will Achieve 50MHz-66MHz Access
  - What is Their *Total System* Size?
    - CPU, Peripherals, Memory I/F, Memory size
  - System Builder Megawizards are a Significant Competitive Advantage
- Nios has 1-year head start on documentation, applications & reference designs

Software Tools

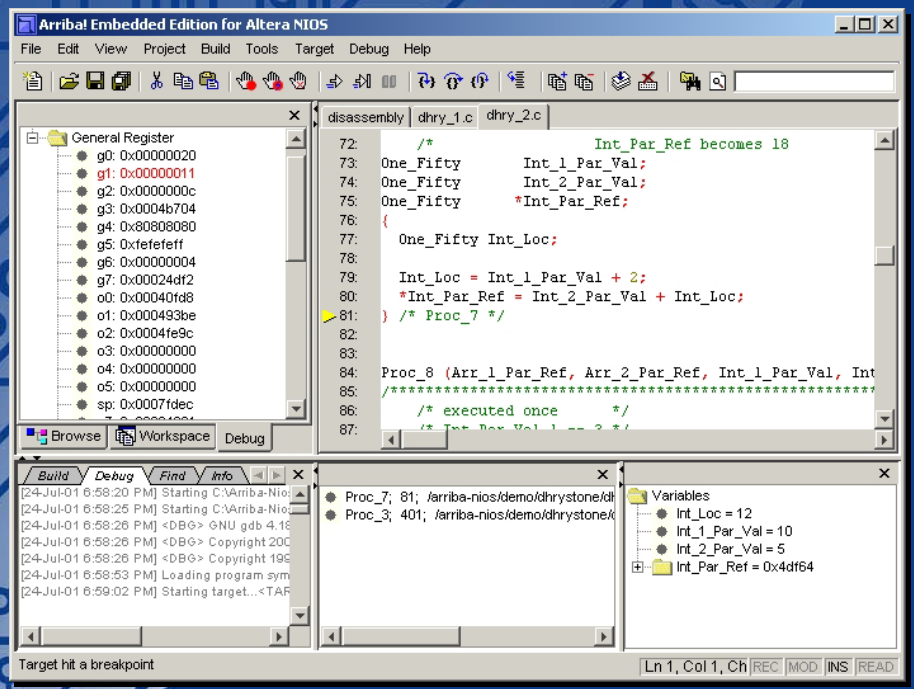
Accelerating Software Development

Software Developer Needs

- Integrated Development Environment
  - Edit, Compile, Run, Download, Debug
- Real-Time Debug
  - Stop on Condition
  - Hardware Break Points
- Software Trace
  - Capture Program Information During Execution
  - Reconstruct to a Source Listing

Software Debugger

- On-Chip Debug (OCD) Peripheral
  - Real-Time Debug (Hardware Breakpoints)
  - Software Trace
- Viosoft Arriba! IDE
  - Supports Nios OCD
  - Edit, Compile
  - Download
  - Run, Debug



Arriba! On-Chip Debug Plug-In

- Real Time Break on Data or External Input
- Software Trace - PC and Data