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ARM®

The ARM Microprocessor Architecture

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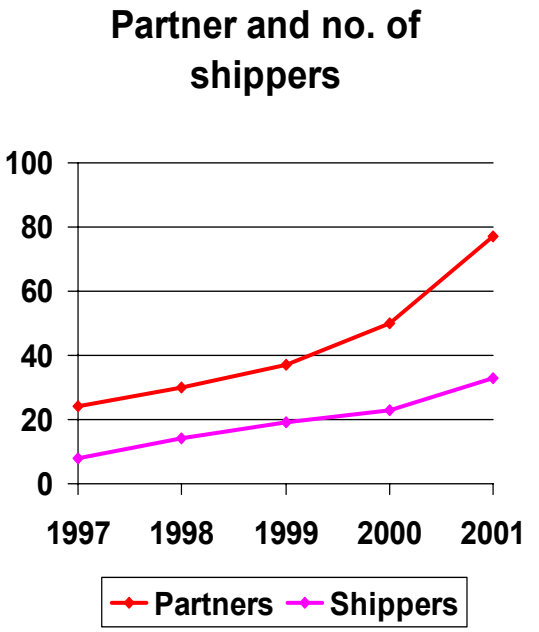
ARM

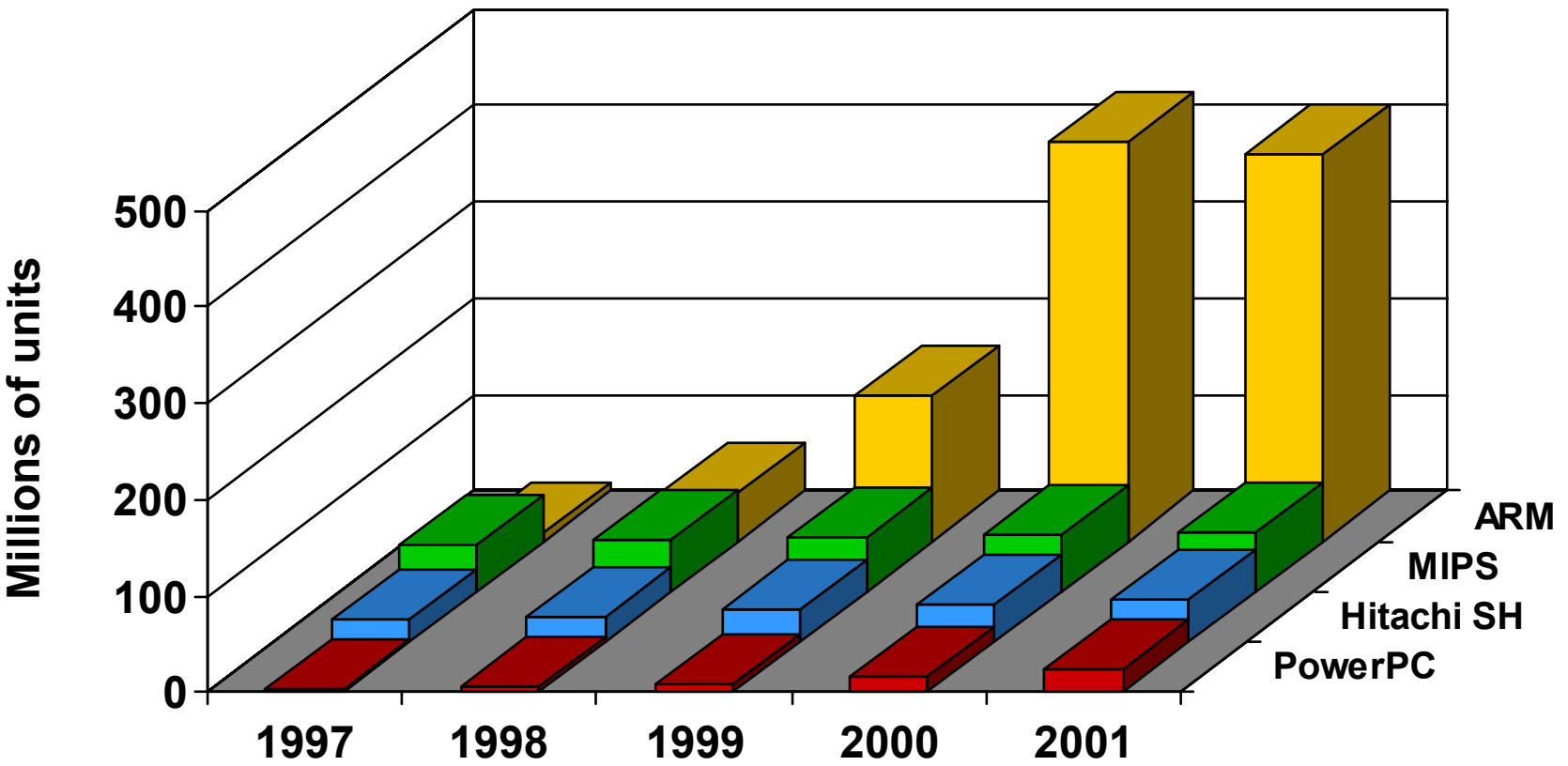
- ARM customers include all the leading international electronics companies
- Shipping product in eight distinct markets:
  - wireless
  - automotive
  - mass storage
  - networking
  - consumer entertainment
  - imaging
  - industrial

ARM Success

- All eight end markets shipping product
- Billionth ARM chip shipped in Nov '01
- ARM Community
  - 30 ATAPS, 4 pure foundry, 77 Semi Partners,
  - Leading apps specific OS > 50
- Trends
  - Software standards become more important
  - Security is new growth driver
- New products to be announced this year and next

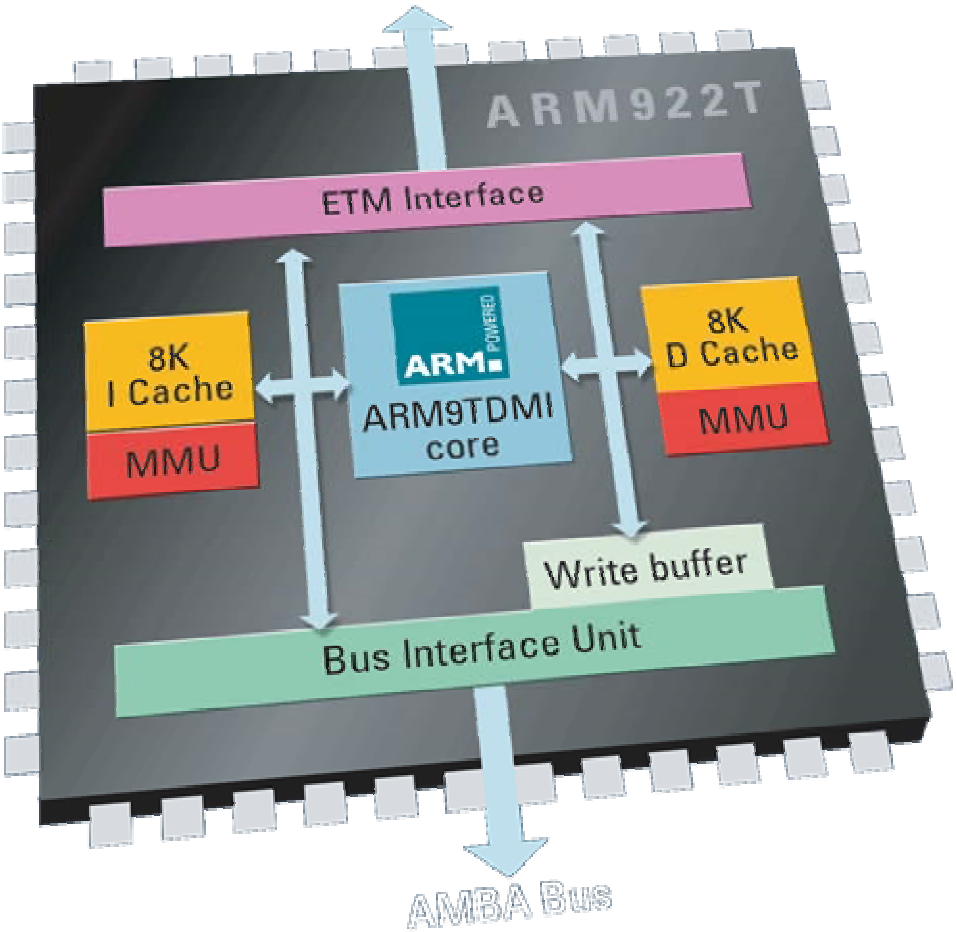


Market Share (Embedded 32-bit RISC Shipments)



Source: Andrew Allison, Inside The New Computer Industry, January 2002

ARM922T



- **Cached Processor for Platform OS-based Applications**
  - Core processor for Excalibur™
  - 8K Instruction & Data Caches
  - ARMv4 MMU for: Symbian OS, Linux, Windows CE & Palm OS
  - ETM9 interface for real-time trace with ETM9 macrocell
  - Hard Macro
    - 8.1mm^2 on 0.18µm
    - 3.2mm^2 on 0.13µm
  - 250MHz* performance (0.13µm

* TSMC 0.13µm G - worst case: slow silicon, +125C, Vcc-10%

ARM922T Specifications

	ARM922T TSMC 0.18µm G	ARM922T TSMC 0.13µm G
Area	8.1mm^2	3.2mm^2
Frequency (typical)**	290MHz	400MHz
Frequency (worst case)*	200MHz	250MHz
Average Power (mW)	0.8mW/MHz	0.25mW/MHz
Mips/W	1375	4400

** Typical frequency: std silicon, 25°C, nominal voltage
* Worst case frequency: slow silicon, 125°C, Vcc -10%

ARM922T Benefits

- High performance with low power
  - 250MHz @ 1.08V 0.13µm (TSMC G worst case)
  - Power 0.25mW/MHz @ 1.2V (typical)
- Small die size for low cost applications
  - 4.7mm^2 & 3.2mm^2 on 0.13µm (including caches)
- ETM9 interface
  - Real time trace capability with ETM9 Macrocell
- Upward code compatibility from ARM7 Family

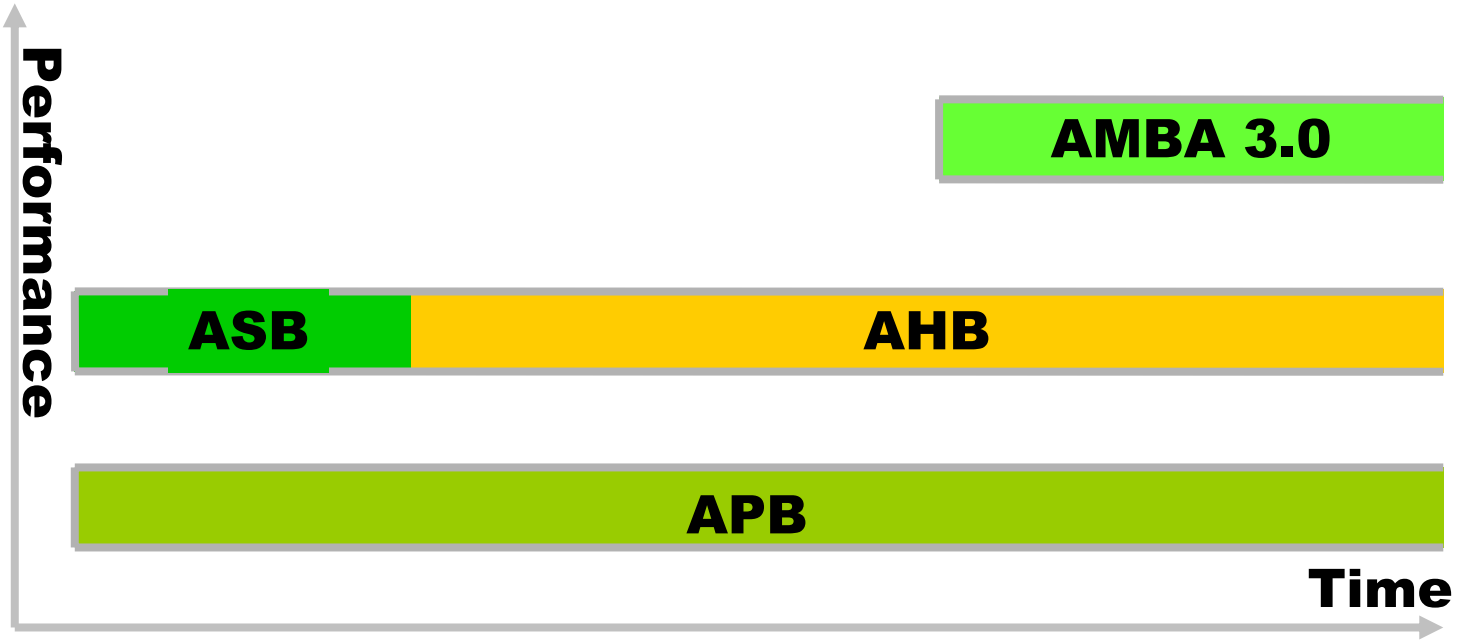
AMBA™

- AMBA - the *de-facto* on-chip bus standard for the industry
- AMBA is an open specification
- Widely adopted by the semiconductor industry including over 90% of ARM partners
- Downloaded by over 2000 design engineers

AMBA - the on-chip bus standard

- AMBA's popularity has encouraged support from third party tool vendors including Altera's Excalibur FPGA
- AMBA remains central to ARM's strategy and is actively supported and developed in conjunction with ARM Partners

AMBA Roadmap



- With the development of AMBA 3.0, ARM is ensuring that AMBA will continue to meet the requirements of the semiconductor industry

AMBA Interface Protocol

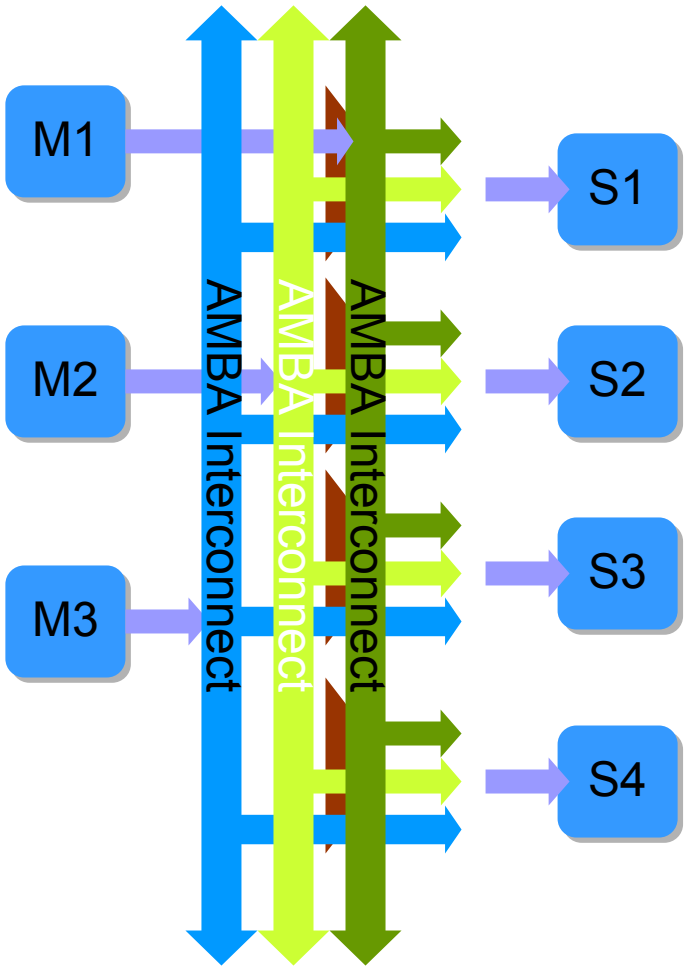
- The AMBA 2.0 Specification defines protocol for two interfaces:
  - APB: Low complexity for low bandwidth slaves
  - AHB: High performance, multi-master capability
- For systems with only one AHB master the interface can be simplified to AHB-Lite
  - Compatible sub-set of full AHB
  - No arbitration, no SPLIT or RETRY responses

AMBA Multi-layer AHB

- Enables the system architect considerable flexibility to optimize the bandwidth and latency
- Allows the flexible partitioning of resources between sub-systems
- Additional routing comparable to a wider bus of equivalent bandwidth
- All layers must operate from a single HCLOCK

Multi-layer AHB

- Increased channel capacity
  - multiplied by the number of layers
  - Performance limits at peripherals, not interconnect
  - Layers with a single master can use AHB-Lite



The AMBA Compliance Program

- Reduces risk and time-to-market by guaranteeing compliance of third party IP
- The AMBA Compliance Program exists to promote this added value to IP vendors and users
- IP developers claim AMBA Compliance using the AMBA Compliance Testbench (or other approved tool) to be members of the Program
- Altera part of Beta Program

Embedded Trace Buffer

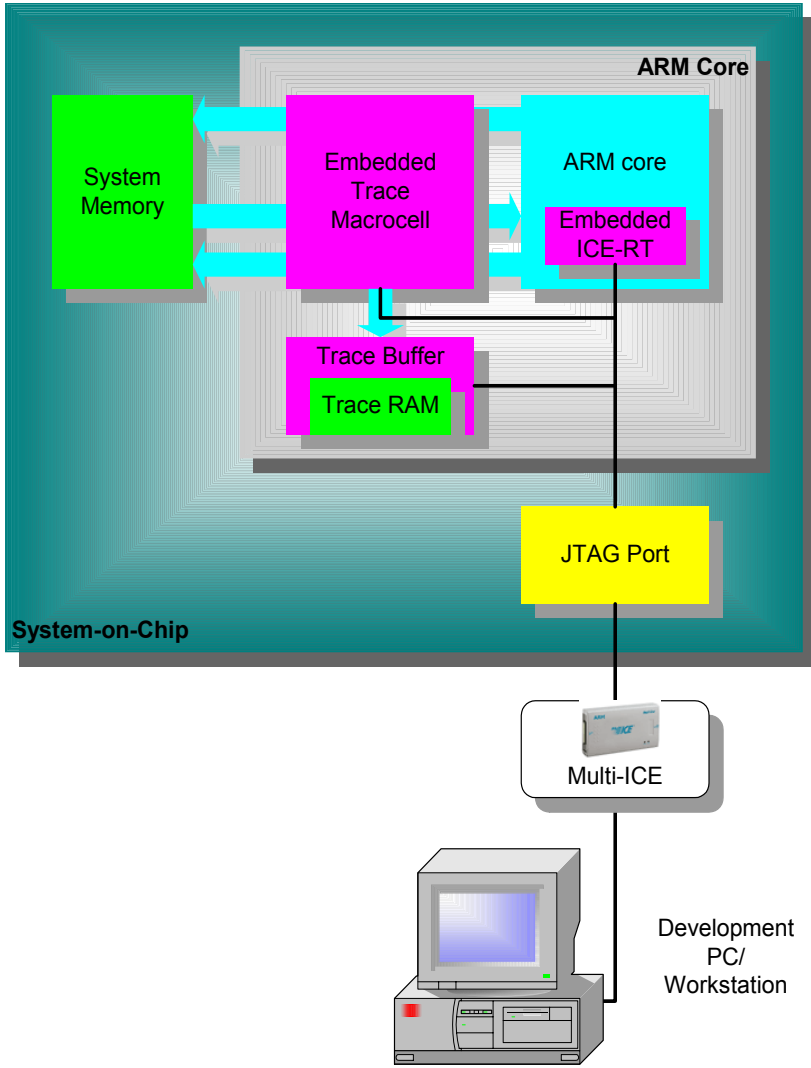
- World-leading embedded debug technology
- Non-intrusive trace and debug
- Full-speed capture up to 200MHz
- System runs at full speed
- Traces both instructions ***and data***
- Cycle-accurate trace
- Time-stamping allows data to be captured for later analysis and profiling
- Glueless connection to all supported ARM processors

Embedded Trace Macrocells

- Conventional debug tools cannot be used with deeply-embedded processor cores
- Consequently, debugging software on highly integrated SoC devices is complicated
- ARM's ETMs solve this problem by providing fully-featured real-time trace capabilities
- Developers can use the same debug facilities from prototype to final fully-integrated product

ETM features

- Zero performance overhead
- Trigger possible on complex sequential conditions
- Filter conditions control which data is captured
- Dedicated trace port, configurable for number of pins and bandwidth
- Data compression and small on-chip FIFO buffer
- User configurable for FIFO overflow condition
- Configured non-intrusively through JTAG



RealView™ ARM Tools by ARM

- RealView Development Solution delivers
  - OEMs with the fastest time to market
    - More functional, lower cost OEM products
  - Integrated development solution
  - One brand family with the same quality promise
  - Broadest compatibility between tools
- The Benefits of RealView
  - The best performance tools for the ARM architecture
  - The best visibility of ARM cores and platforms
  - Tools, Cores and Platforms are developed together

RealView Product Views

- Debug view: RealView Debug solution
  - Speeds development time, simultaneous multi-core debug, extended target visibility and OS 'awareness'
  - Includes RealView Debugger, RealView ICE and RealView Trace
- Software view: RealView Compilation tools
  - Delivers tighter code density, reduces memory budget, increases performance
- Platform view: Integrator® Platforms and boards
  - Enables integration of software and hardware IP, reduces development times, early prototyping increases confidence in final silicon

RealView ICE and Trace

- Modular Construction
  - Scaleable hardware allows the users to build systems they need
  - Trace Module for ETM trace capture
  - New requirements, new modules e.g analyser module
- Unbeatable performance
  - Highly optimised, intelligent JTAG hardware acceleration
- Supports all current ARM cores
  - ARM7™, ARM9™, ARM9E™, ARM10™ families and Intel® XScale™ microarchitecture

RealView ICE Key Features

- High performance debug
  - Code download 600k bytes/sec over JTAG @ 10MHz
  - Stepping speed 100 steps/sec
  - JTAG clocks up to 66MHz, 1 - 5V
- New differential signal probe for high JTAG frequencies, longer cable
- Both network and local host connection
  - Ethernet 10/100baseT
  - USB 1.1/2.0
- Non-ARM and co-processor (DSP) support
- Tightly coupled, synchronized multi-core control
- Trigger synchronisation with external events
  - to/from target
  - to/from logic analyser

RealView Trace Key Features

Trace support using on-chip Embedded Trace Buffer

Trace support using add-on trace module

- 4M deep buffer 4/8-bit trace port 2M 16-bit
- Maximum target clock frequency 200+ MHz
  - 2.5 ns set-up, 1 ns hold
- On-the-fly trace data upload, up to 8 MB/s
- ETM trace ports modes supported:
  - ETM protocols v1.x, v2.x, v3.x for ETM7/9, ETM10 and ETM11
  - single and doubled edged clocking
  - normal, multiplexed and de-multiplexed ports
  - 4, 8, 16-bit data port widths
- Time stamp (48-bit) 10ns resolution 32 day duration

RealView Debugger: Overview

- Multi-Core debug
  - ARM + ARM or ARM +DSP
  - Single debug kernel
- Real-time trace
- OS awareness
- Extended target visibility
  - Visualisation of the whole target
- Built in IDE
  - Own editor
  - Project manager
  - Build system

Multi-Core Debug Features

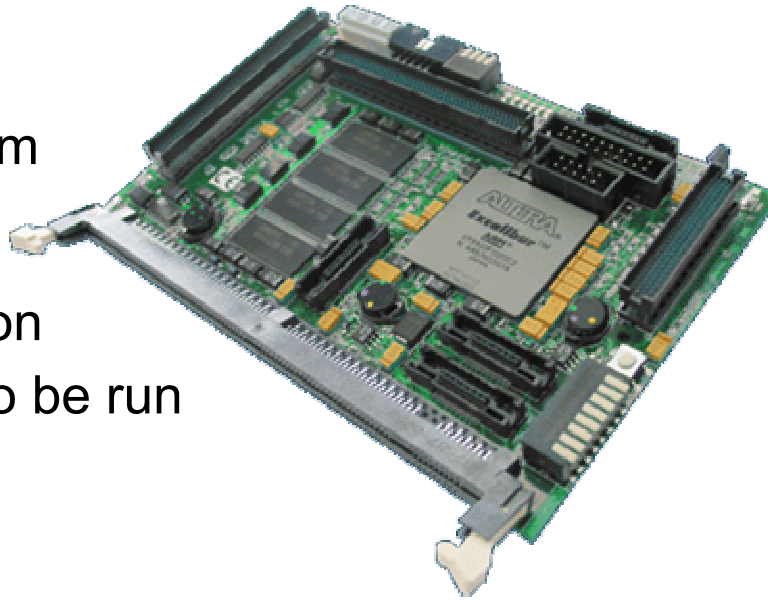
- **Multiple core connection**
  - Multiple ARM cores
  - Connects to ARM(s) + DSP(s)
- **Multiple core control**
  - Support for Synchronised Start and Stop
  - Support for Synchronised Stepping
  - Support for Cross Triggered breakpoints
    - Target H/W support required

RealView Compilation Tools

- Market leading compilers
  - up to 30% better than 3rd party ARM compilers
- Code size
  - Reduced product build cost for same functionality
- Performance
  - Lower frequency for same performance – leading to longer battery life
- Reliability
  - Excellent code quality, improving time to market
  - Mature – continual development and improvements over 12 years
- Roadmap
  - Future code density and performance improvements
  - Further support for new V6 architecture and beyond

RealView Platforms

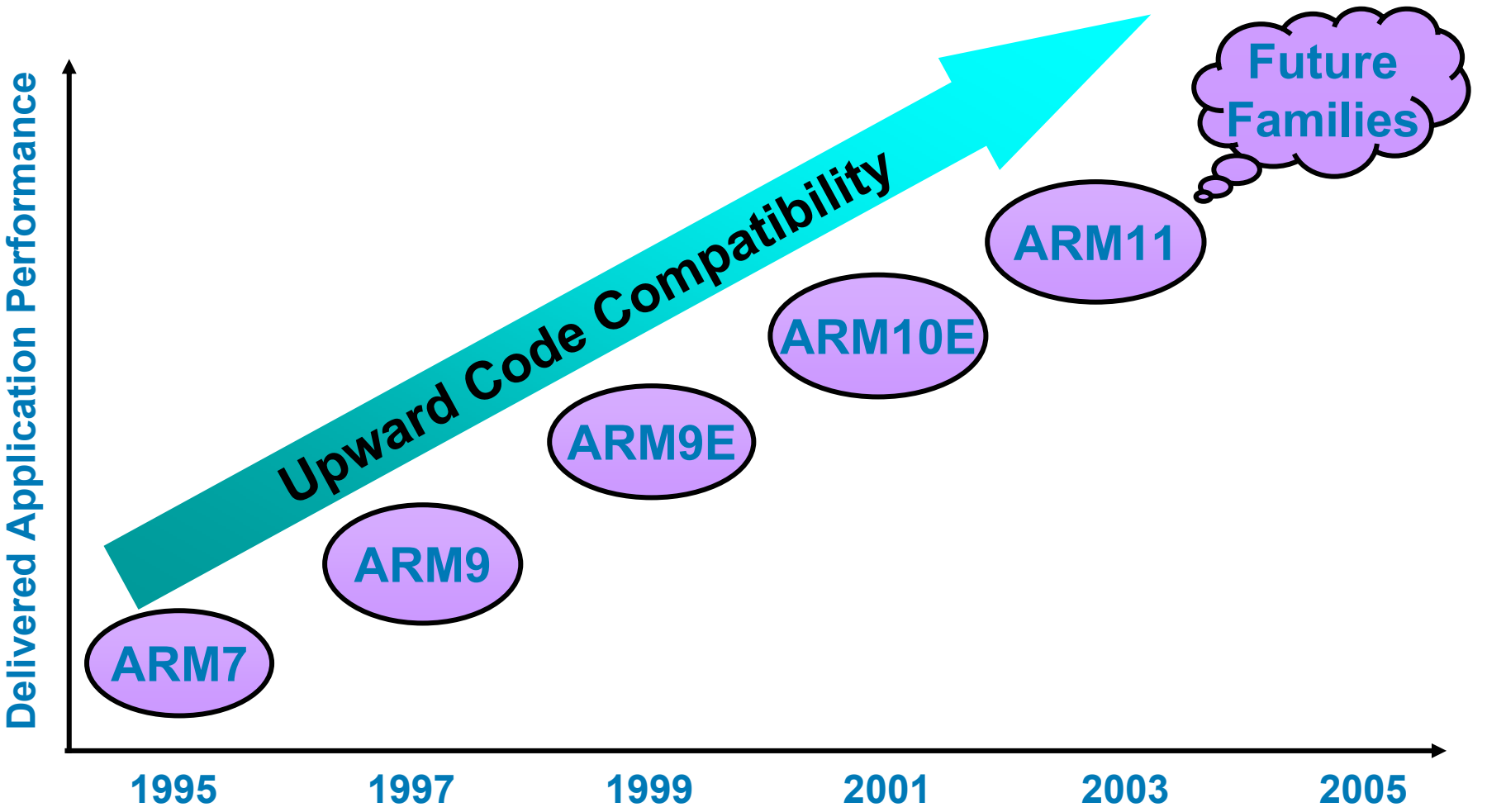
- Integrator part of the RealView solution
  - Provides an early access platform for SoC developers
  - Supports the full range of ARM cores
  - Cost effective emulation of final system
    - Including Multi-core
  - Increases confidence level of validation
    - Enables millions of lines of code to be run
  - Increases confidence in first silicon
  - Shortens design cycle



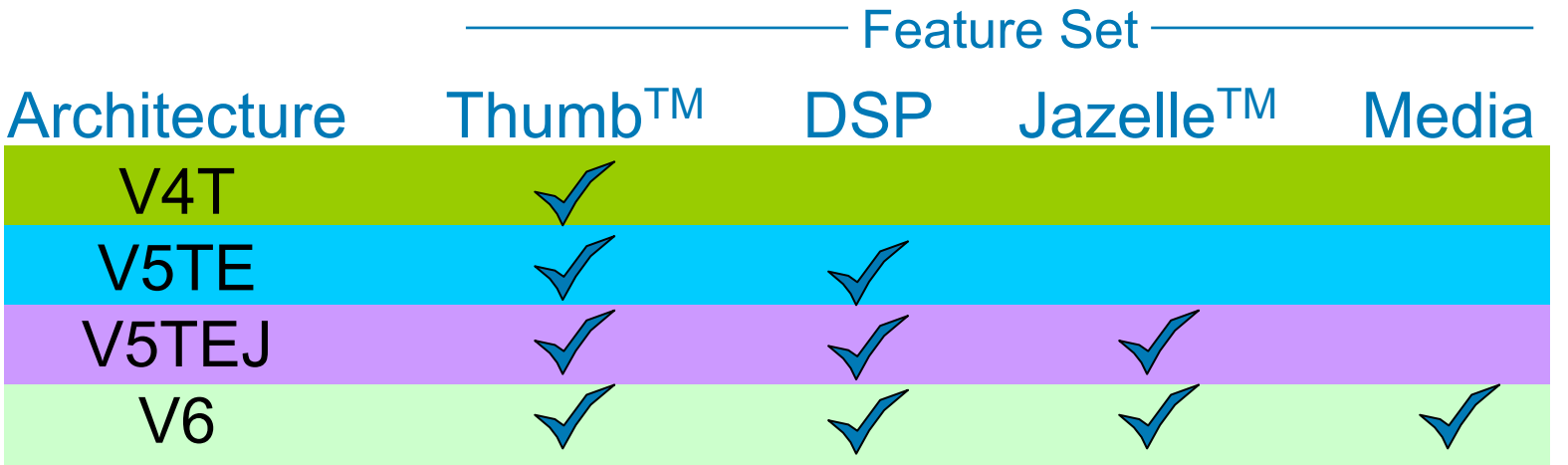
Summary

- RealView Development Solution
  - Offers best available ARM support
  - Industry-leading debug methodology for ARM SoCs
    - RealView ICE & Trace
    - RealView Debugger
  - Highest performance compilers
    - Best code density and performance
  - Range of development boards for prototyping
  - Accelerates product development
  - Reduces risk

ARM CPU Processor Core Roadmap



ARM Architecture

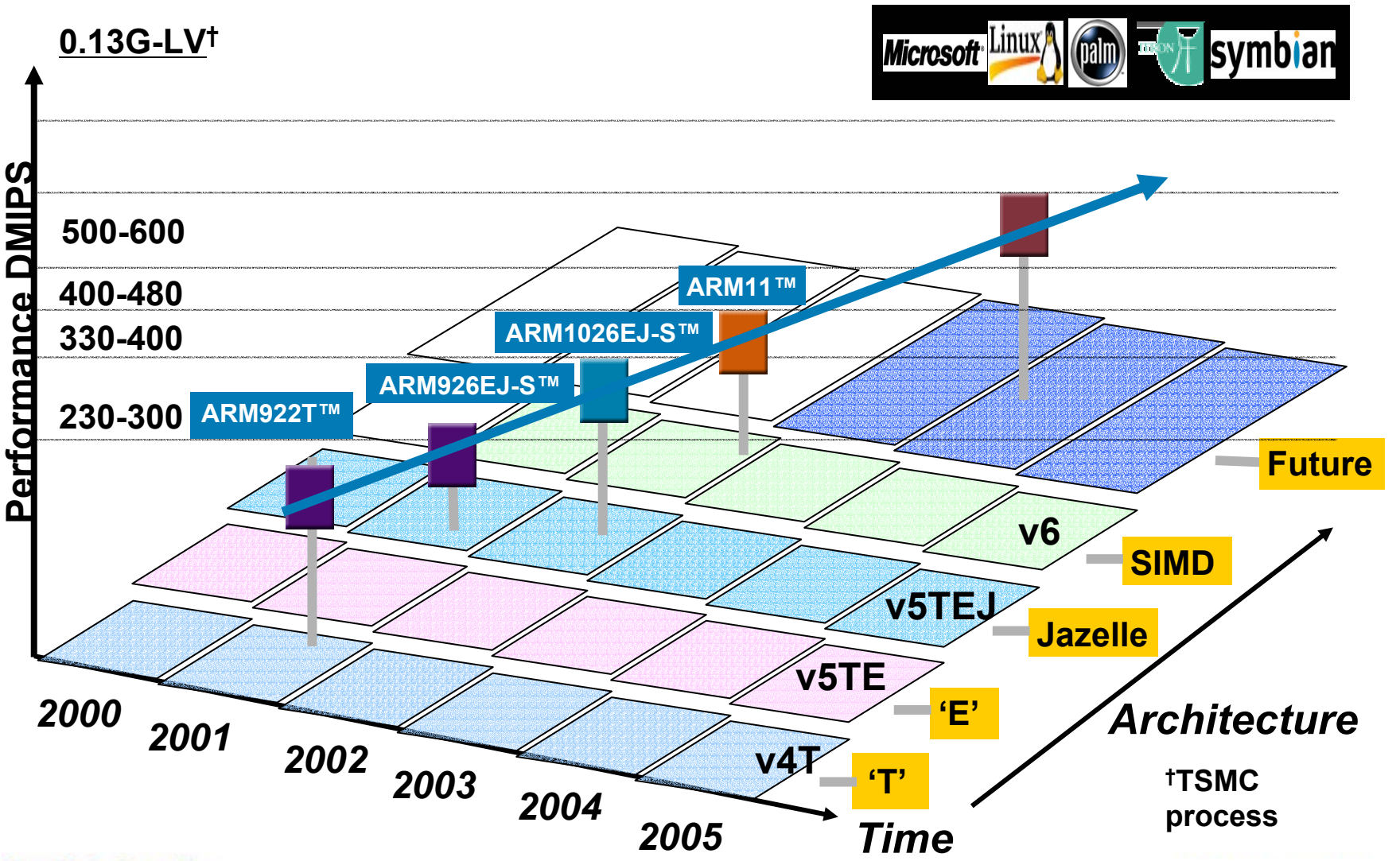


Enhanced performance through innovation

Thumb™:	Up to 35% code compression
DSP Extensions:	Higher performance for fixed-point DSP
Jazelle™:	Up to 8X performance for Java
Media Extensions	Up to 2X performance for audio & video

Preserve software investment through compatibility

Consumer OS Roadmap



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