

20 YEARS of

ALTERA®

INNOVATION



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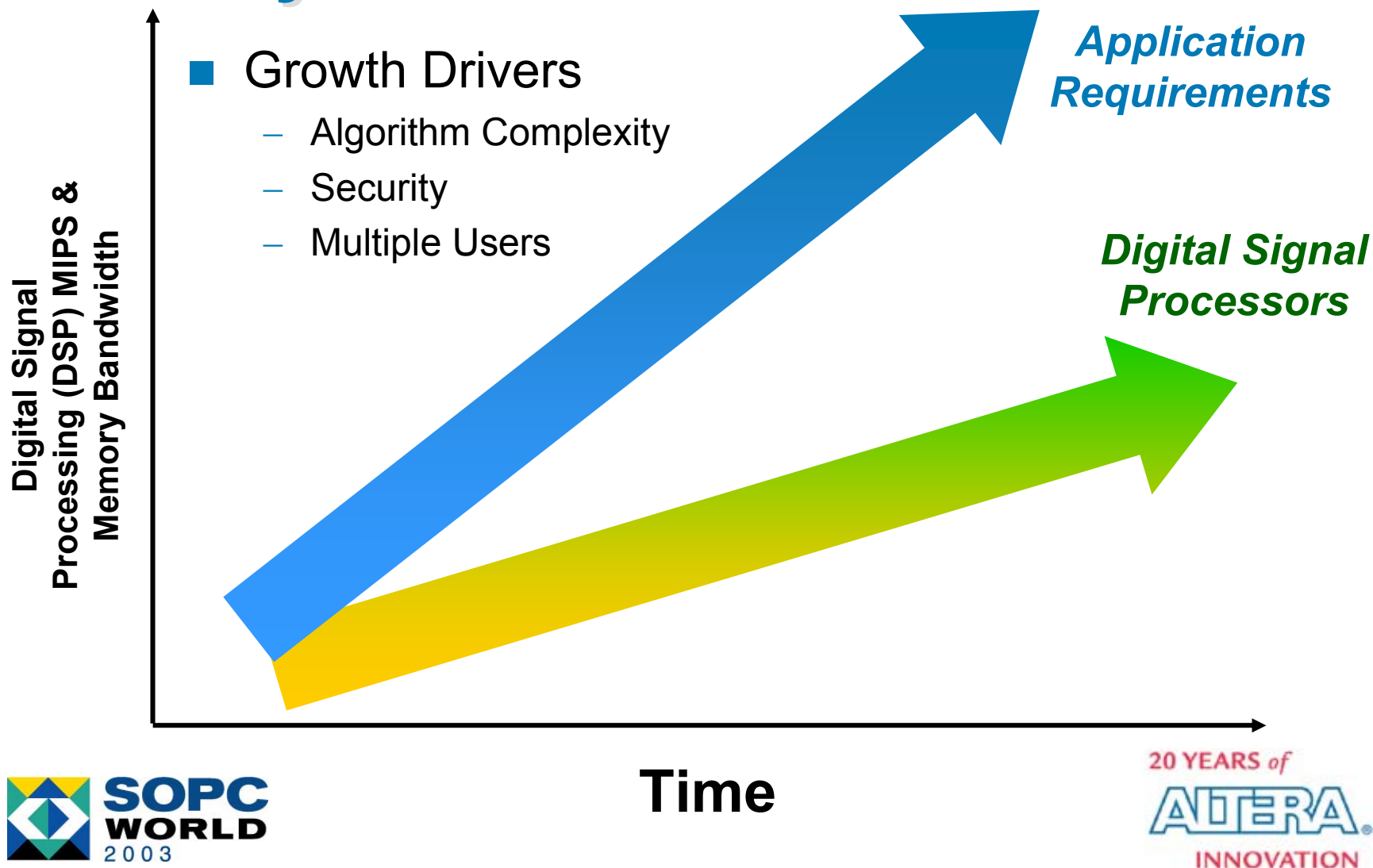
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FPGA Co-Processing for DSP

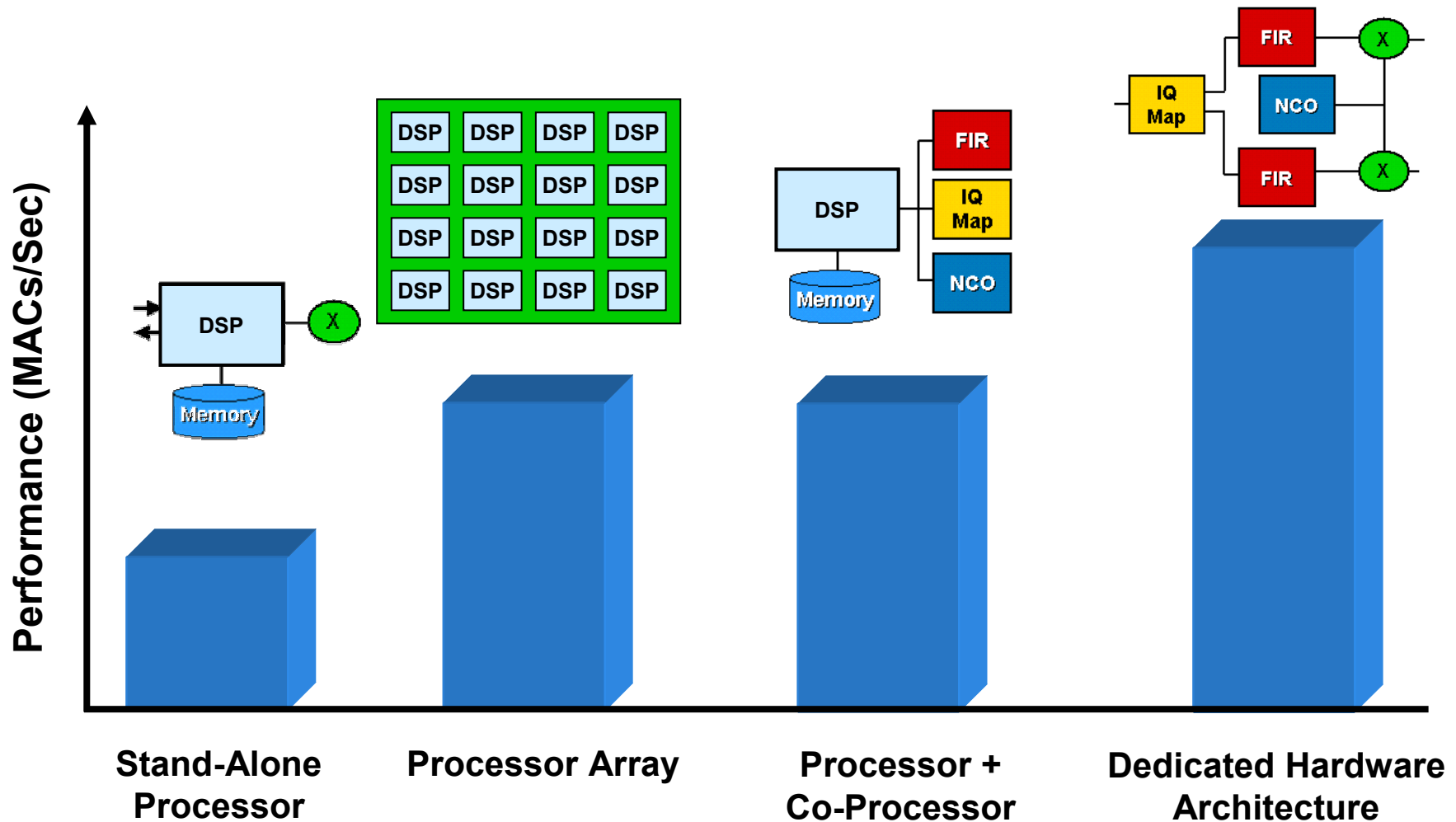
Agenda

- Applications of FPGA-Based Co-Processors for DSP
- Development Tools & Methodologies Available from Altera to Build Co-Processors
 - SOPC Builder
 - DSP Builder
- FPGA Co-Processor Development Examples
 - QAM Modulator
 - FIR Filter

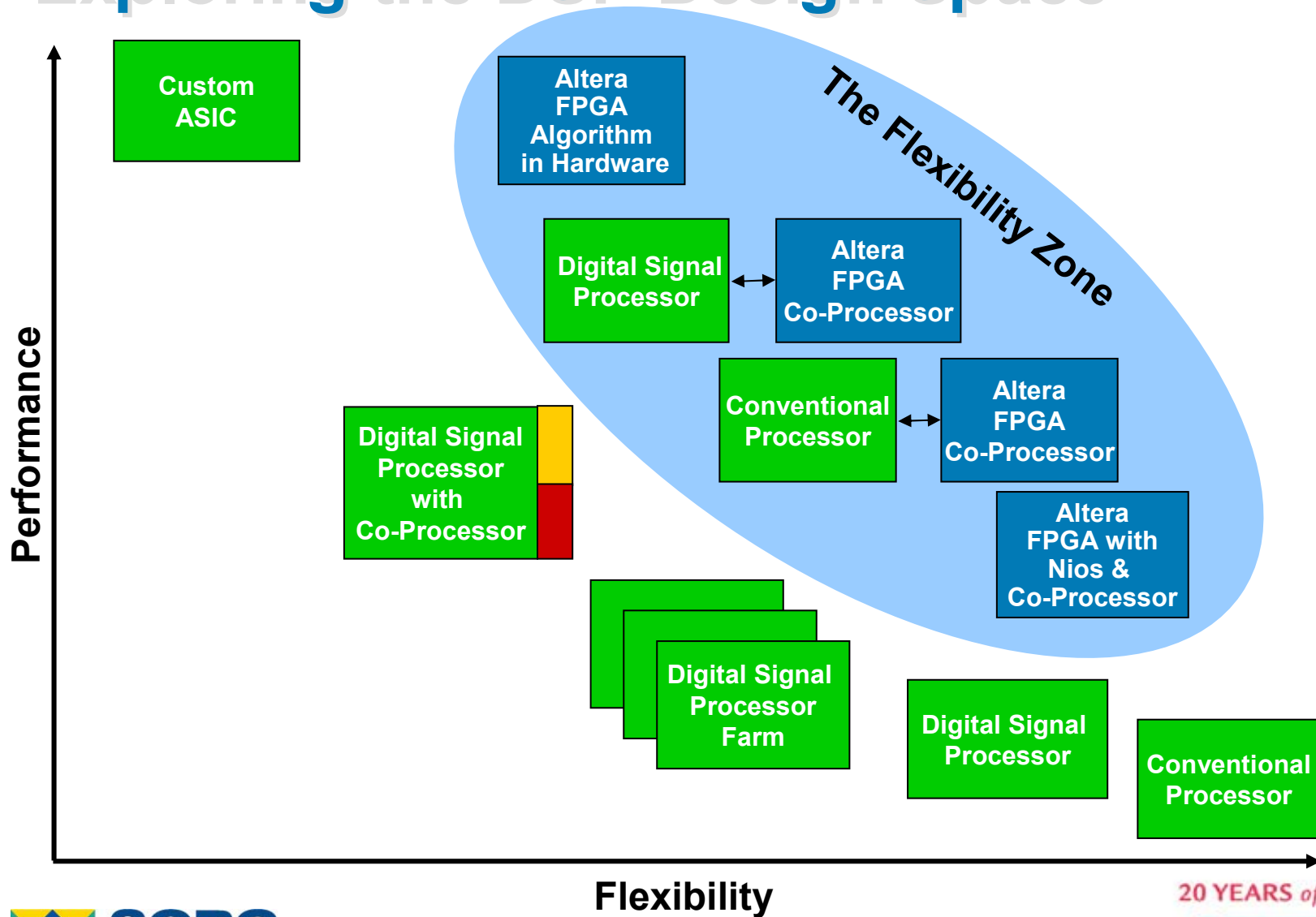
Growing Demand for MIPS & Memory Bandwidth



DSP System Architecture Options

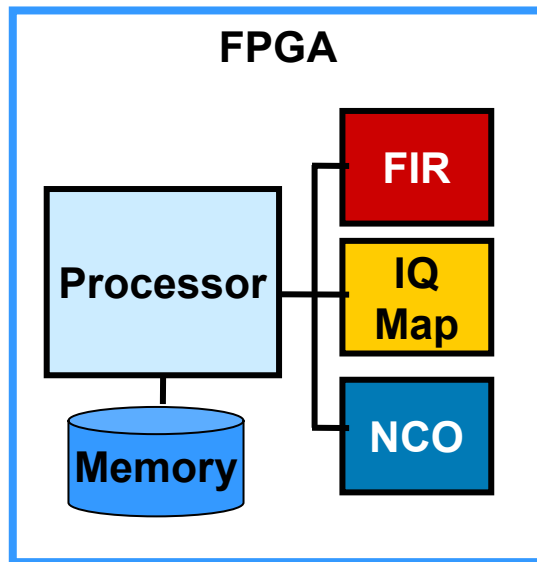


Exploring the DSP Design Space

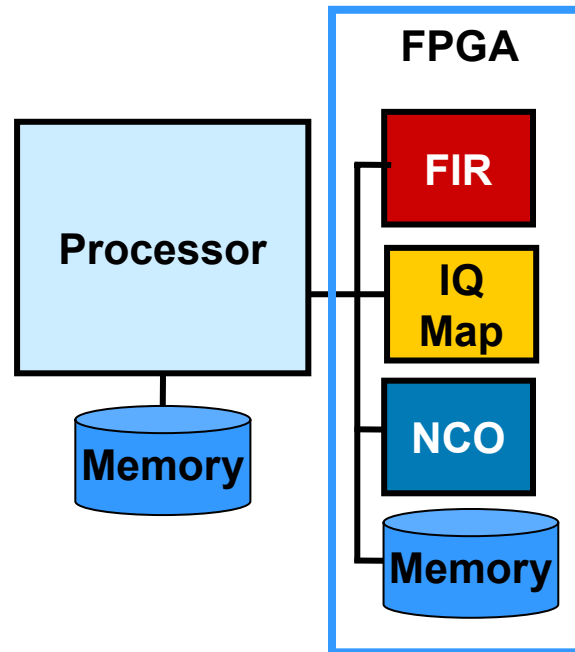


Co-Processing on FPGAs

Processor on FPGA

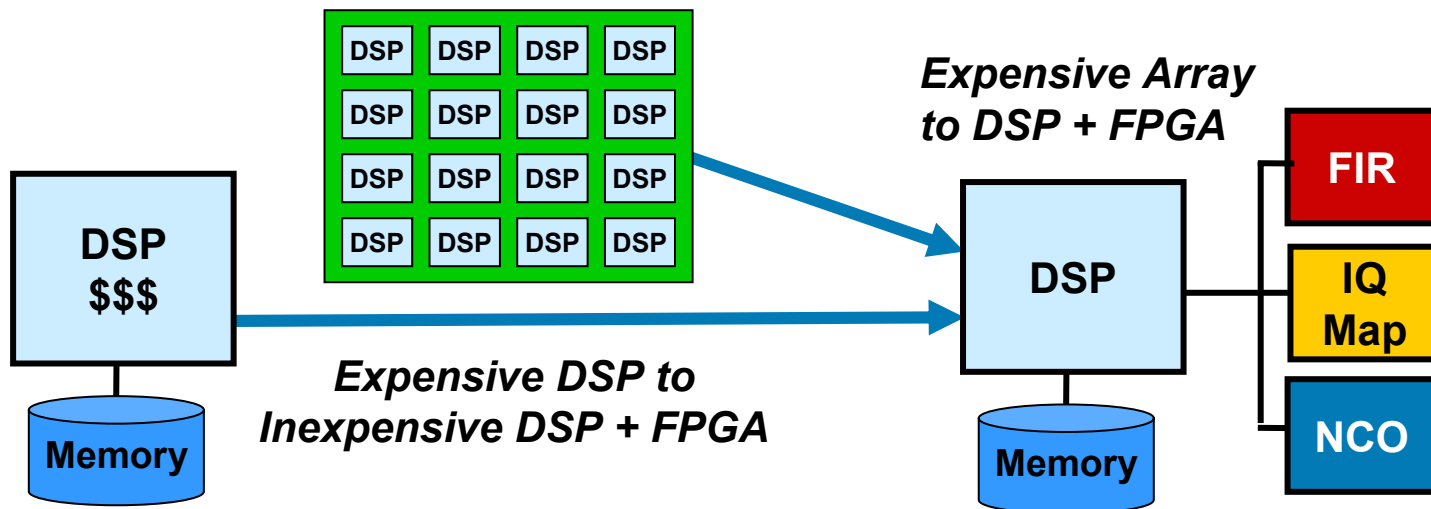


Processor External to FPGA



When Do FPGA Co-Processors Reduce System Cost?

- Off-Loading Algorithms to Co-Processor Reduces Number or Cost of Digital Signal Processors



- Applications
 - Algorithms with Large Amount of Digital Signal Processing & Small Amount of Control Processing

FPGA Co-Processor Applications

■ Wireless

- 2.5-G EDGE Equalization
- 3-G Baseband Processing
 - HSDPA
 - 1xEVDO
- 3-G RF Linearization

■ Consumer

- Broadcast - Studio & Cable Plant
- Digital Entertainment – MPEG2 & MPEG4

■ Medical

- Imaging

■ Wireline Communications

- Encryption
- Framing
- Traffic Management
- TCP/IP

■ Computer & Storage

- Data Analysis & Routing Engine
- Digital Imaging

■ Military & Aerospace

■ Security

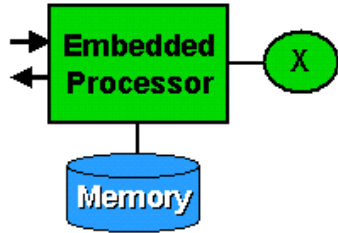
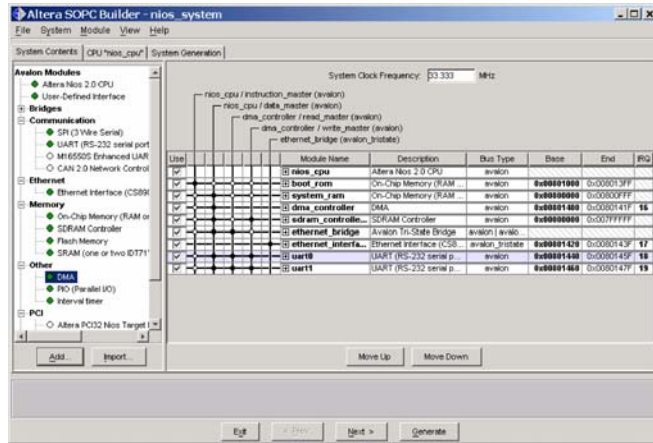


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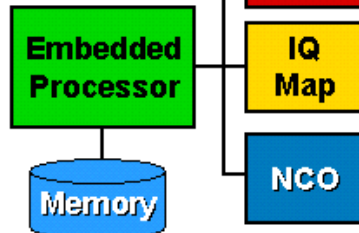
DSP Development Tools & Design Methodology

FPGA Co-Processor Design Tools

SOPC Builder

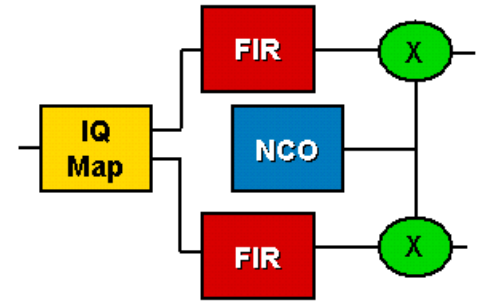
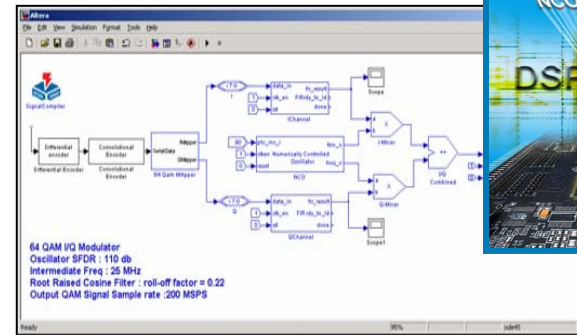


Stand-Alone Processor



Processor + Co-Processor

DSP Builder



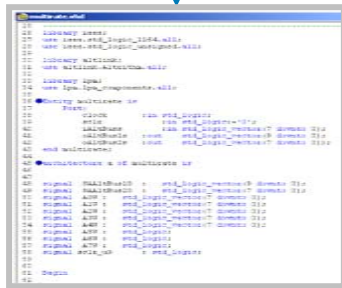
Dedicated Hardware Architecture

DSP Builder Overview

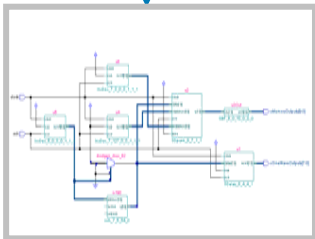
DSP Builder

MATLAB®
& SIMULINK®

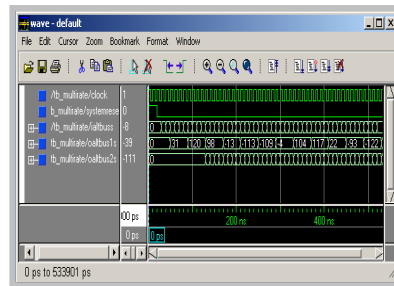
Creates
HDL Code



HDL
Synthesis



Creates
Simulation Test Bench



Model Technology
A MENTOR GRAPHICS COMPANY

Creates
Processor
Plug-In



Download
Design to
Development
Board



Verify
in
Hardware



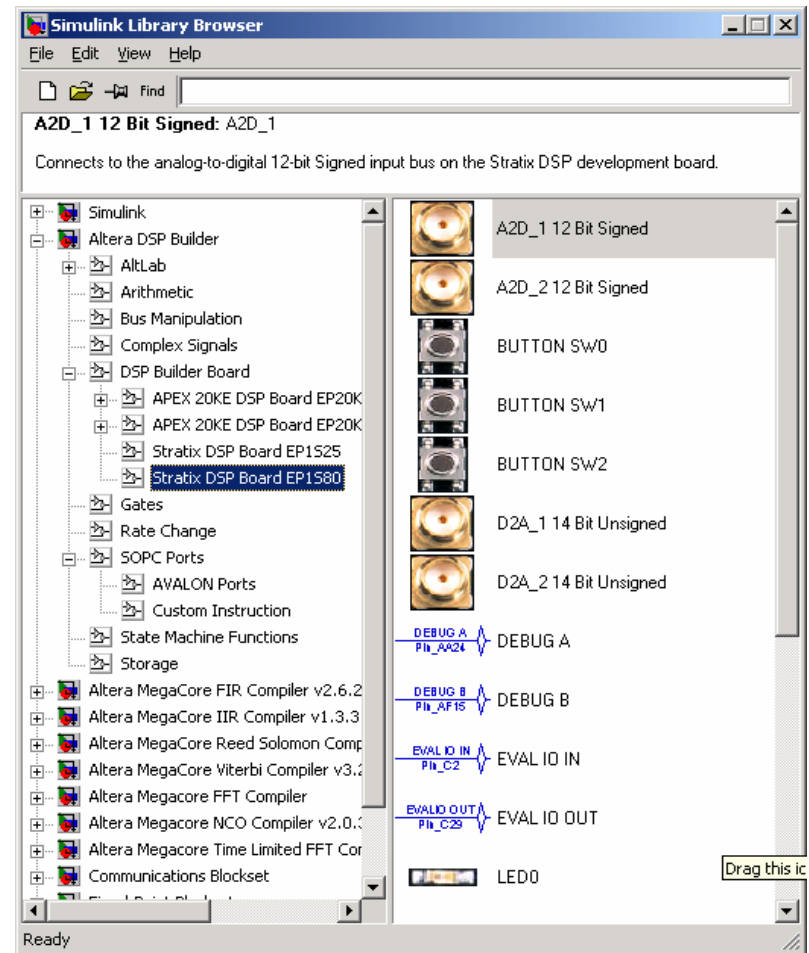
QUARTUS® II

exemplar
A MENTOR GRAPHICS COMPANY



DSP Builder Library Components

- Arithmetic
- Bus Manipulation
- Complex Signals
- Logical Components
- SOPC Ports
- Storage
- MegaCore® IP
- Rate Change
- State Machine
- Altera Library
- DSP Board



MegaCore IP in DSP Builder

The image is a collage of screenshots from Altera DSP Builder and MegaWizard, illustrating the configuration of MegaCore IP blocks.

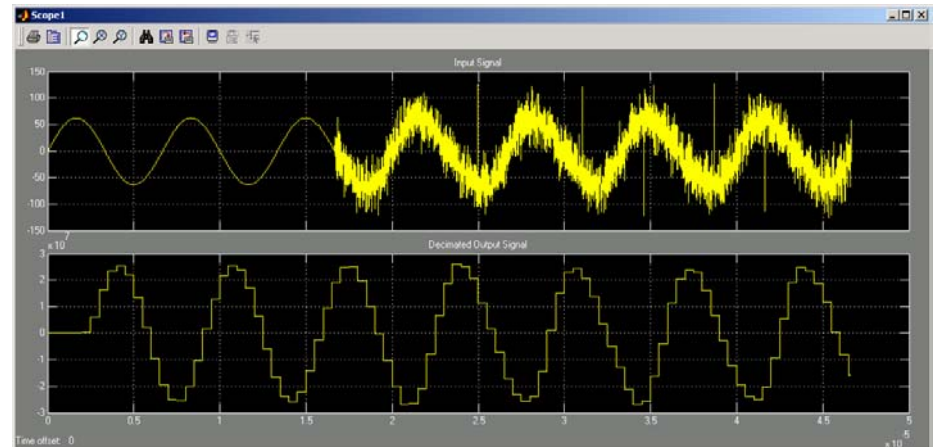
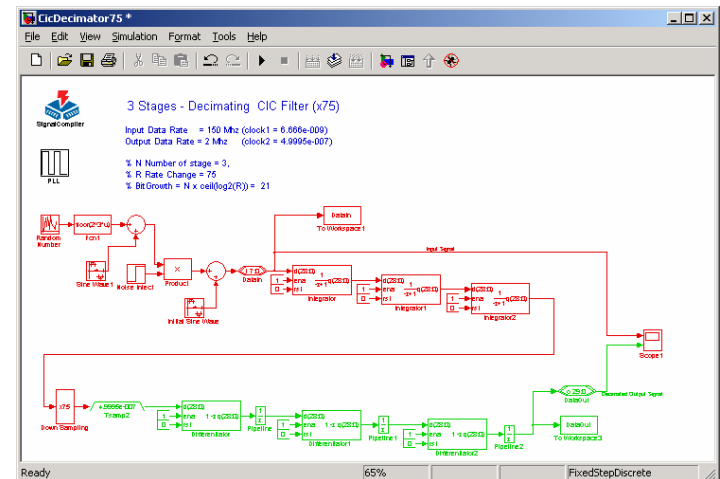
- Simulink Library Browser:** Shows the 'NCO: Numerically Controlled Oscillator' block. It includes instructions: '1 - The system must contain the "Signal Compiler" block with the c... interface.' and '2 - Double click on the NCO Compiler block to invoke the MegaWiz...'. A list of available blocks is shown, including 'Altera DSP Builder', 'Altera MegaCore FIR Compiler v2.6.2', 'Altera MegaCore IIR Compiler v1.3.3', 'Altera MegaCore Reed Solomon Comp...', 'Altera MegaCore Viterbi Compiler v3.1', 'Altera Megacore FFT Compiler', 'Altera Megacore NCO Compiler v2.0.1', 'Altera Megacore Time Limited FFT Co...', and 'Communications Blockset'.
- DSP Kit Filtering:** A block diagram showing the integration of various MegaCore blocks. A blue circle highlights the 'Time Limited Numerically Controlled Oscillator' block, with a blue arrow pointing to the 'filter_design_NCO_10MHz' block in the MegaWizard window.
- MegaWizard - DSP Builder: NCO Compiler v2.0.3 Time Limited [Page 1 of 2]:** Shows the configuration parameters for the NCO. The 'Parameters' tab is active, showing 'Generation Algorithm' (Multiplier-Based), 'Precisions' (Accumulator Precision: 32, Angular Precision: 12, Magnitude Precision: 13), and 'Phase Dithering' (Implement Phase Dithering: checked). The 'Generated Output Frequency Parameters' are set to 'Clock Rate: 80 MHz', 'Desired Output Frequency: 10 MHz', and 'Phase Increment Value: 536870912'. The 'Frequency Domain Response' and 'Time Domain Response' plots are shown at the bottom.
- FIR Compiler 2.3.1 : Coefficient Analysis:** A window showing the coefficient analysis for an FIR filter. It displays '97 Coefficient(s) in this set' and 'Positive Symmetry'. The 'Coefficient Bit Width' is set to 10, and the 'Scaling Factor' is 4. The 'Coefficient Values' list shows a range from 32 to 40. The 'Current Coef. Set' is 1. The 'Frequency' plot shows the frequency response of the filter, with a legend indicating 'Blue : Freq. Response of Fixed Point Coefficients' and 'Green : Freq. Response of Floating Point Coefficients'.

DSP Builder MegaCore® Functions

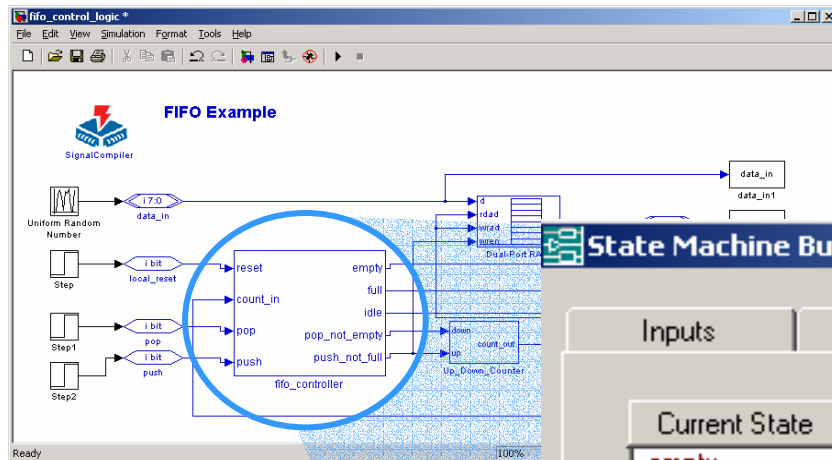
- FIR
- FFT
- Viterbi
- Turbo
- Reed Solomon
- NCO

DSP Builder Support for Multiple Clock Domains

- Inherit Sampling Frequency (FS)
- Adhere to Clock Design Rules
- All Sample Times Match One of Phase-Locked Loops (PLLs) Output Clock Periods
- Simplify Analysis & Implementation of Multi-Rate System
 - Up Sampling
 - Down Sampling



State Machine Builder



State Machine Builder v2.1.0

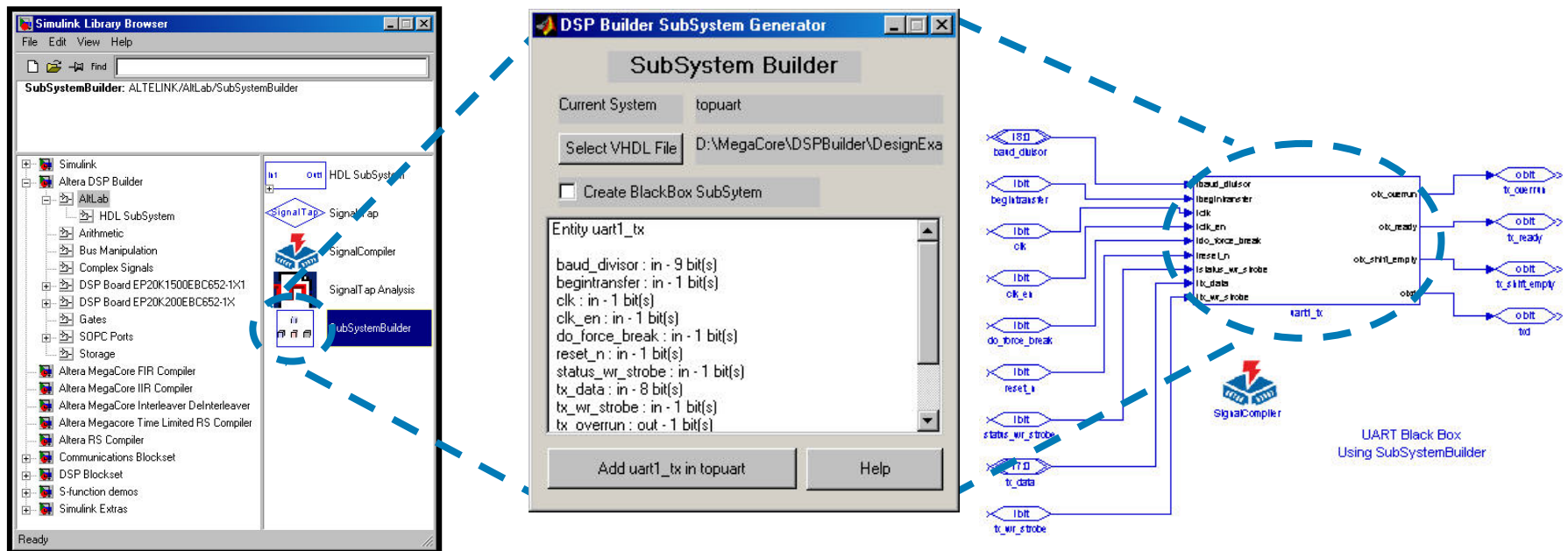
Inputs States Conditional Statements Design Rule Check

| Current State | Condition | Next State |
|---------------|--------------------------|---------------|
| empty | (push=1)&(count_in!=250) | push_not_full |
| empty | (push=0)&(pop=0) | idle |
| full | (push=0)&(pop=0) | idle |
| full | (pop=1) | pop_not_emp |
| idle | (pop=1)&(count_in=0) | empty |
| idle | push=1 | push_not_full |
| idle | (pop=1)&(count_in!=0) | pop_not_emp |
| idle | (push=1)&(count_in=250) | full |

Buttons: Add, Change, Delete, Move Up, Move Down, OK, Help, Cancel

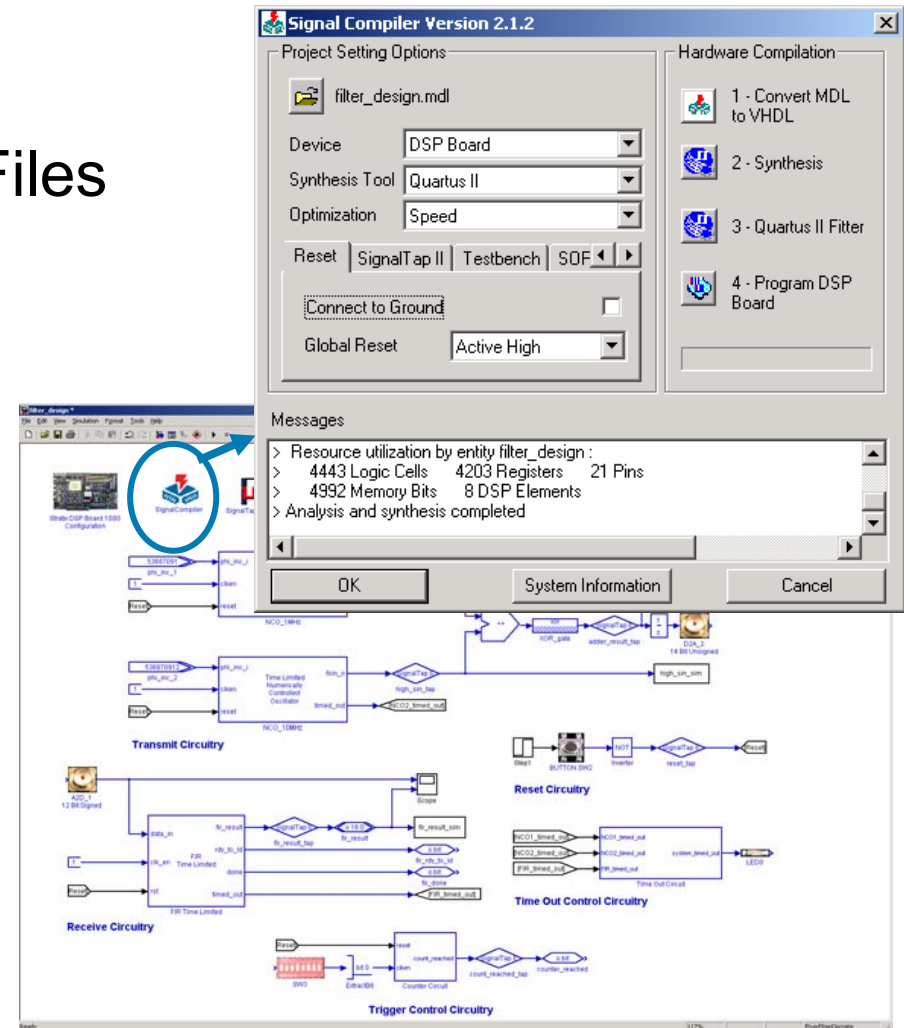
Sub-System Builder

- Import Existing VHDL Design into Simulink
- Simulink Simulation Options
 - Convert into DSP Builder Blocks or MATLAB Functions
 - Treat VHDL Design as Black Box

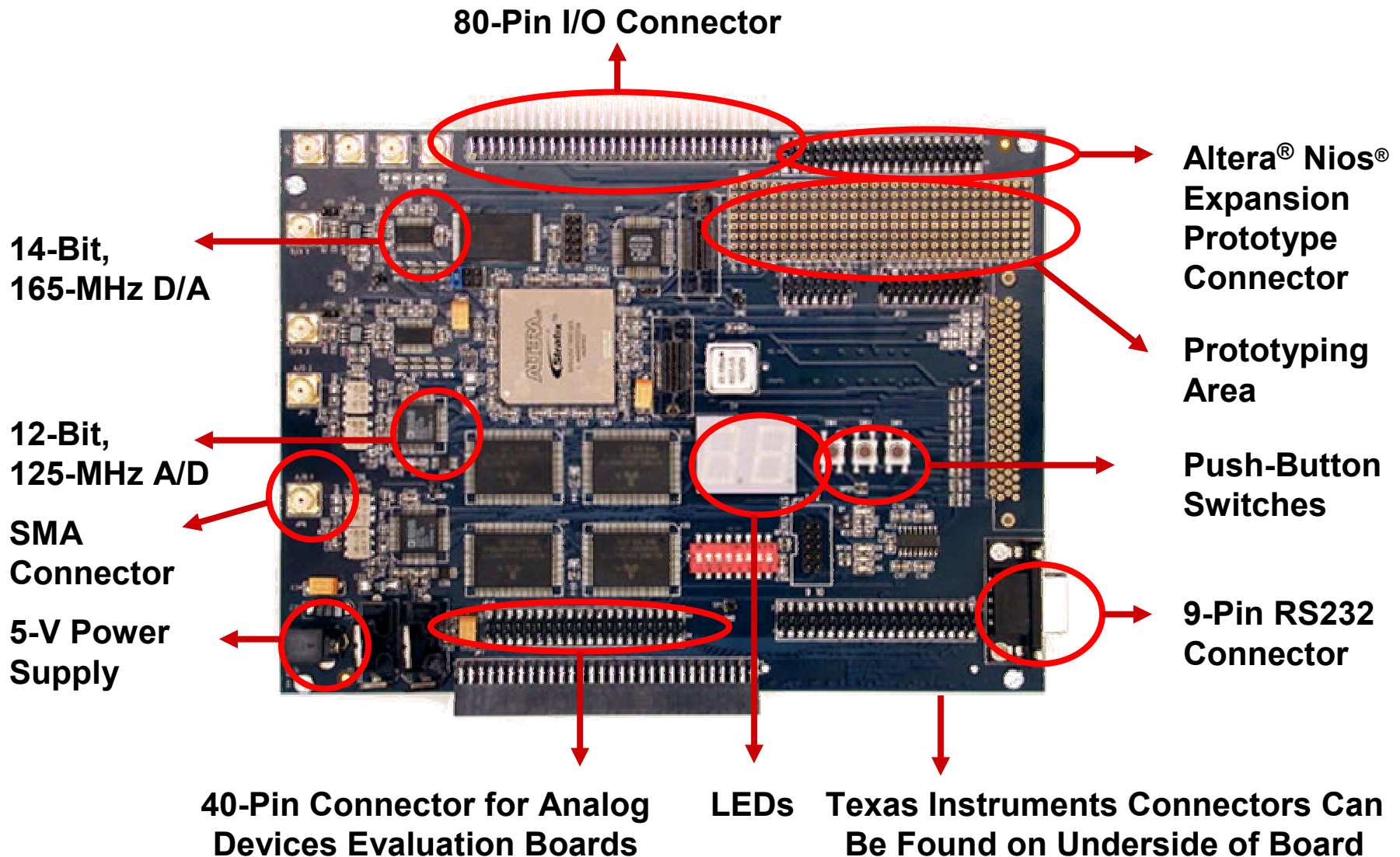


Signal Compiler

- Generates VHDL Design Files
- Generates Tool Command Language (Tcl) Scripts
- Generates Testbench
- Enables Parameterization of IP Blocks
- Launch Hardware Compilation from Simulink Cockpit

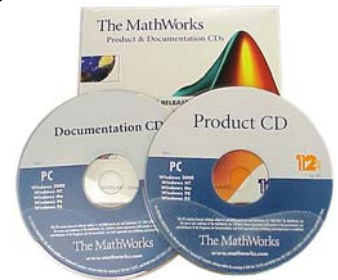
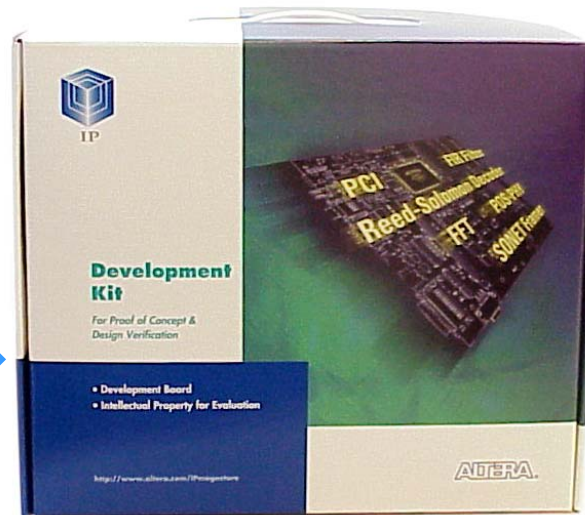
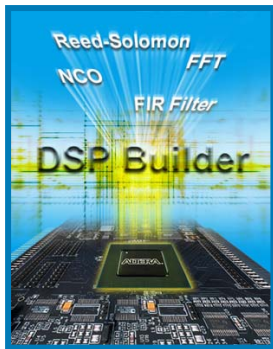


Stratix DSP Development Board

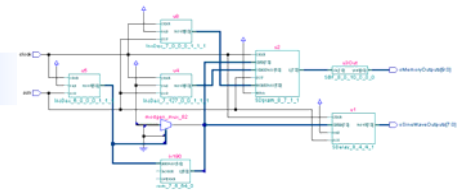


Altera DSP Development Kits

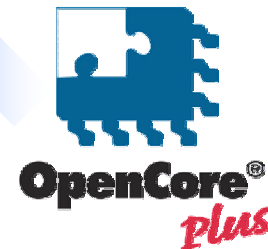
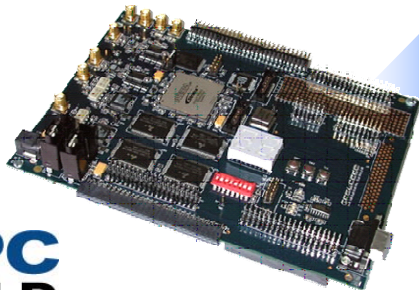
*Contains Everything You Need
to Develop High-Performance DSP
Designs on FPGAs*



**30-Day Evaluation
Version**



**System Reference
Designs**



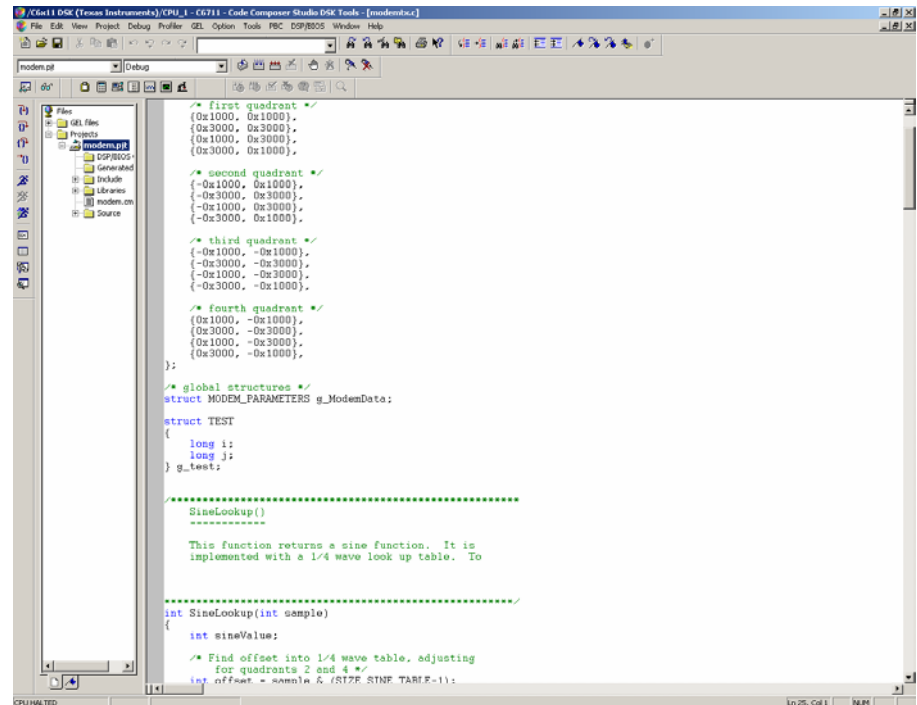


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QAM Modulator Co- Processor Design Example

Modem Reference Design

- Installed with Code Composer Studio As a Tutorial
 - C:\ti\tutorial\dsk6711\modem
- Used to Demonstrate CCS Functionality
- 16 QAM TX Modem



```
/* first quadrant */
{0x1000, 0x1000},
{0x3000, 0x3000},
{0x1000, 0x3000},
{0x3000, 0x1000},

/* second quadrant */
{-0x1000, 0x1000},
{-0x3000, 0x3000},
{-0x1000, 0x3000},
{-0x3000, 0x1000},

/* third quadrant */
{-0x1000, -0x1000},
{-0x3000, -0x3000},
{-0x1000, -0x3000},
{-0x3000, -0x1000},

/* fourth quadrant */
{0x1000, -0x1000},
{0x3000, -0x3000},
{0x1000, -0x3000},
{0x3000, -0x1000},
};

/* global structures */
struct MODEM_PARAMETERS g_ModemData;

struct TEST
{
    long i;
    long j;
} g_test;

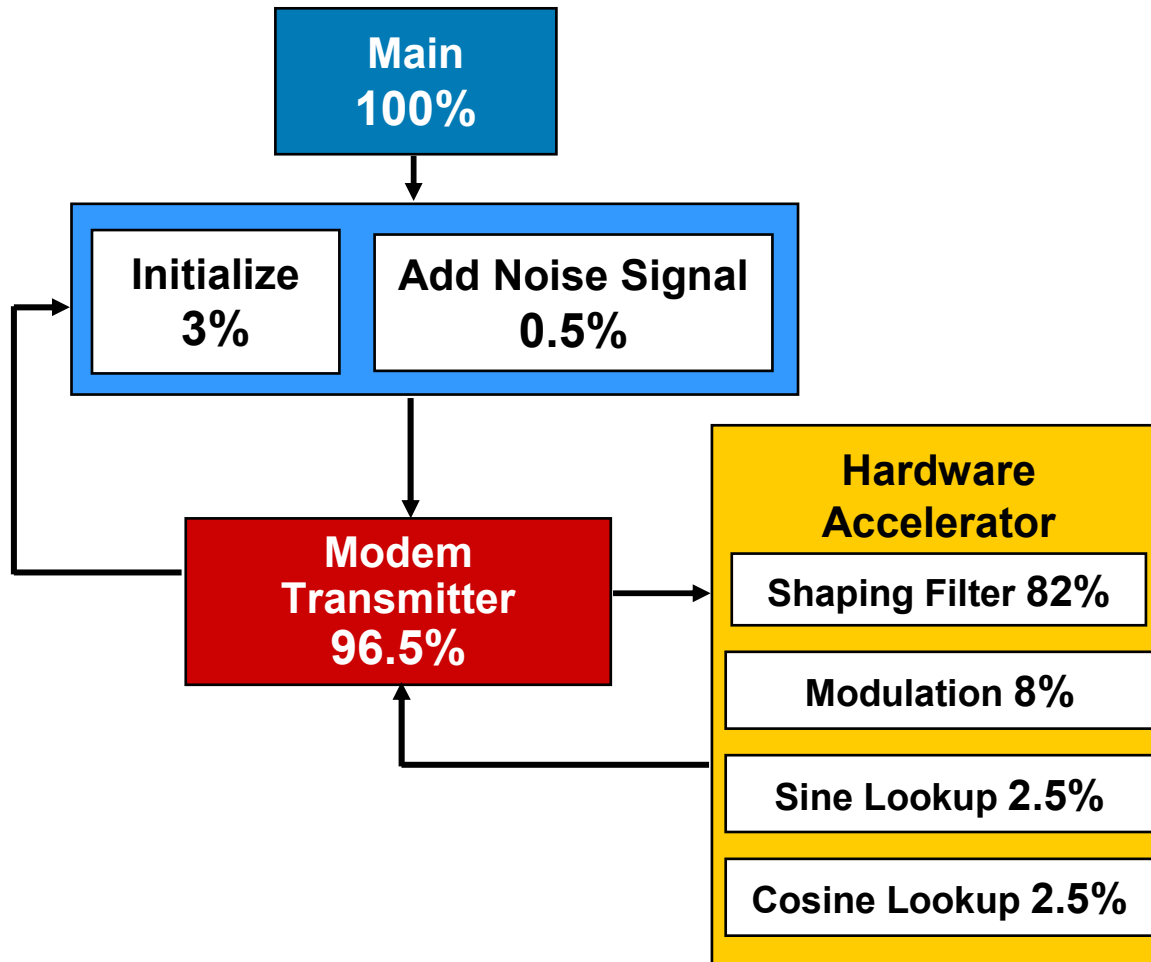
/*-----
SineLookup()
-----
This function returns a sine function. It is
implemented with a 1/4 wave look up table. To
-----*/
int SineLookup(int sample)
{
    int sineValue;

    /* Find offset into 1/4 wave table, adjusting
    for quadrants 2 and 4 */
    int offset = sample & (R17F_SINF_TABLE-1);
```

Modem Design Code Profile

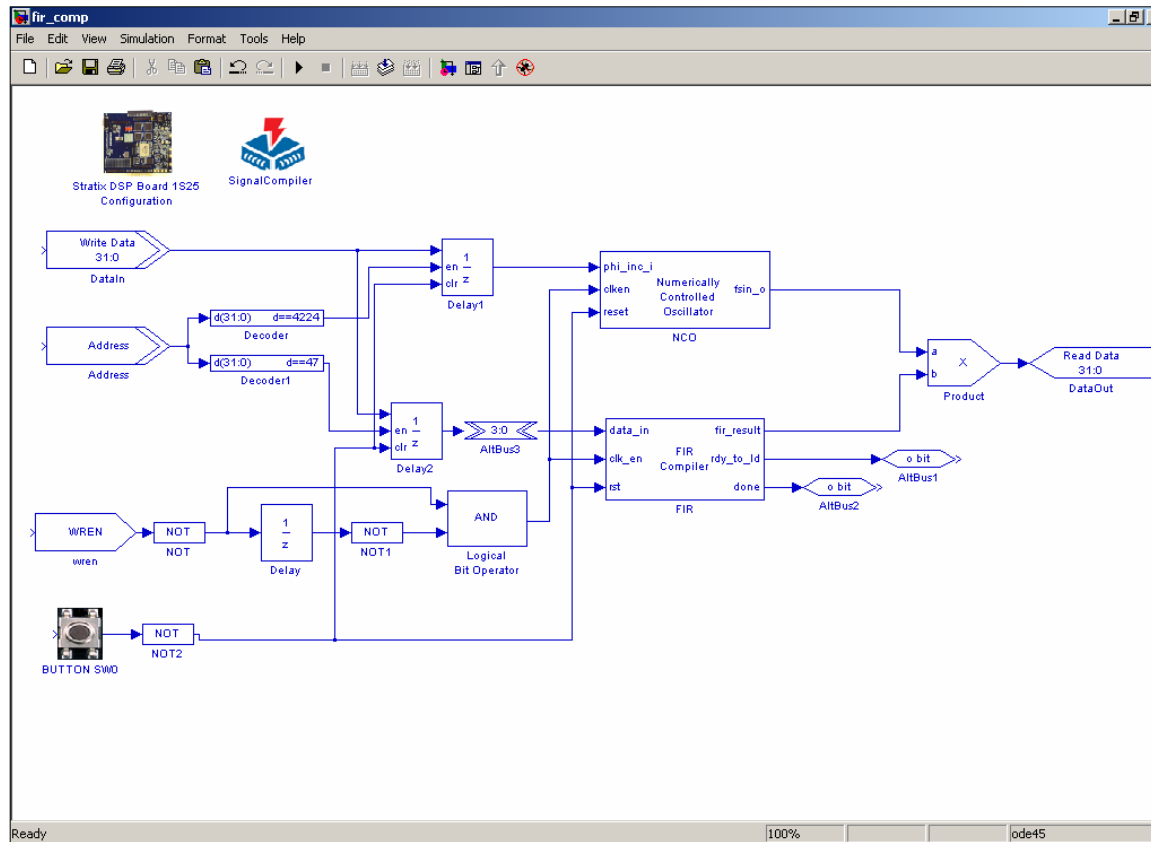
| Functions | Code Size | Count | Incl. Total | Incl. Maximum | Incl. Minimum | Incl. Average | Excl. Total |
|-------------------|-----------|-------|-------------|---------------|---------------|---------------|-------------|
| modem.out | | | | | | | |
| modemtx.c | | | | | | | |
| main | 548 | 1 | 4222002 | 0 | 0 | 4222002 | 23446 |
| ModemTransmitter | 304 | 7 | 4038331 | 580782 | 579499 | 576904 | 83981 |
| ShapingFilter | 356 | 14 | 3610811 | 258438 | 257493 | 257915 | 3610811 |
| Modulation | 236 | 213 | 341498 | 1656 | 1584 | 1603 | 97649 |
| SineLookup | 148 | 490 | 264817 | 615 | 493 | 540 | 264817 |
| Initialize | 636 | 1 | 117760 | 117760 | 117760 | 117760 | 117760 |
| CosineLookup | 56 | 245 | 143448 | 646 | 539 | 585 | 9065 |
| ReadNextData | 40 | 7 | 5692 | 820 | 808 | 813 | 259 |
| ReadConstellation | 40 | 7 | 5370 | 774 | 762 | 767 | 259 |
| AddNoiseSignal | 508 | 7 | 5048 | 728 | 716 | 721 | 5048 |

Modem Design Hardware/ Software Petition



Modulator Co-Processor

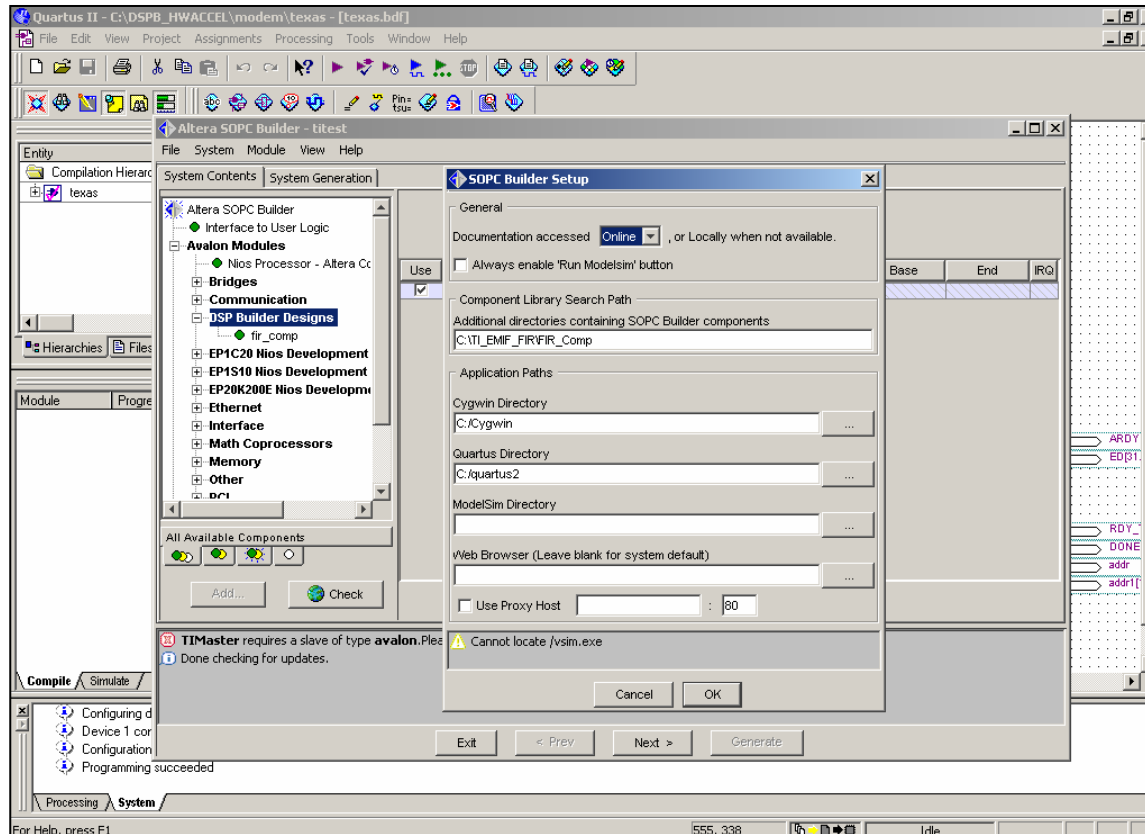
DSP Builder Used to Build Hardware DSP Data Path



The screenshot displays the Altera Sopc Builder - DSP_Builder interface. The top window shows the system configuration, including the Avalon Modules (Altera Nios 2.0 CPU, User-Defined Interface) and the System Clock Frequency (33.333 MHz). The bottom window shows the block diagram of the FIR filter, which includes components like the Write Data 31.0, Address, WREN, Delay, AND, Logical Bit Operator, Numerically Controlled Oscillator (NCO), FIR Compiler, and Read Data 31.0. The diagram is annotated with red circles and arrows, highlighting the data flow and control signals. The left sidebar shows the project hierarchy, including the Altera MegaCore Constellation Mapper and various compilers.

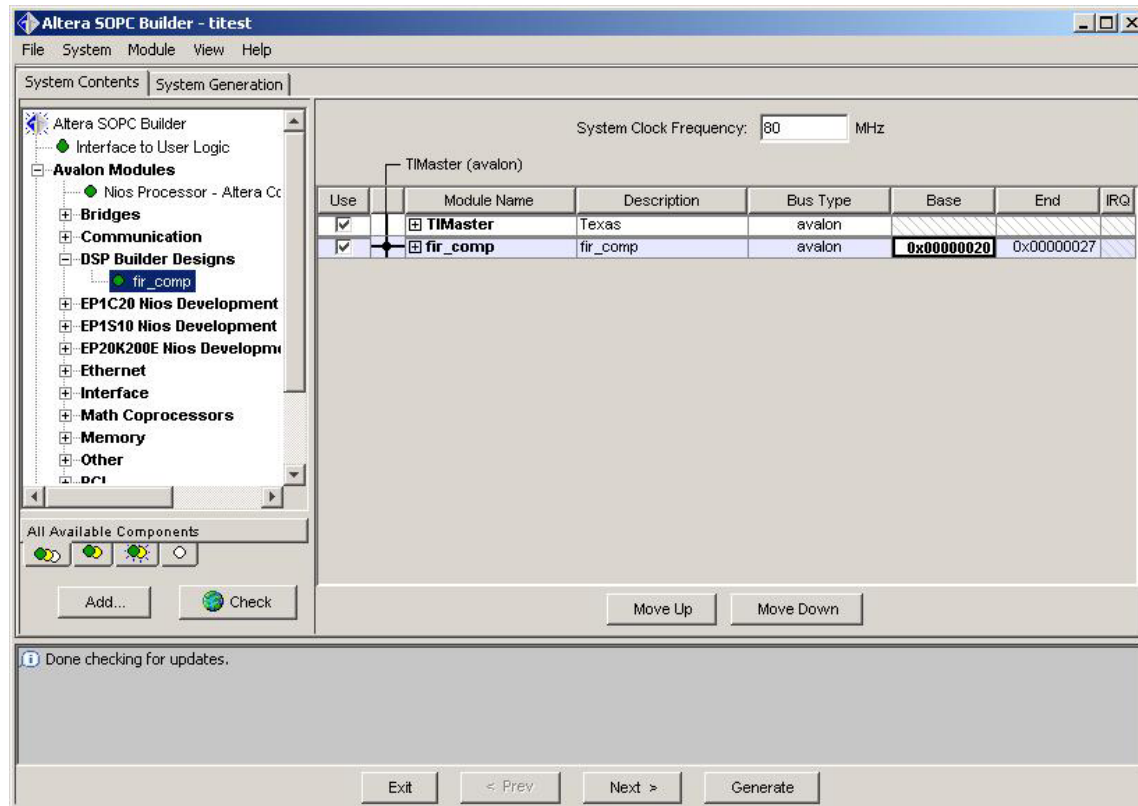
DSP Builder— SOPC Builder Import

Import DSP Builder Generated Co-Processor into SOPC Builder



SOPC Builder Integration

*Modem Co-Processor (fir_comp)
Integrated with TI EMIF I/F (TIMaster)*



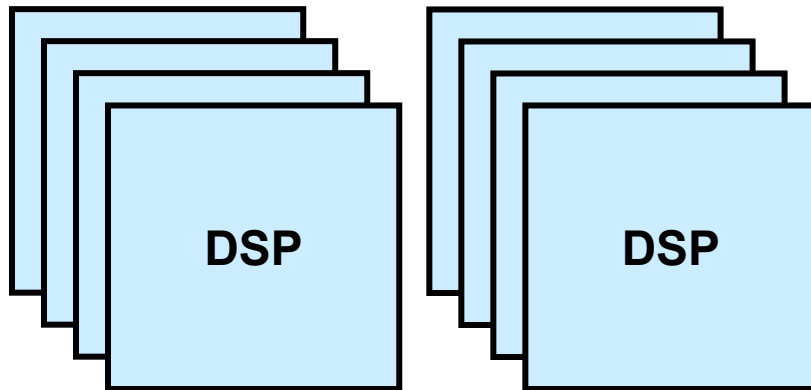


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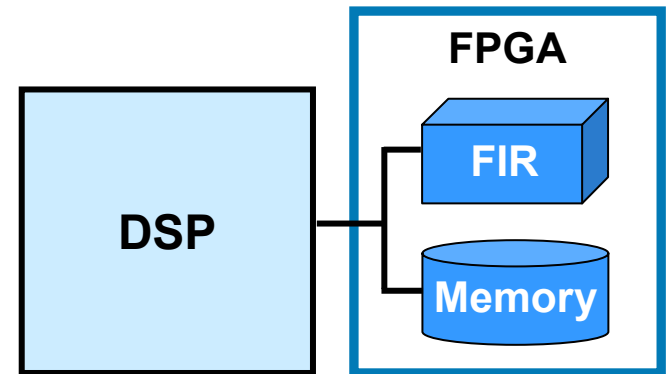
FIR Filter Co-Processor Design Example

Driving Down System Costs

Multi-Processing DSP



Digital Signal Processor + FPGA Co-Processor



FIR Co-Processor Design Example

■ FIR Parameters

- 128-Tap
- 16-Bit Data, 14-Bit Coefficients

■ Four FIR Implementations for Comparison

- TI C6711-Optimized TI DSPLib Function
- TI C6416-Optimized TI DSPLib Function
- Altera Eight-Cycle FIR Co-Processor
- Altera One-Cycle FIR Co-Processor

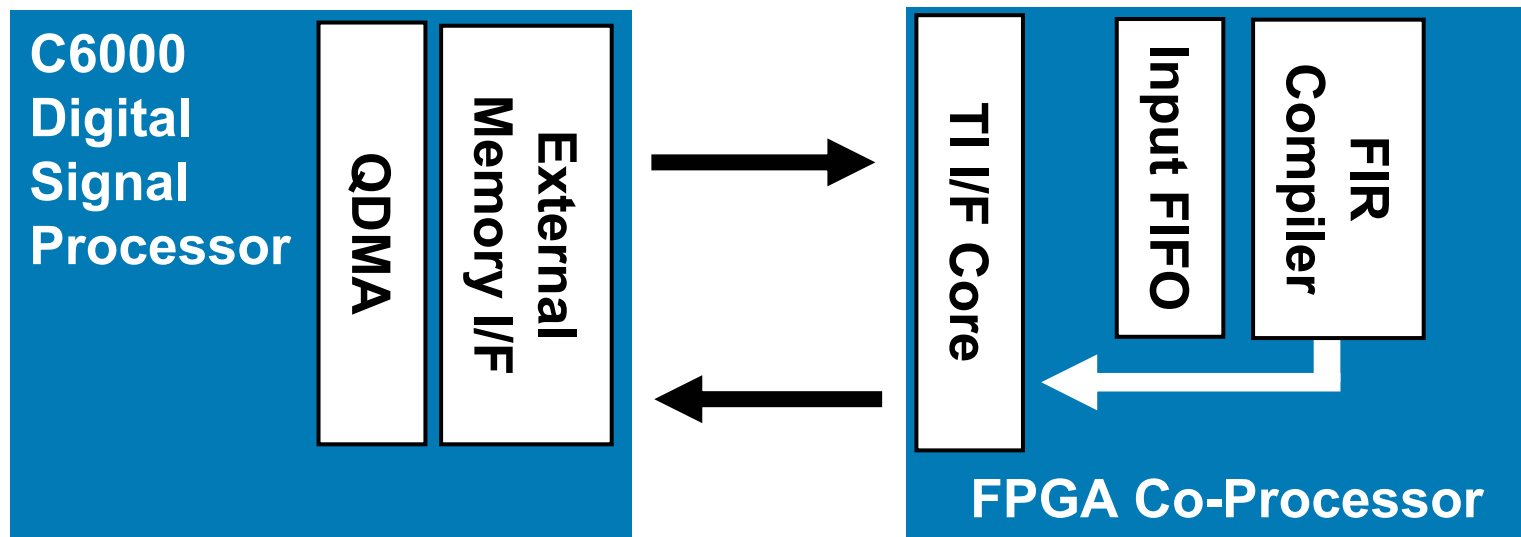
TI Filtering Library (DSP Lib)

- C-Callable Optimized Assembly Routines
- TI C67x DSPLib: Fir Filter (Radix 8)
 - Formula: $N_h * N_r / 2 + 13$
 - N_h = Number of Coefficients
 - N_r = Number of Samples
 - ~1 Sample/ 64 Cycles (128 Tap Filter)
- TI C64x DSPLib: FIR Filter (Radix 8)
 - Formula: $N_h * N_r / 4 + 17$
 - ~ 1 Sample/ 32 Cycles (128 Tap Filter)

Filter Co-Processor Design Example

■ Current Implementation

- 100 MHz, 32-Bit, Asynchronous EMIF on DSK
- TI Writes 300 Samples to Co-Processor (Input Data)
- Filter & Send Output to TI



FIR Filter Example* – 16X Cost/Performance Improvement

| Device | Solution | FIR Performance (MHz) | Device Cost**** | Cost per FIR MHz |
|-----------------|---------------------------|-----------------------|-----------------|------------------|
| TI C6713-200 | 64-Cycles** at 200 MHz | 3.125 | \$24.59 | \$7.87 |
| TI C6416-600 | 32-Cycles** at 600 MHz | 18.75 | \$160 | \$8.53 |
| Altera EP1C3-8 | 7-Cycles*** at 200 MHz | 28 | \$14 | \$0.50 |
| Altera EP1C12-8 | 1-Cycle*** at 170 MHz | 170 | \$84 | \$0.49 |

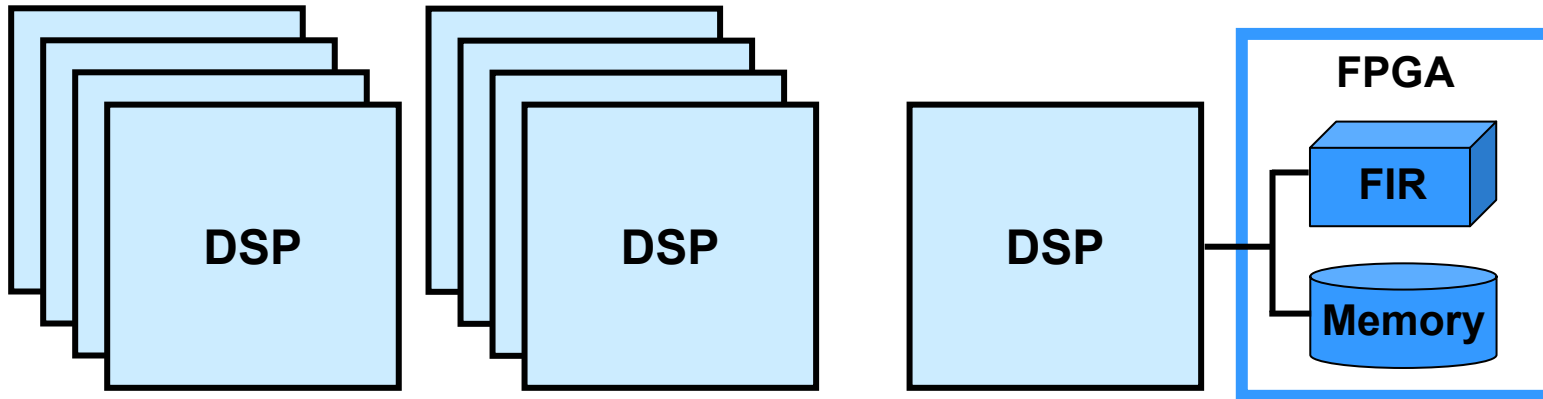
* FIR 128 Tap, 16-Bit Data, 14-Bit Coefficients

** DSPLib Optimized Assembly Libraries from Texas Instruments

*** Optimized MegaCore FIR Compiler from Altera

**** Pricing in Quantity of 100 at Arrow 6/25/03

14X Reduction in System Costs



| Architecture | FIR Performance (MHz) | Total FIR Performance (MHz) | Device Costs | Total Cost |
|----------------------------------|-----------------------|-----------------------------|--------------|------------|
| 9 * TI C6416-600 | 9 * 18.75 | 167 | 9 * \$160 | \$1,440 |
| Altera EP1C12-8 + 1 TI c6713-200 | 170 + 3 | 173 | \$84 + \$25 | \$110 |

Summary

- FPGA Co-Processors for DSP Offer Many Advantages
 - 10X Performance Boost
 - More Channels
 - More Complex Algorithms
 - Increased System Throughput
 - 10X Cost Reduction
 - Fewer Components
 - Complementary to DSP-Based Systems
 - Offloads Existing DSP
 - Integrates Into Existing DSP IDE
 - Evolution Not Revolution

Altera Code: DSP Solutions

- FPGAs
 - Stratix, Stratix GX, Cyclone
- Development Tools
 - DSP Builder, SOPC Builder
- Intellectual Property
 - FIR, FFT, Viterbi, Turbo, Reed Solomon, NCO
 - AMPP Third-Party Partners
- Development Kits
 - Altera
 - Third-Parties
- Design Services
 - ACAP Third-Party Partners
- Training



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