SOPC WORLD 2004

Ensuring Success in High-Speed System Design

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Today's-High Speed Systems

- High-Speed Designs Require Faster Devices & Increasing Data Widths
- Wide Data Buses Demand Higher I/O Pin Count
- Faster Devices Exhibit Faster Edge Rates
- A Memory Interface is a Typical Example for Such a System

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Agenda

- Memory Interface Design
- Simultaneously Switching Outputs
- Altera Design Resources
- References

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Memory Interface Design

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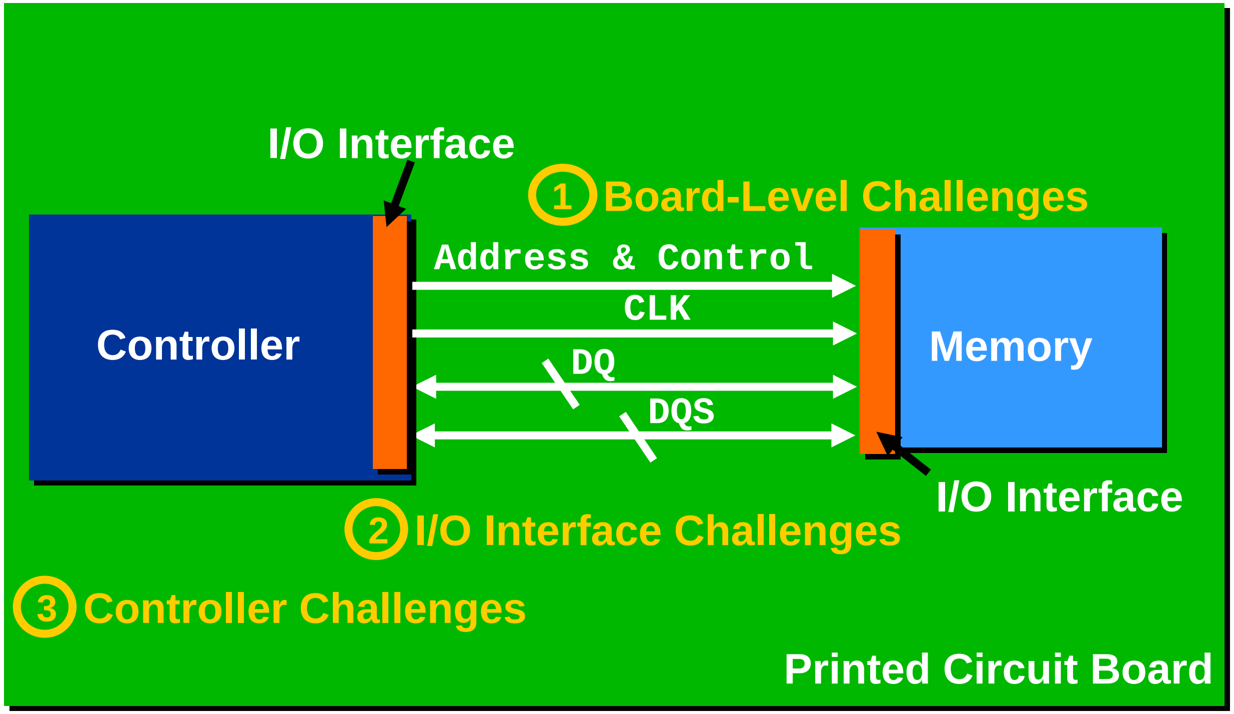
Memory Interface Design Challenges



The Higher the Frequency, the Greater the Design Challenge

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Altera Memory Interface Solutions

Challenge	Altera Resolution
Board-Level Challenges	■ Simultaneous Switching Outputs (SSO) Guidelines ■ Fully Verified Hardware Reference Platforms with Gerber Files ■ Termination Recommendations & Board Design Guidelines ■ SPICE & IBIS I/O Simulation Models
I/O Interface Challenges	■ DQS Phase Shift Circuitry in Stratix® Series FPGAs ■ Detailed Timing Margin Analysis for Non-IP Users ■ Fully Optimized Memory Controller Intellectual Property (IP) Cores with Automatic Timing Analysis for IP Users
Controller Design Challenges	■ Fully Optimized Memory Controller IP Cores with Automatic Timing Analysis & Functional Simulation Capabilities ■ Feature-Rich Phase-Locked Loops (PLLs) to Manage Clocks

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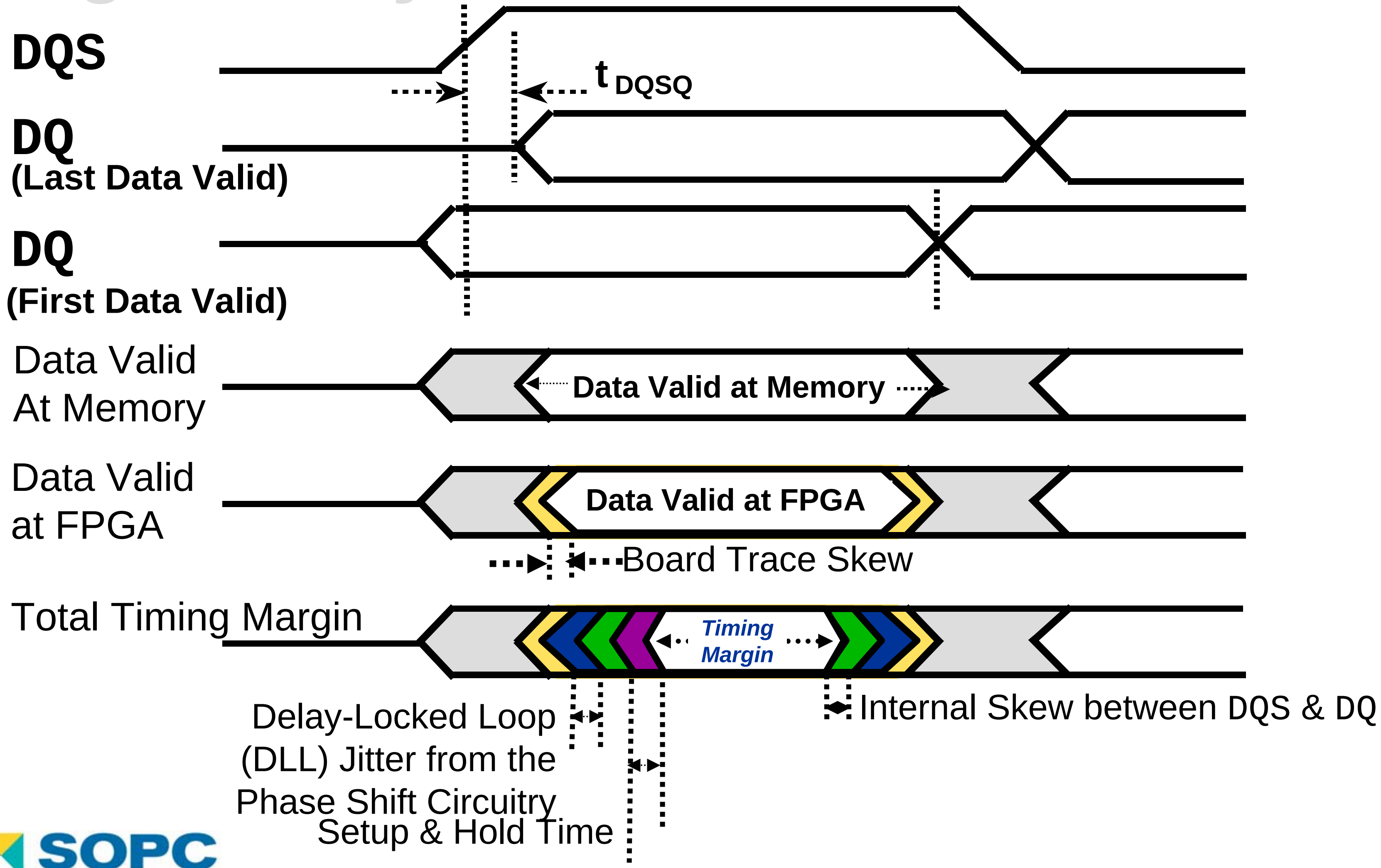
Example: DDR2 Read Timing Margin Analysis



DQS

t_{DQSQ}

DQ
(Last Data Valid)

DQ
(First Data Valid)

Data Valid
At Memory

Data Valid at Memory

Data Valid
at FPGA

Data Valid at FPGA

Board Trace Skew

Total Timing Margin

Timing Margin

Internal Skew between DQS & DQ

Delay-Locked Loop
(DLL) Jitter from the
Phase Shift Circuitry

Setup & Hold Time

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Signal Integrity & Board Design

Design Item	Effect on Performance/Reliability of the System
Bus Width	Increasing Bus Width Increases SSO Noise & also Increases Board Design Complexity
Noise	Causes Bit Errors, Effects Signal Integrity & Degrades Performance & Reliability
Loading	Increasing Number of Devices or Modules will Reduce Performance
Termination Scheme	Termination Scheme & Resistor Values Affect Signal Quality & Performance

Board Simulations Should be Performed to Check for Signal Integrity

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Simultaneously Switching Outputs

- Increased Bus Width, Pin I/O Counts & Inherent Package Trade-Offs Can Introduce More SSO Noise
  - I/O Count vs. I/O Drive Strength
- An FPGA Offers the Flexibility to Employ Reduction Techniques to Minimize Detrimental Effects of SSO

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Simultaneous Switching Outputs (SSO)

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Components of SSO Noise

- Ground Bounce
- Power Bounce Commonly Referred to as Vcc Sag

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What is SSO Noise?

- Ground Bounce & Vcc Sag are Voltage Fluctuations on a Static Signal (Quiet) as a Result of High Current Change (di/dt) from Nearby I/O Buffer Circuitry that Share Common Ground (Vcc) Return Paths
- Ground Bounce Affects Static Low Signals;
  Vcc Sag Affects Static High Signals
- Enough Ground Bounce or Vcc Sag on a Static Signal May Cause Sampling of Wrong Data, Depending on:
  - I/O Standard Used
  - Available Noise Margin
  - Amount of Ground Bounce
  - When the Signal is Sampled

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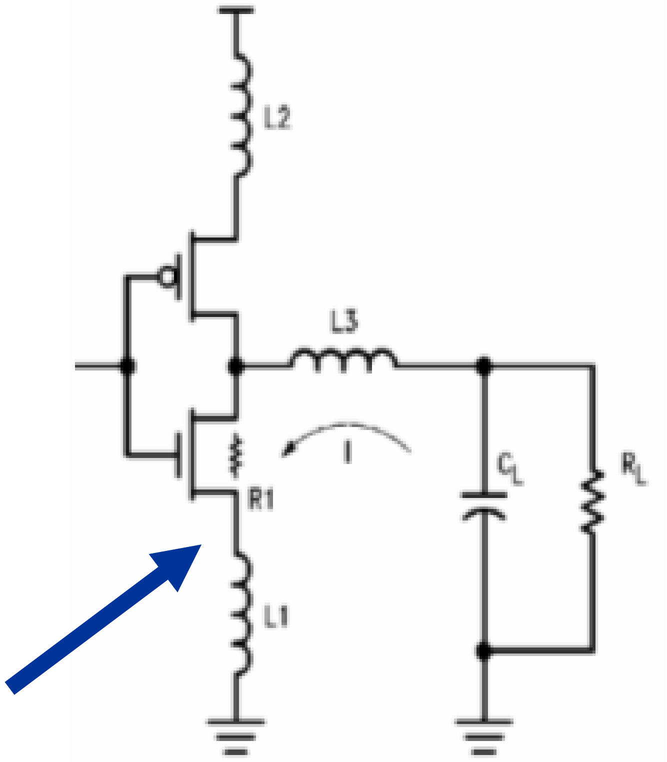
Ground Bounce Circuit Model

- L1 is Lumped Inductance for Die, Bump, Package, & Ball
- Output Buffer Current

  i(t) = C * dv/dt
- Voltage Across L1

  v(t) = L * di/dt
- High-to-Low Transitions on Output Raises Local Ground V



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Ground Bounce Circuit Model

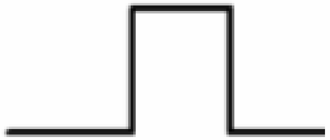
- Key Equations

  $i(t) = C * dv/dt$

  $v(t) = L * di/dt$

- Output Voltage (b) with Certain Slew Rate
- Induces Current (c) through Pull-Down Transistor & L1
  - Ideal Waveform
- Creates Voltage Ground Bounce (d) in Local Ground, through Other Quiet Low Outputs via NMOS Transistors

b. Output Voltage (V)



c. $I = -C_L \cdot (\Delta V/\Delta t)$

d. $V_{GB} = L \cdot (\Delta I/\Delta t)$

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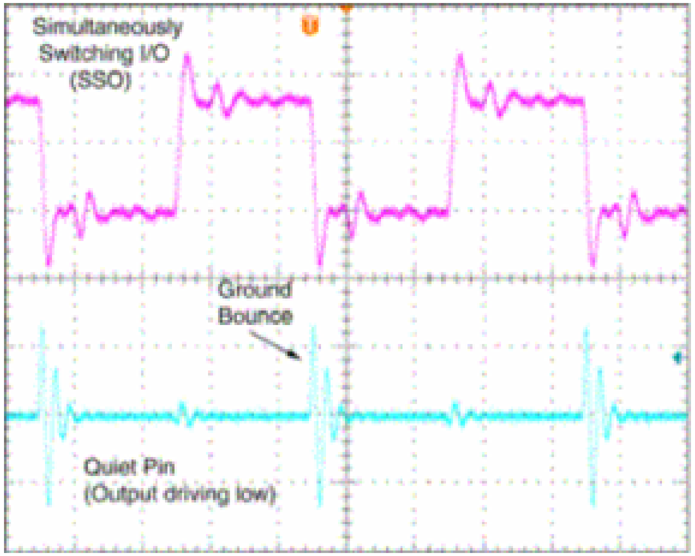
Impact of Ground Bounce (cont.)

- If Enough Outputs Switch Simultaneously to Induce 0.8V of Ground Bounce on a Nearby “Victim” Pin, that Pin Momentarily Glitches to 0.8V
  - 3.3-V LVTTL, Maximum V_{IL} is 0.7V

- If Victim Pin is Clocked During the SSO Event, the Sampled Value May Be Wrong
  - Similarly Applies to Vcc Sag & V_{IH} Minimum.



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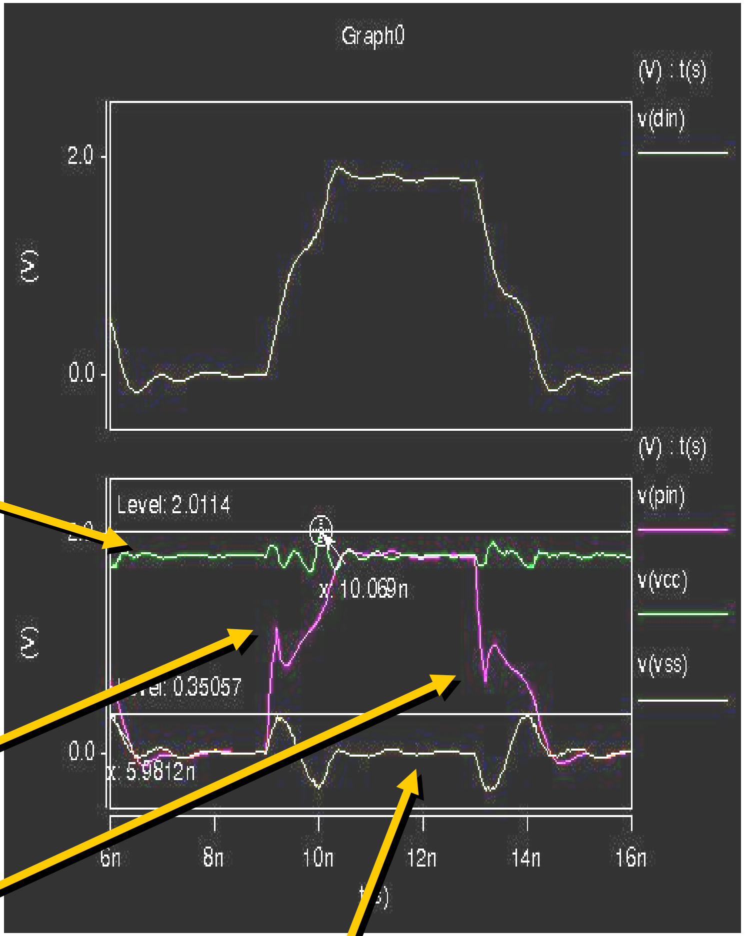
Impact of Ground Bounce

- Ground Bounce
  - Effects Worse than Power Bounce
  - Can Cause Logic 1 Instead of 0 in Extreme Cases
- Vcc Sag
  - Causes Drop in Power Supply
  - Can Affect Outputs
- Both Cause Degradation in Waveforms



Power

Due To Power Bounce

Due Ground Bounce

Ground

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Elements That Contribute To SSO Noise

- Package:
  - Number of Power/Ground Pins
  - Reference Planes
  - Decoupling
  - Package Type (Flip-Chip vs. Wirebond)
    - Majority of SSO Noise Occurs at Package Level
- Board:
  - Decoupling Capacitors
  - Power Ground Planes
  - Sockets
  - Vias

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Packaging

- Wire-Bond: Lacks Referencing Structures for Every Signal Trace, thus Contributes to Overall High Inductance
- Flip-Chip: Signal Bumps Enter the Package Laminate without Having to Traverse through Long, Unreferenced Wire-Bonds

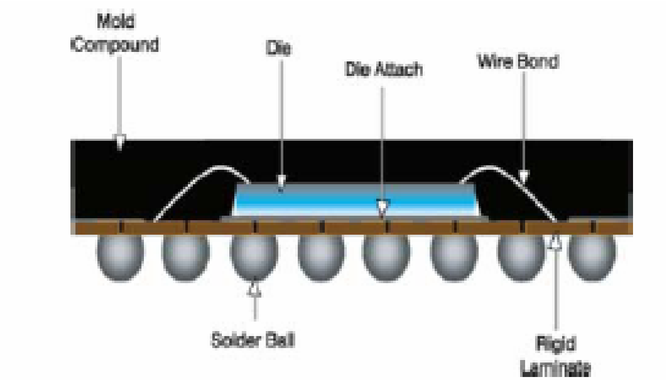

Figure 1.6 – Wire bond package cross section

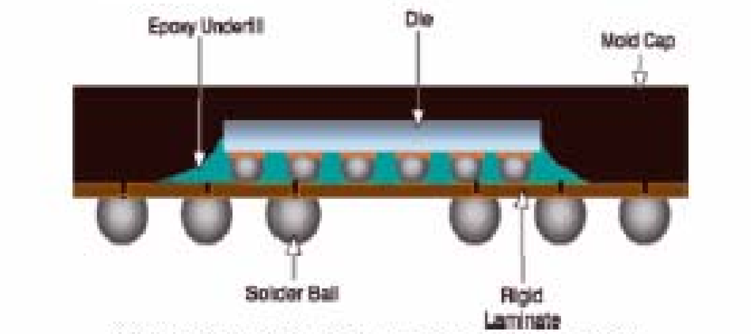

Figure 1.7 – Flip Chip package cross section

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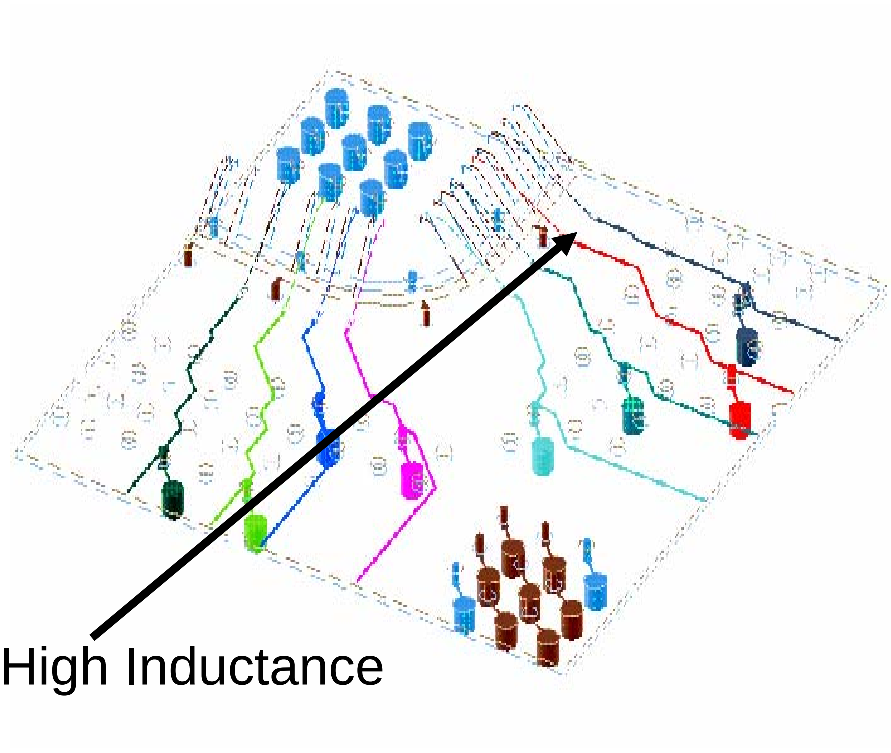
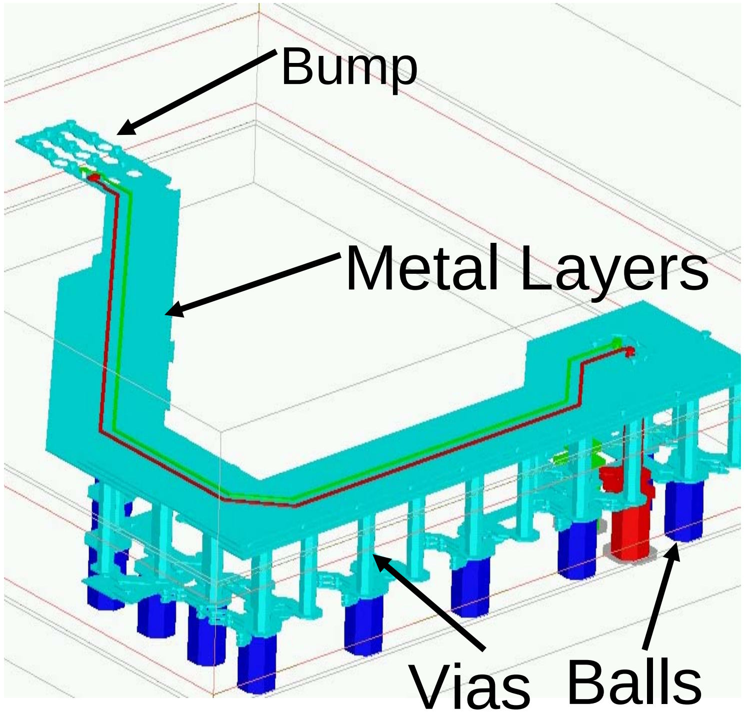
Packaging

Flip-Chip Vs. Wire-Bond



Wire-Bond



Flip-Chip

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Techniques For Reducing SSO Noise

- Use Flip-Chip Package
- Add/Utilize Better Return Paths
  - Use Unused I/O Pins as Programmable Vcc & GND
- Use Lower Drive Strength
- Use Slow Slew Rate (SSR) vs. Fast Slew Rate (FSR)
- Proper I/O Pin Selection
- Add Decoupling Capacitors & on Board Power Ground Capacitance
- Proper Trace Layout
- Remove Sockets
- Use On-Chip Termination

All Techniques Verified Using
Stratix® & Stratix GX Reference Boards

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Utilize Unused I/O Pins as Programmable Vcc & GND

# of I/O Pins Switching	Ground Bounce (mV)	Vcc Sag (mV)
20: All Pins Switching	650	1,020
20: Every Other I/O Pin switching	490	910
20: Every Other I/O Pin Switching & Every Other Tied to Ground	364	820
20: Every Other I/O Pin Switching & Every Other Tied to Power	490	700
24: Every Third I/O Pin Switching, Every Third Tied to Power & Every Third Tied to Ground	300	320

Results For 24 mA LVTTL I/O Pins

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Use Lower Drive Strength

# of I/O Pins Switching	Drive Strength	Ground Bounce (mV)	Vcc Sag (mV)
20: All I/O Pins Switching	24 mA	650	1,020
20: All I/O Pins Switching	12 mA	456	730
20: All I/O Pins Switching	4 mA	328	660

Results For LVTTL I/O Pins

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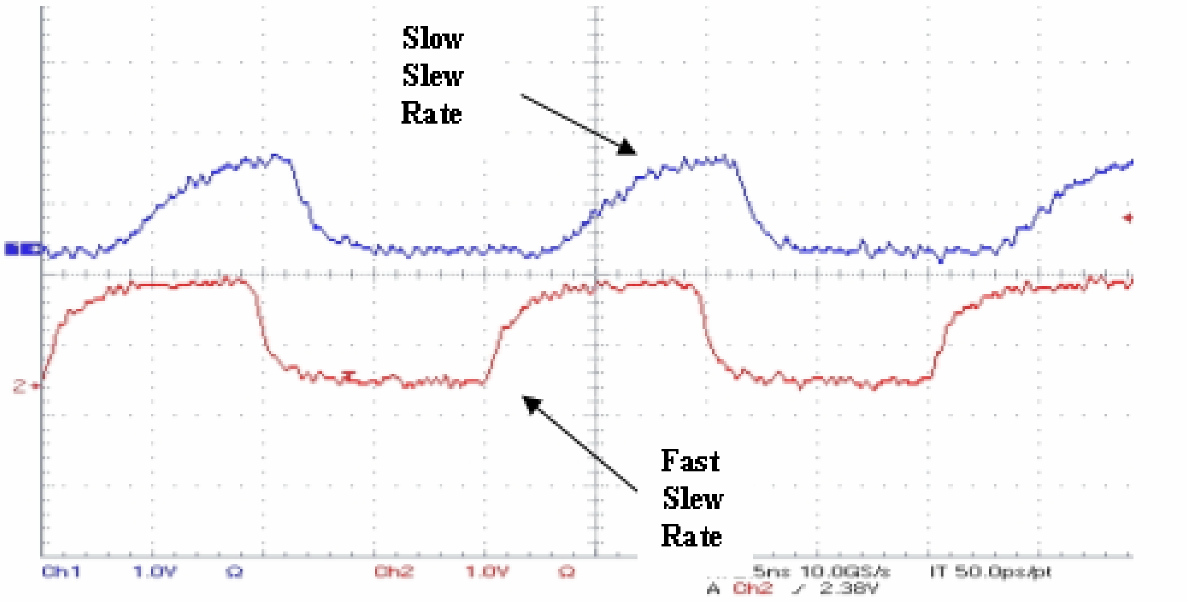
Turn on Slow Slew



8 mA Drive Strength, 40 3.3-V LVTTL I/O Pins, Switching Simultaneously

Switching	With Fast Slew Rate	With Slow Slew Rate
Bounce (mV)	288	200
Vcc Sag (mV)	620	310

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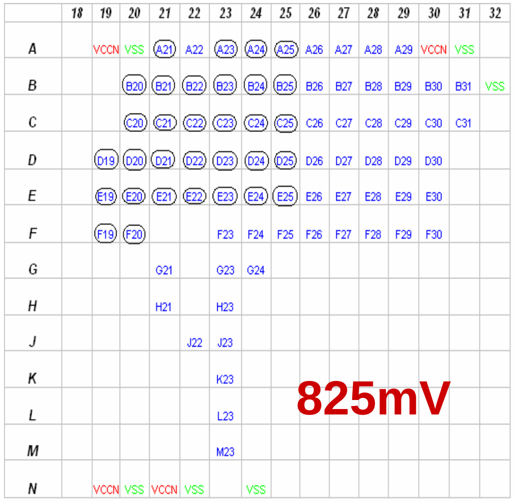
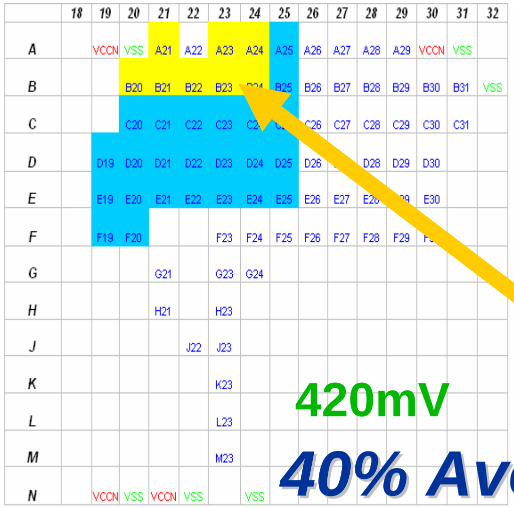
Delay Shift SSO pins



	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

825mV



	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	[illegible]	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	[illegible]	[illegible]	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	[illegible]	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	[illegible]	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	[illegible]		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

420mV

32 SSO, w/ 8 pins delayed by 3ns (in yellow)

40% Average Reduction!

- Reduces Current Density
- Add PLL Phase Shift, or Add Output Timing Delays

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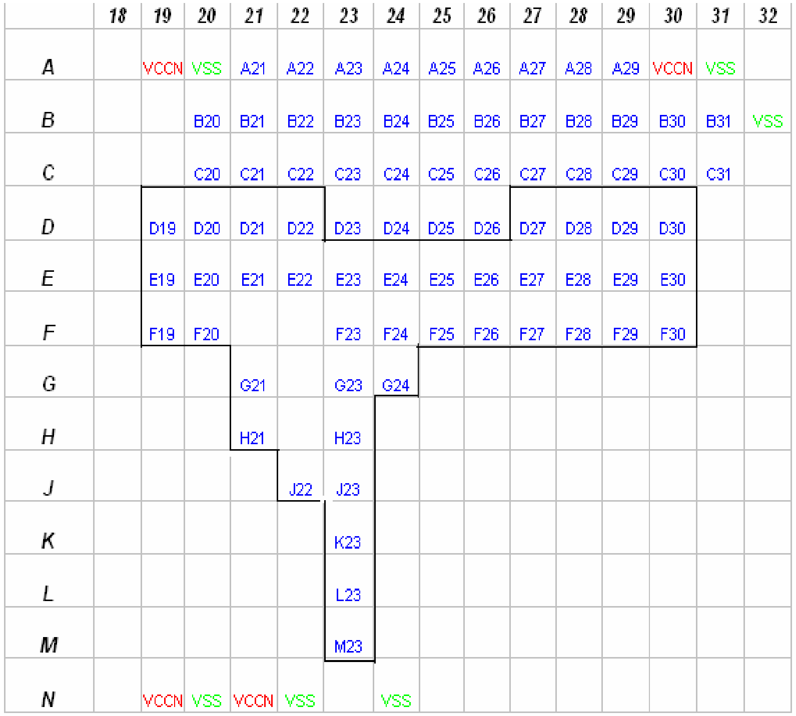
Spread Out Selected I/O Pins



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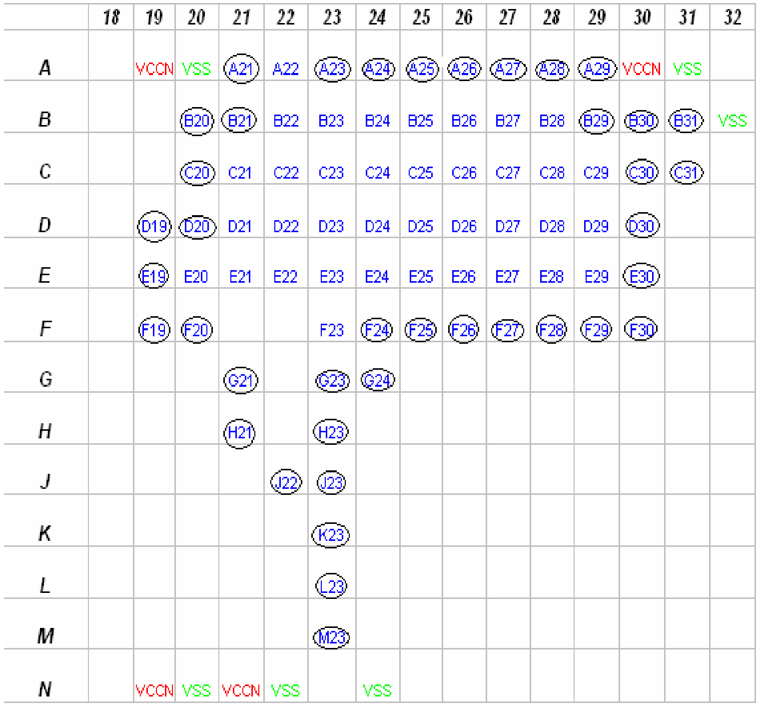
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								



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A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

Bounce = 570
Sag = 1,017 mV

Bounce = 412
Sag = 810 mV

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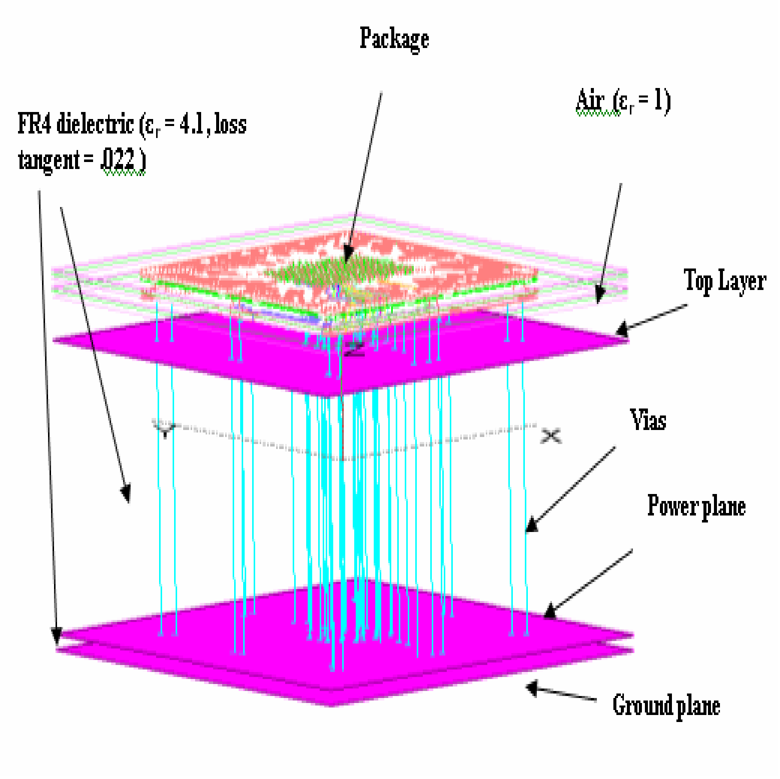
On-Board Power Ground Capacitance

- Solid Power & Ground Planes

Configuration	**Ground Bounce**
Ground/Power, 140 mils from IC, 6 mils Apart	370 mV
Ground/Power, 20 mils from IC, 6 mils Apart	248 mV
Ground/Power, 20 mils from IC, 4 mils Apart	228 mV



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Decoupling Capacitors

- Decoupling Capacitors Provide Localized Power Supply
  - Capacitance Stores Energy & Provides It When There Is Transient Requirement
- When Solid Power/Ground Sandwich Present, High Frequency on Board Capacitors Can Be Useless if Path to IC Is Very Inductive
- Bigger Capacitors Are Effective for Lower Frequency Noise

Stratix II FPGAs Offer On-Chip Decoupling, an Optimal Solution to Provide Better Return Paths

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Other Techniques

- Don’t Use Any Sockets between IC & Board
  - Reduces Inductance
- Differential Signaling Helps with SSO
  - Traces Should Be Tightly Coupled
- Series On-Chip Termination Reduces SSO by Absorbing Reflections
  - Slows Edge Rate

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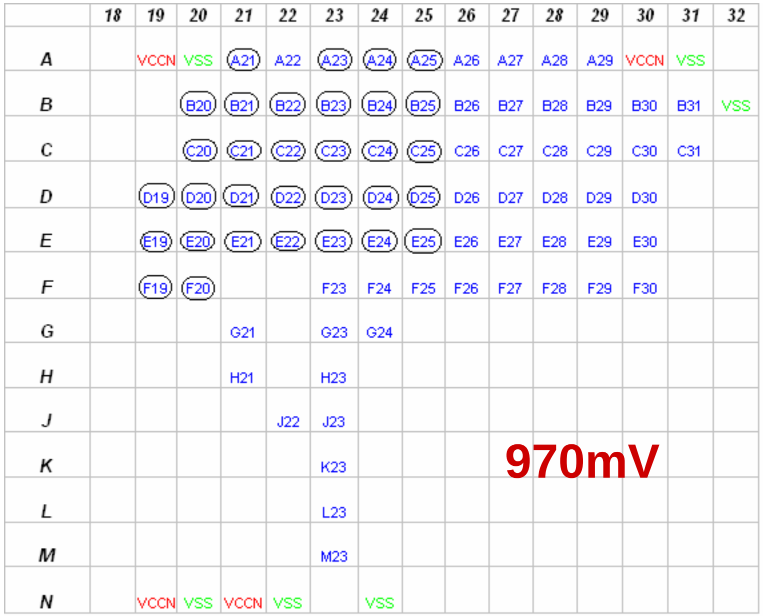
Worst Case (Before Optimization)

- Combination of Several Factors Can Significantly Reduce Ground Bounce & Vcc Sag Noise



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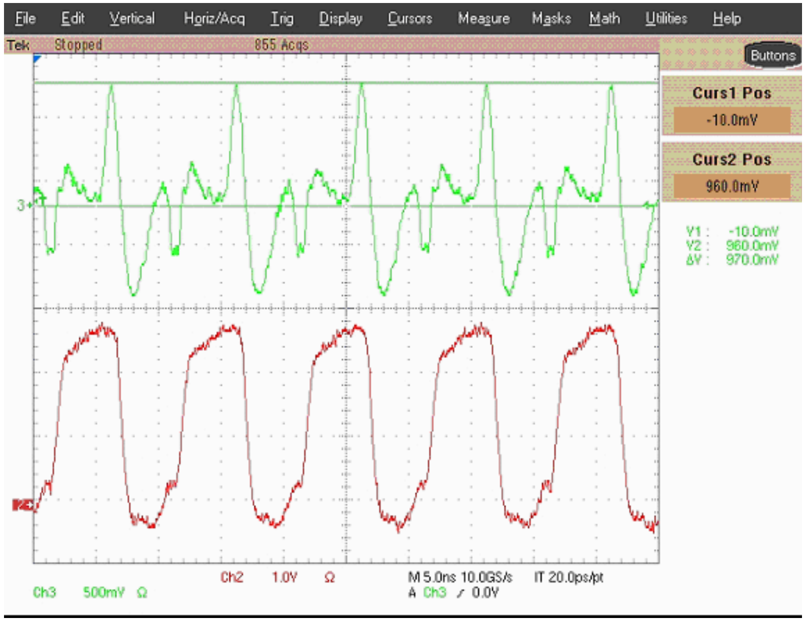
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

970mV



Curs1 Pos: -10.0mV

Curs2 Pos: 960.0mV

V1 : -10.0mV
V2 : 960.0mV
ΔV : 970.0mV

Ch2 1.0V Ω
Ch3 500mV Ω
M 5.0ns 10.0GS/s IT 20.0ps/pt
A Ch3 ⟋ 0.0V

40 SSO Pins, 24-mA Current Drive, FSR, No Delay, No Programmable Grounds

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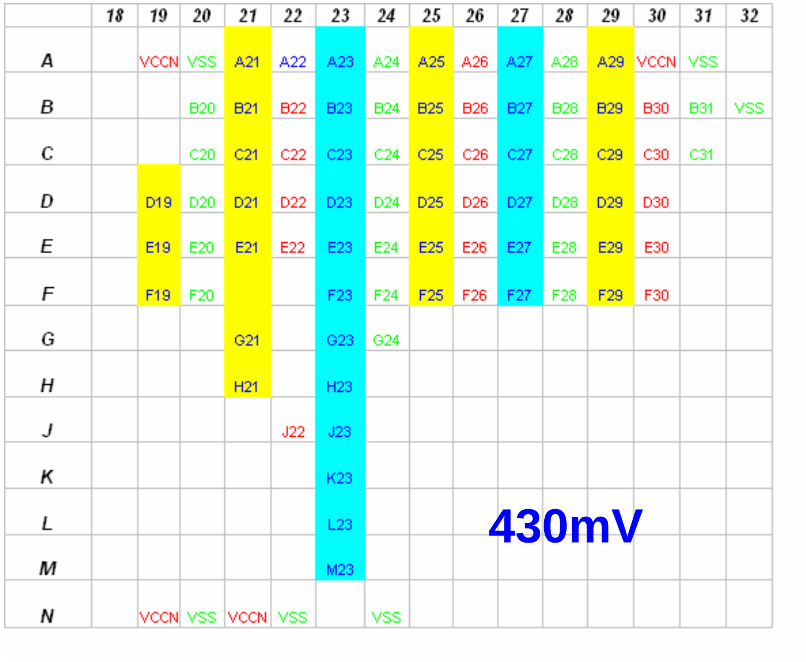
Nominal Case



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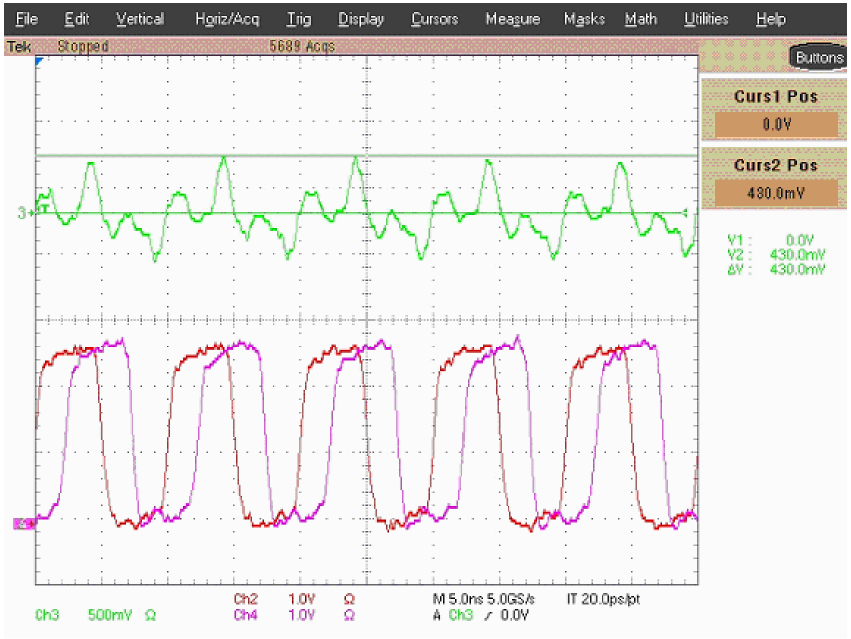
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

430mV



Curs1 Pos 0.0V
Curs2 Pos 430.0mV
V1: 0.0V
V2: 430.0mV
ΔV: 430.0mV

Ch3 500mV Ω
Ch2 1.0V Ω
Ch4 1.0V Ω
M 5.0ns 5.0GS/s
A Ch3 ⟋ 0.0V
IT 20.0ps/pt

40 SSO Pins, 36 Interleaved Programmable Powers (Red) & Grounds (Green), 16-mA Current Drive, FSR, 22 Pins with 3-ns Delay (Yellow)

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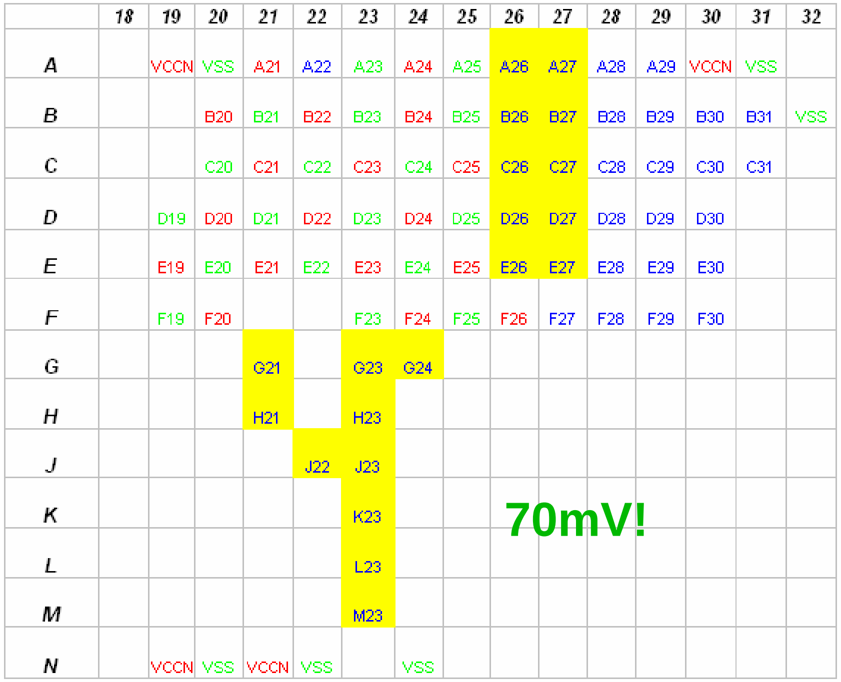
Best Case



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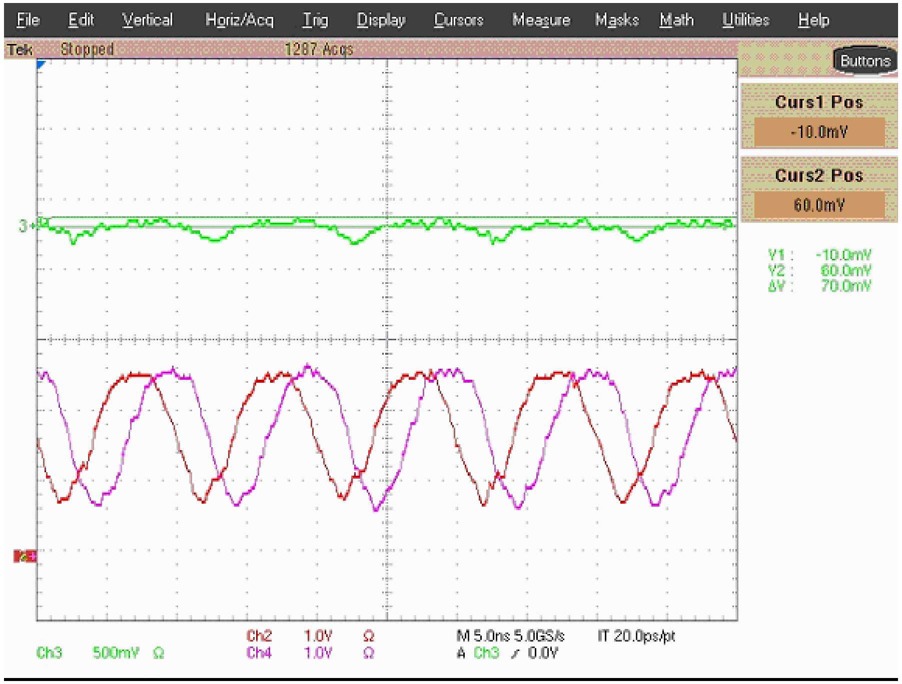
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

70mV!



Curs1 Pos -10.0mV

Curs2 Pos 60.0mV

V1 : -10.0mV
V2 : 60.0mV
ΔV : 70.0mV

Ch2 1.0V Ω
Ch4 1.0V Ω
Ch3 500mV Ω
M 5.0ns 5.0GS/s IT 20.0ps/pt
A Ch3 ⟋ 0.0V

40 SSO Pins Far Away, 36 Programmable Powers (Red) & Grounds (Green) around Quiet Pin, 4-mA Current Drive, SSR, 20 Pins with 3-ns Delay

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Altera Design Resources

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Modeling

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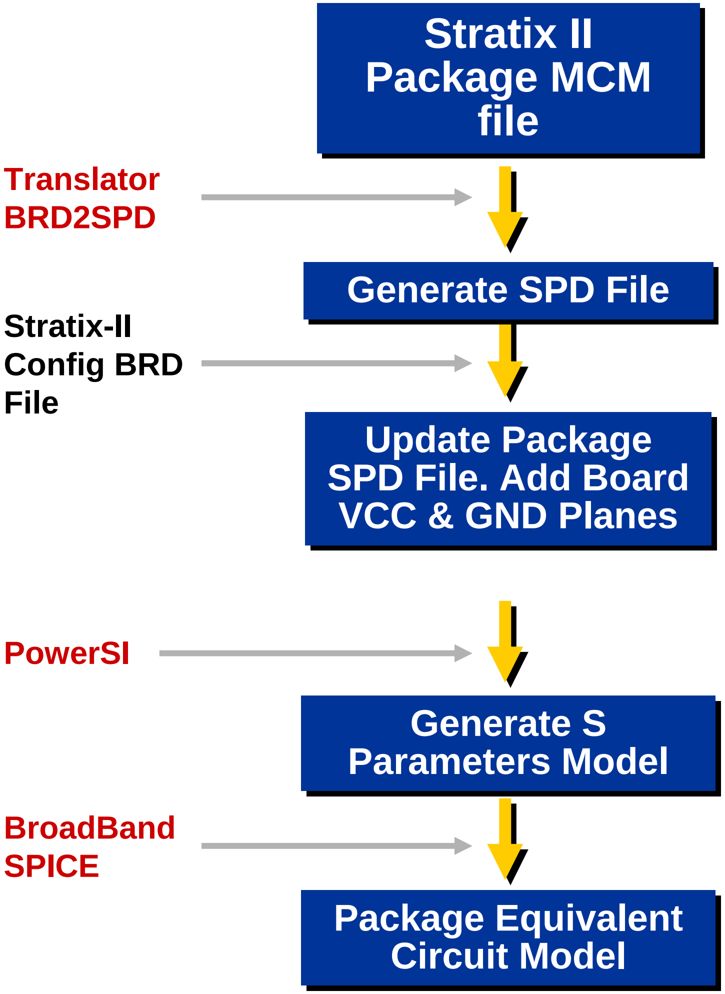
Objective of SSO Modeling

- Explore, Derive & Verify a Robust Methodology that Can Be Consistently Used in Future SSO Analysis
- Simulate & Correlate the Results Obtained from Lab Measurements
- Generate & Validate Simulation Models that Can Be Used as a Black Box for ‘what-if’ Analysis

SSO Model Extraction Flow

- Translation of Database
  - Translate Package MCM File into Sigrity SPD Format
- Structure Verifications/Modifications
  - Verify Stackup, Material Properties, Plane Shape, Via/Trace Dimensions
  - Add Board VCC & Ground Planes
  - Others
- Mesh Settings
  - Add Solder Ball Vias
- Error Corrections
- Coupled Line Selection
- Define Ports
- Pre-Simulations Tests
  - DC Test
  - AC Test
  - Signal Transmission Test



Stratix II Package MCM file

Translator BRD2SPD

Generate SPD File

Stratix-II Config BRD File

Update Package SPD File. Add Board VCC & GND Planes

PowerSI

Generate S Parameters Model

BroadBand SPICE

Package Equivalent Circuit Model

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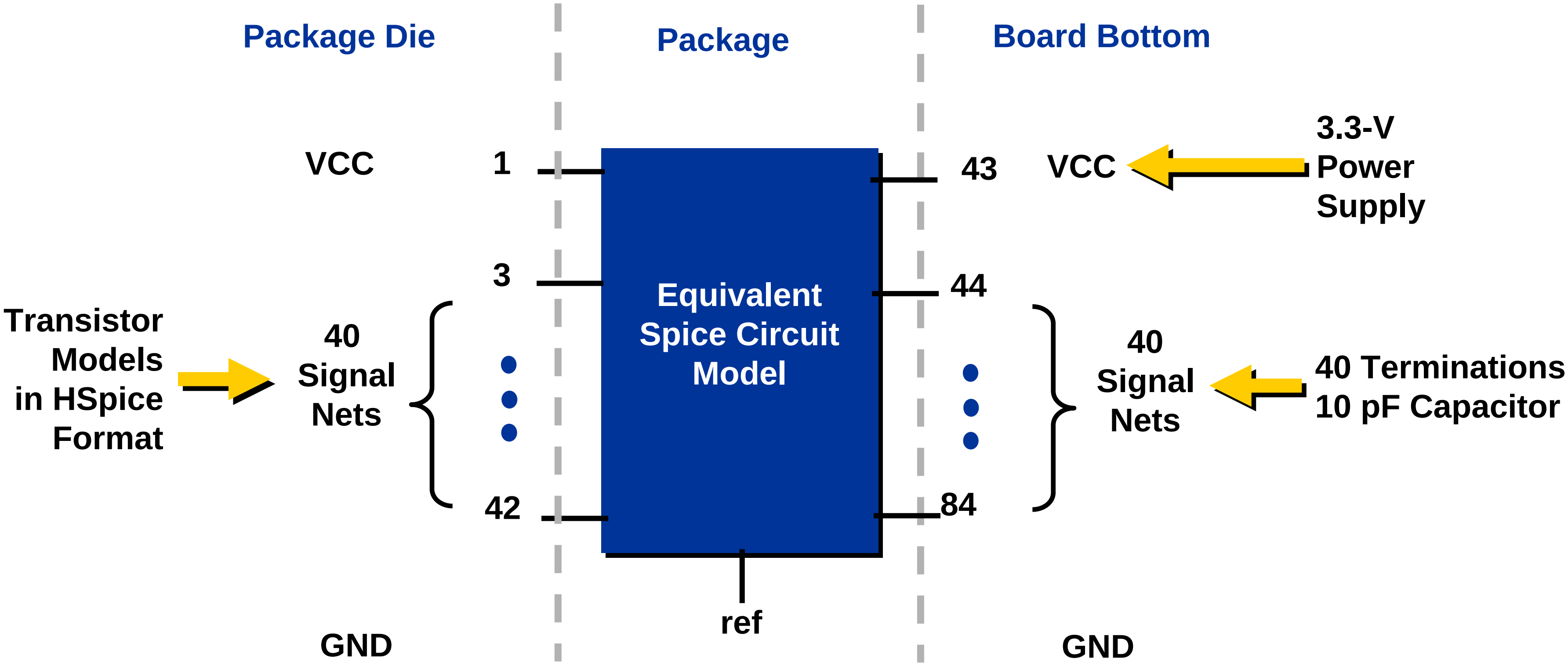
Simulation Flow Using HSpice



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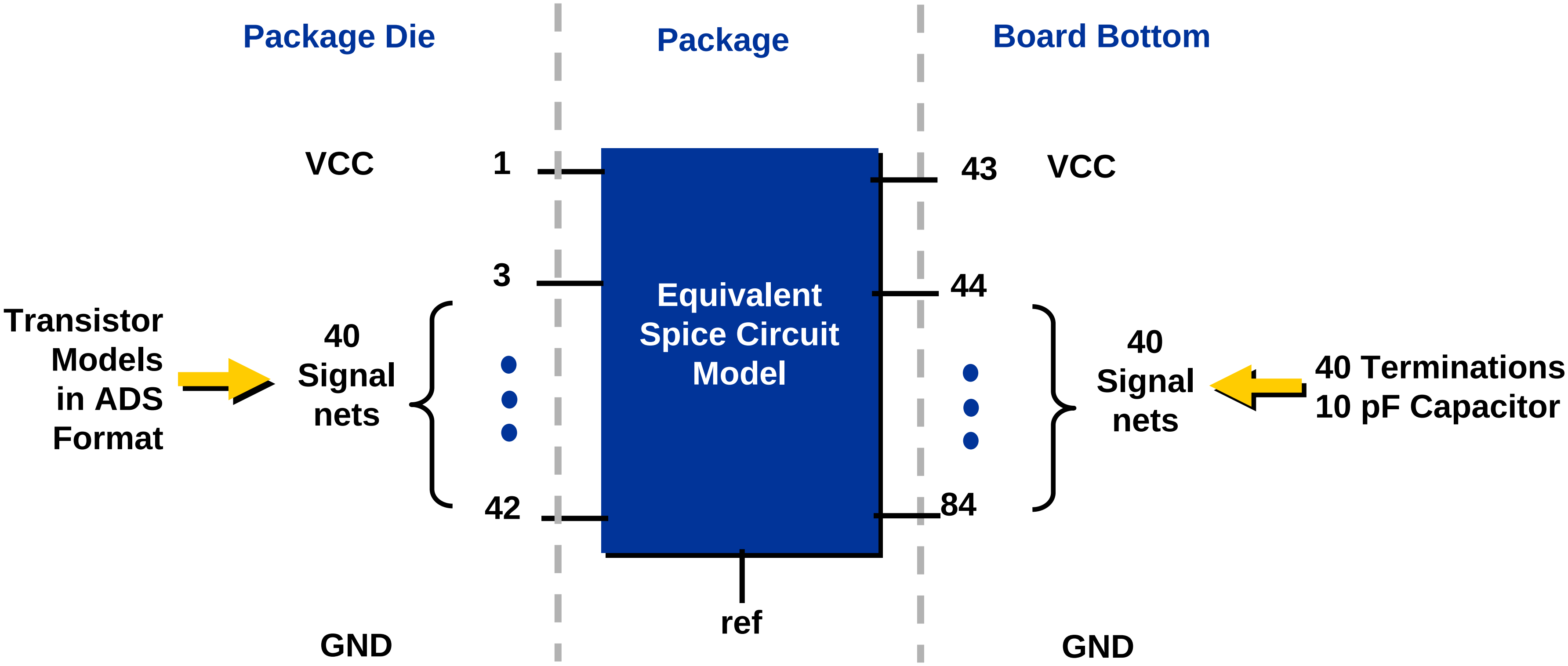
Simulation Flow Using ADS (Optional)



Package Die

Package

Board Bottom

VCC

1

43

VCC

3

44

Transistor Models in ADS Format

40 Signal nets

Equivalent Spice Circuit Model

40 Signal nets

40 Terminations 10 pF Capacitor

42

84

ref

GND

GND

The Simulation Flow Will Be Updated after ADS Model Becomes Available.

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SSO Modeling Matrix Chart

Task	Number of I/O Pins				Current Strength				I/O Location			
	1	10	40	Max	Min	Typ	Max		VIO	HIO	SSTL2	LVTTL3.3V
SSN Measurement	●	●	●	●	●	●	●	●	●	●	P1	P1
SSO Timing Push Out	●		●	●	●		●	●	●		P1	P1
SSO vol/voh Violation	●		●	●	●		●	●	●		P1	P1
Vref	●		●	●	●		●	●	●	●	P1	
Programmable Power/GND Ppins			● ●			● ●		● ●	● ●	●	P1	P1 ●
Indivudual vs. Adjacent Banks			●			●		●	●	●		●
Distribution of I/O Pins			●			●		●	●	●	●	●
SSN Measurement												

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HSpice Models

- Encrypted HSpice Models For All I/O Pins
- Models Are Accompanied by Correlation Report & User Guide
- Package Models:
  - Distributed Models
  - Lumped Models

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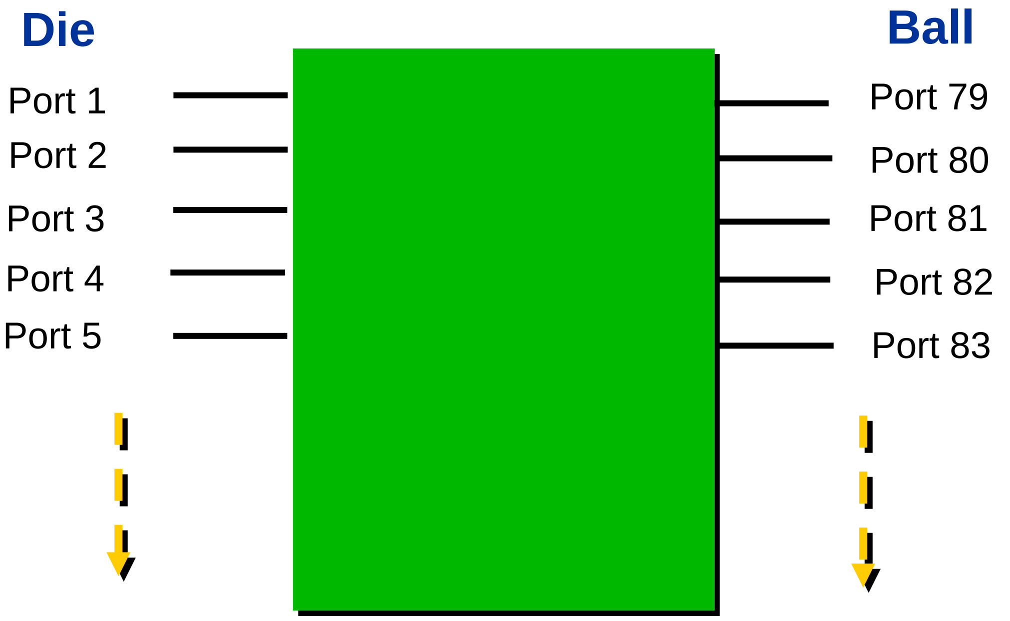
SSO Kit

- S-Parameter Models Using Sigrity Power SI
- HSpice Models Derived From S-Parameter Models Using Broadband Spice

HSpice Sub-Circuit Call



Die

Port 1
Port 2
Port 3
Port 4
Port 5

Ball

Port 79
Port 80
Port 81
Port 82
Port 83

```
.subckt ss 1  2  3  4  5  6  7  8  9  10  11  12  13
              14  15  16
 +17  18  19  20  21  22  23  24  25  26  27  28
              29  30  31
 +32  33  34  35  36  37  38  39  40  41  42  43
            44  45  46  47
 +48  49  50  51  52  53  54  55  56  57  58  59
            60  61  62  63
 +64  65  66  67  68  69  70  71  72  73  74  75
            76  77  78  79
 +80  81  82  83  84  85  86  87  88  89  90  91
            92  93  94  95
 +96  97  98  99  100  101  102  103  104  105
          106  107  108  109
 +110  111  112  113  114  115  116  117  118
          119  120  121  122
 +123  124  125  126  127  128  129  130  131
          132  133  134  135
 +136  137  138  139  140  141  142  143  144
          145  146  147  148
 +149  150  151  152  153  154  155  156  ref
```

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Other Modeling Collateral

- HSpice Kit
  - Library Of Transmission Line Models, Via Models & Connector Models, Correlated with Lab Measurements

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Design Services Partner Program

ACAP®

Altera Consultants Alliance Program

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ALTERA®

Premise Behind Partner Program

- Altera Partners with Best-in-Class Engineering Firms to Provide Altera–Based Design Services for Mutual Customers
- Altera's Motivation
  - Expand Technical Resource Base
- Partner's Motivation
  - Worldwide Co-Marketing
  - Access to a Large Sales Channel
  - Access to Worldwide Customers

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Benefits to Customers

Single Contact Point

Focus on Specification

Reduced Time-to-Market

Access to Expertise Improves System Performance

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Characteristics of Partners

- Altera Partners with Only the Best & Partners Are Limited in Number
- Characteristics of Partners:
  - Aligned Along Vertical Market Segments
  - Expertise at Architectural Level (Not at Socket Level)
  - Identified as Being Leaders in Their Segment
  - Significant Size & Financially Secure for Credibility
  - Already Known & Trusted by Customers
  - Worldwide Position
  - No Universal Pricing Method, Pricing Negotiated between Customer & Consultant
  - Supports Customer Directly

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Additional Altera Resources

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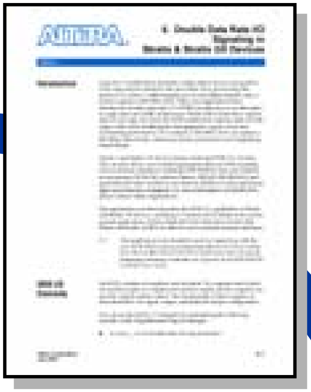
Memory Interface Standard Deliverables

Handbook

- Device Description
- Electrical Parameters
- Device Timing



Application Note

- Interface Description
- Timing Analysis
- Electrical Analysis

MegaCore®

- User Interface
- Open Source Datapath
- System Timing Analysis
- Reference Design
- Constraints
- User Guide

QUARTUS® II

- Compilation Support
- Timing Models

Demonstration Board

- Demonstration Project
- Board Layout Guidelines
- Schematics/Gerbers
- Signal Integrity Analysis
- Documentation

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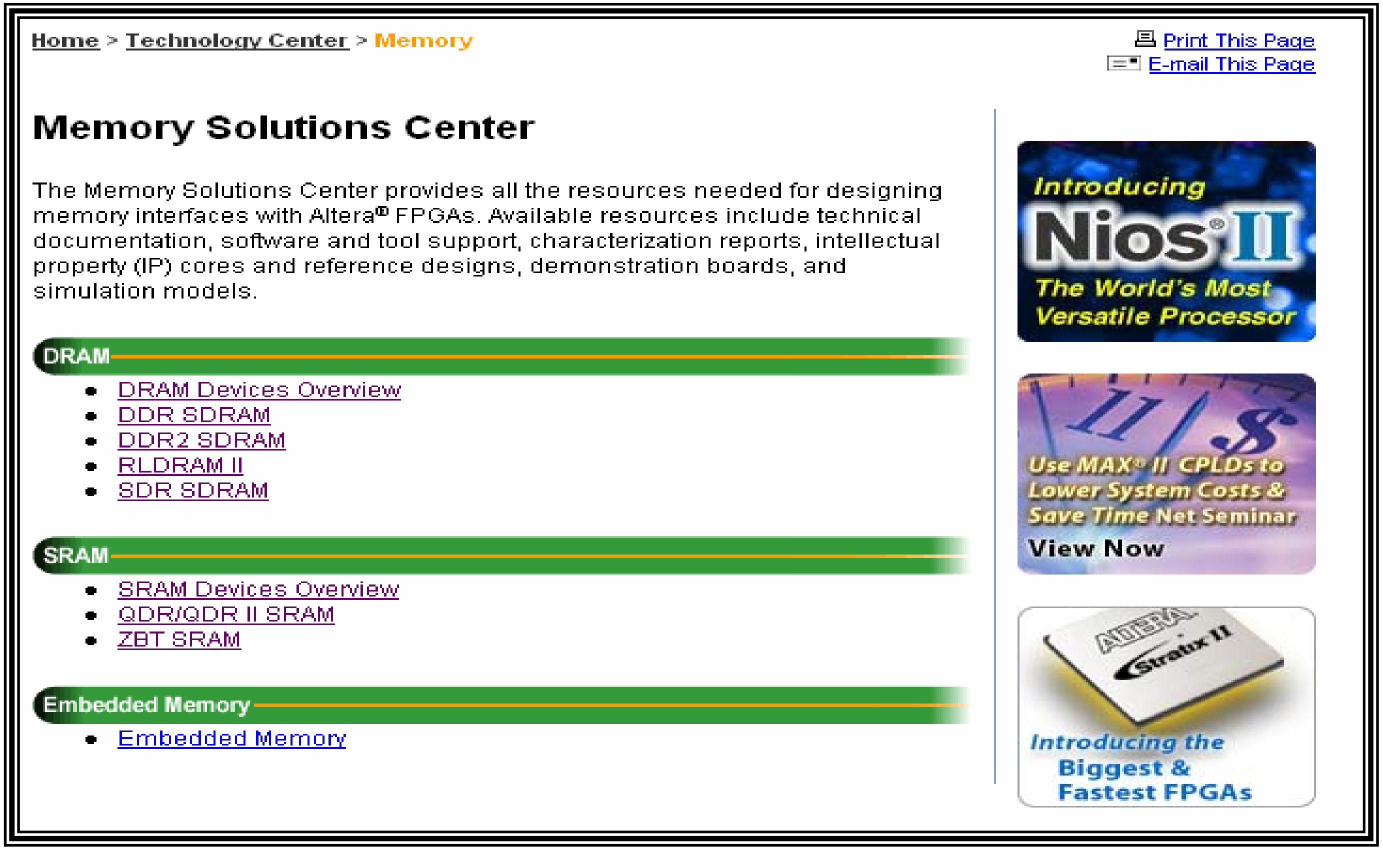
Memory Solutions Center



Home > Technology Center > Memory

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Memory Solutions Center

The Memory Solutions Center provides all the resources needed for designing memory interfaces with Altera® FPGAs. Available resources include technical documentation, software and tool support, characterization reports, intellectual property (IP) cores and reference designs, demonstration boards, and simulation models.

DRAM

- DRAM Devices Overview
- DDR SDRAM
- DDR2 SDRAM
- RLDRAM II
- SDR SDRAM

SRAM

- SRAM Devices Overview
- QDR/QDR II SRAM
- ZBT SRAM

Embedded Memory

- Embedded Memory

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Use MAX® II CPLDs to Lower System Costs & Save Time Net Seminar

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Web Site to Provide Easy Access to Memory Support Information

Benefits of Altera's Memory Solution

- Simplifies Memory Interface Design Process
  - Dedicated Circuitry in Silicon, Software & Tool Support
- Ensures First-Time Design Success
  - Hardware Reference Platform for Design Verification
- Reduces Design Cycles
  - IP Core Support, Detailed Documentation

Complete System-Level Solution

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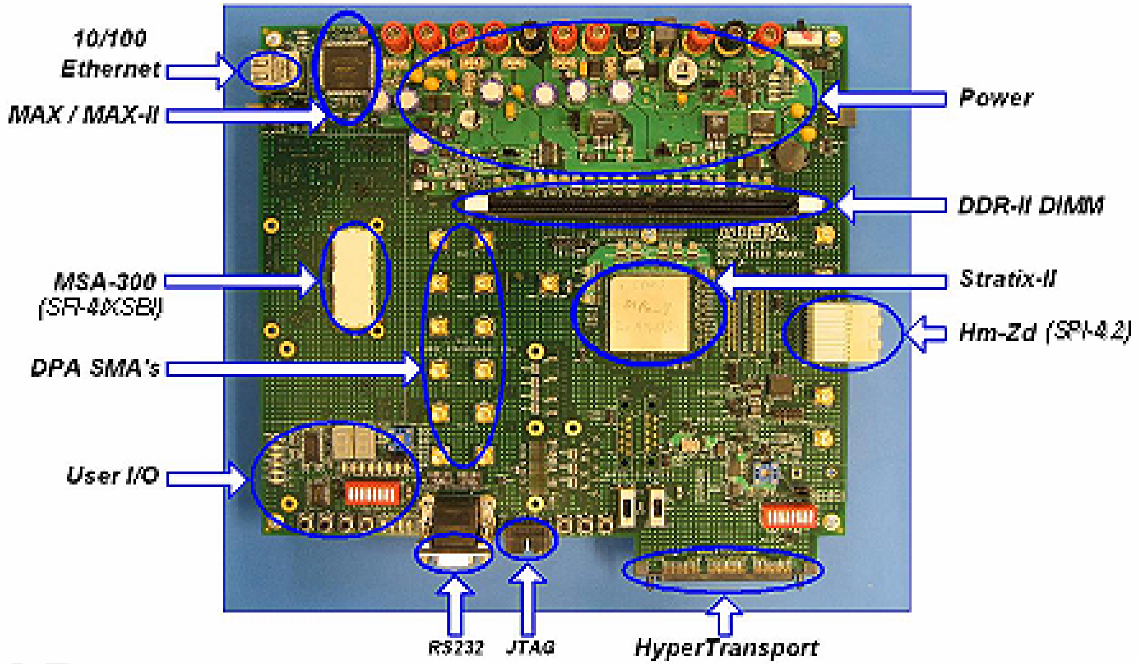
Stratix II High-Speed Development Board

- Designed for the Development of Applications that Incorporate High-Performance Interfaces
  - Stratix II EP2S60F1020C3 FPGA
  - External Connectors for a Broad Array of Applications



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More Information

- Simultaneous Switching I/O Noise Guidelines for Stratix & Stratix GX FPGAs
- Minimizing Ground Bounce & Vcc Sag
  http://www.altera.com/literature/wp/wp_grndbnce.pdf
- Basics of Signal Integrity White Paper
  http://www.altera.com/literature/wp/wp_sgnlntgry.pdf
- High-Speed Board Layout Guidelines
  http://www.altera.com/literature/an/an224.pdf
- Guidelines for Designing High-Speed FPGA PCBs
  http://www.altera.com/literature/an/an315.pdf

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More Information (cont.)

- Visit Altera’s Memory Solution Center at: www.altera.com/memory

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Thank You !

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