

nbit_adder: adderx

GENERIC MAP (x => 8)

PORT MAP (AddSub: R, G, H, M, ...)

multiplexer: mux2to3

GENERIC MAP (x => 1)

PORT MAP (A: R, Z: S, ...)

Implementing Video and Image Processing Designs Using FPGAs

Click to add subtitle

Agenda

- Key trends in video and image processing
- Video and Image Processing Suite
- Model-based design for video processing
- Tutorial

Video and Imaging With FPGAs



Broadcast Infrastructure



HDTV Display



Medical Imaging



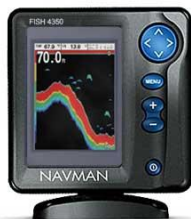
HDTV Videoconferencing



Security DVR



HD Security Camera



Consumer/Auto Display



Document Imaging



Military Imaging

Key Trends in Video and Imaging

■ Higher resolutions

- 3,000 x 3,000 (and higher): medical imaging, military, machine vision
- 4,096 x 1,714: digital cinema
- 1,920 x 1,080: HDTV, broadcast
- 1,280 x 720: video surveillance, videoconferencing

■ Advanced video compression

- H.264, JPEG2000, VC1

Current Solutions Do Not Deliver

**Video/
Imaging
ASSPs**

*Not optimized for target applications
Risk of obsolescence*

DSP

Cannot achieve high definition in single device

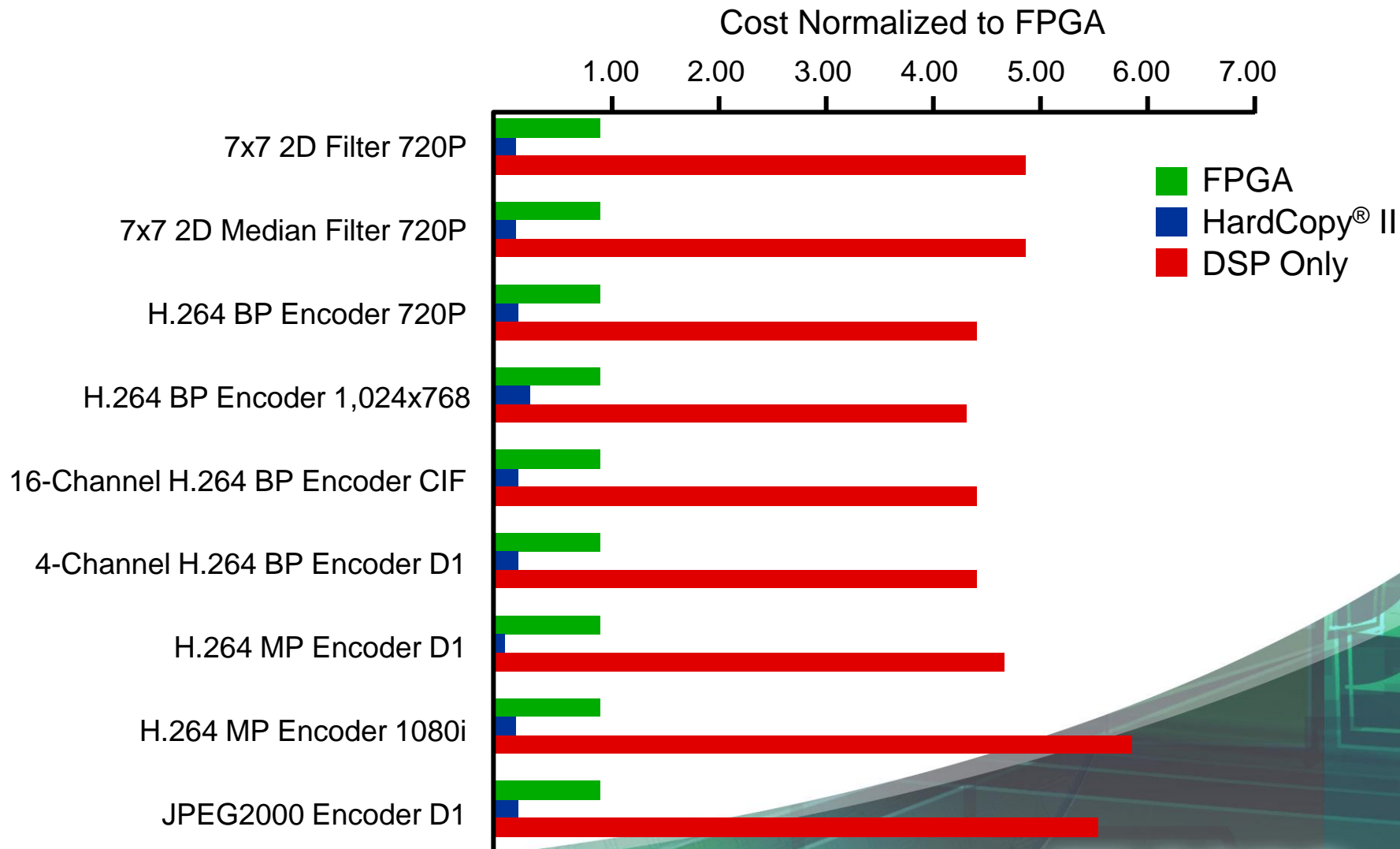
ASIC

*High development cost
Cannot keep up with fast-evolving applications*

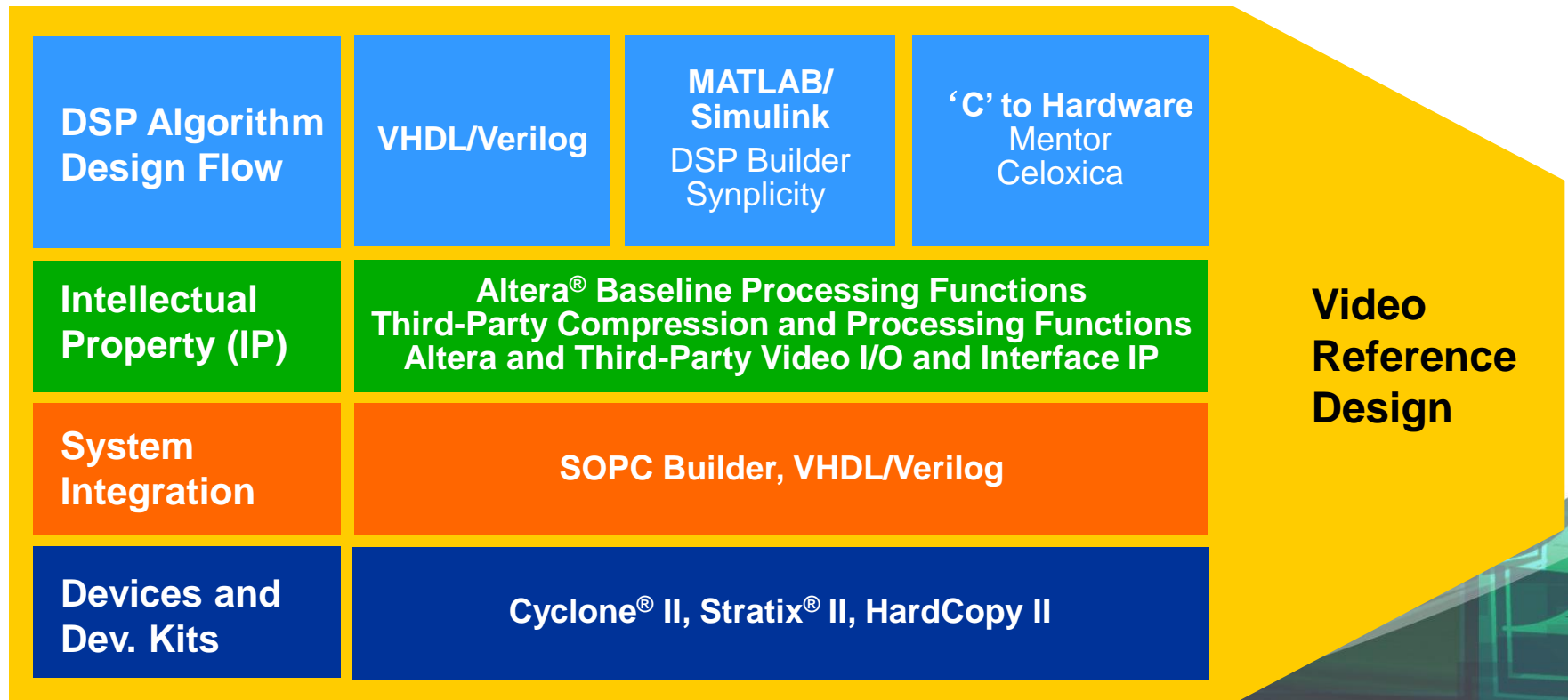
Altera's FPGA Solution

- ✓ High performance in a single device
- ✓ Fast time-to-market
- ✓ Easy to upgrade
- ✓ Low development cost
- ✓ Obsolescence proof
- ✓ Lower unit costs at high volumes

Video Benchmarks



Altera Video and Image Processing Solutions Overview



IP Examples – Video

I/O and System

- PCI Express
- Serial Rapid I/O
- EMIF Interface
- ASI
- SDI
- ATA HDD (Nuvation)
- MPEG2 Transport
- 10/100/1000 Ethernet
- DDR/DDR2 Controller

Video and Image
Processing Suite

Pre-/Post-Processing

- Scaler
- Deinterlacer
- 2D FIR Filter
- 2D Median Filter
- Color Space Converter
- Chroma Resampler
- Gamma Corrector
- Alpha Blender
- Highest Quality HDTV Upconversion (Let It Wave)
- AES/DES/Sha-1 Encryption (CAST)

Compression

- H.264 MP, HP (ATEME)
- H.264 BP (4i2i, CAST, W&W)
- H.264 CABAC/CAVLC (ATEME)
- H.264 Loop Filter (ATEME)
- MPEG4 SP/ASP (CAST, Barco)
- JPEG (CAST, Barco)
- JPEG2000 (CAST, Barco, Broadmotion)

HDTV Upconversion – Let It Wave

- Breakthrough super-resolution Bandlet technology for HDTV upconversion
- Broadcasting equipment
 - Upconverter implemented on cost-effective Altera FPGA
 - Main features
 - Standard definition (SD) to high definition (HD) up to 1080P
 - 2-frame delay
 - Color conversion
 - Per pixel automatic film mode and cadence detection
 - Aspect ratio conversion
 - Additional features
 - Cross conversion 720P to 1080I
 - HD to SD down conversion
 - Video enhancement
 - Board reference design available



Video and Image Processing Suite

Altera Video and Image Processing Suite

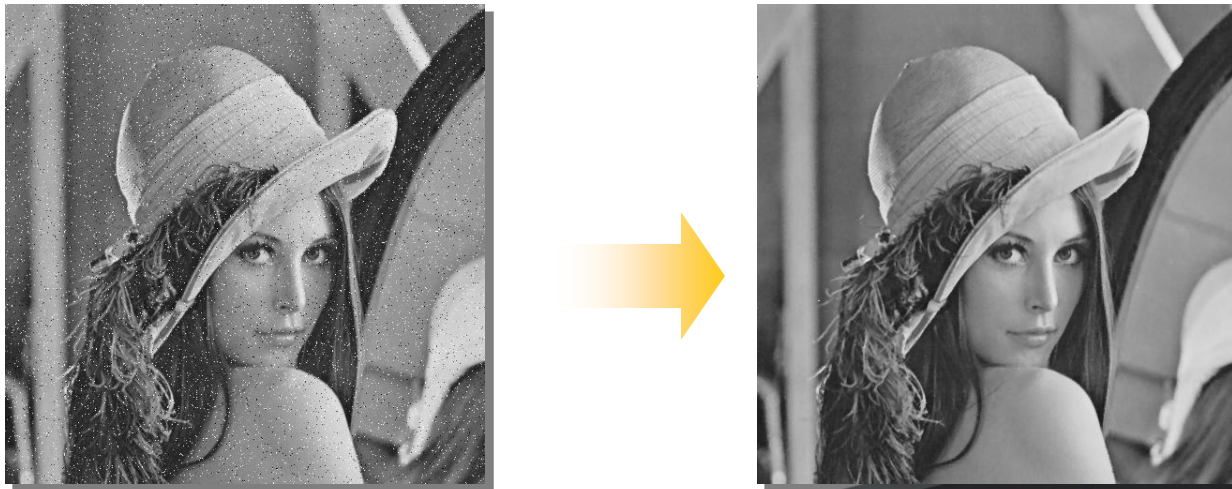
- Baseline set of IP with standard interfaces and protocols that allow users to easily add their own proprietary algorithms
- Optimized for Altera FPGAs
- Works with any design flow
 - RTL, model-based design, C-based design

Video and Image Processing Suite

| Core | Function |
|-----------------------|---|
| Deinterlacer | Converts interlaced video formats to progressive video format |
| Color space converter | Converts image data between a variety of different color spaces |
| Scaler | Resizes and clips image frames |
| Gamma corrector | Performs gamma correction on a color space |
| Alpha blending mixer | Mixes and blends multiple image streams, including picture-in-picture (PIP) |
| Chroma resampler | Changes the sampling rate of the chroma data for image frames |
| 2D filter | Implements a 3x3, 5x5, or 7x7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images |
| 2D median filter | Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values |
| Line buffer compiler | Efficiently maps image line buffers to Altera on-chip memory |

2D Filtering

- 2D FIR filter and 2D median filter
 - 3x3, 5x5 or 7x7 filter sizes
- Useful for noise reduction and smoothing filters
- Supports symmetric optimization

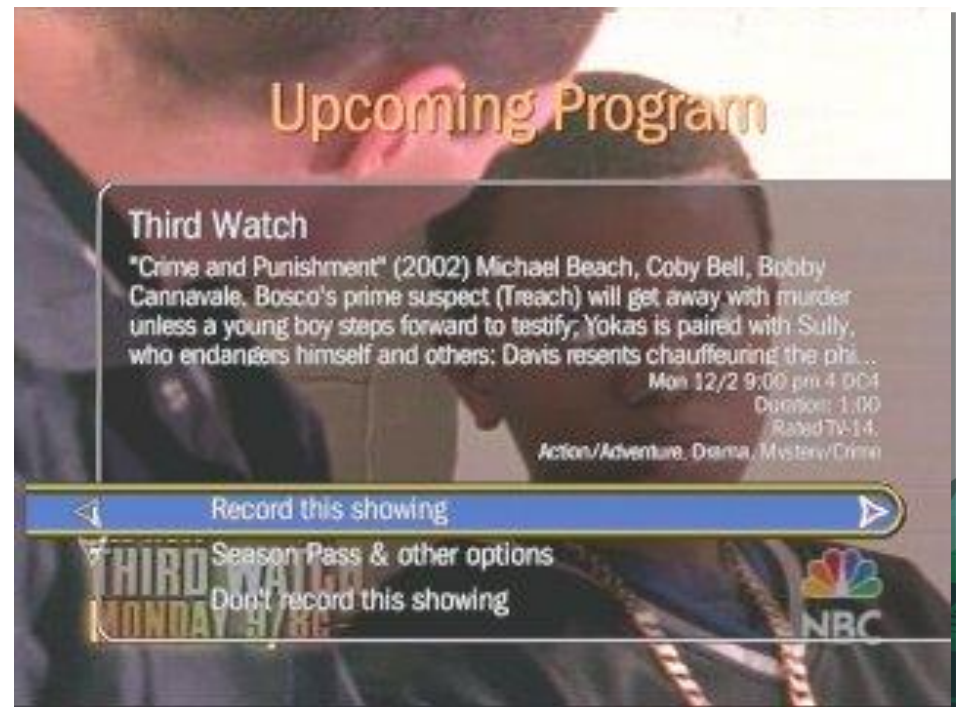


Color Format Conversion

- Supplied as three separate cores
 - Color space converter
 - Chroma resampler
 - Gamma corrector
- Supports
 - RGB (computer and studio formats)
 - YIQ/YUV (NTSC, PAL, SECAM)
 - YCbCr (4:4:4, 4:2:2, 4:2:0)

Image Blending and Picture-in-Picture Mixing

- Multi-layer mixing (2 to 8 layers)
- Per-pixel alpha blending
- Run-time control of picture-in-picture location



Scaling



D1/SDTV: 720 x 480



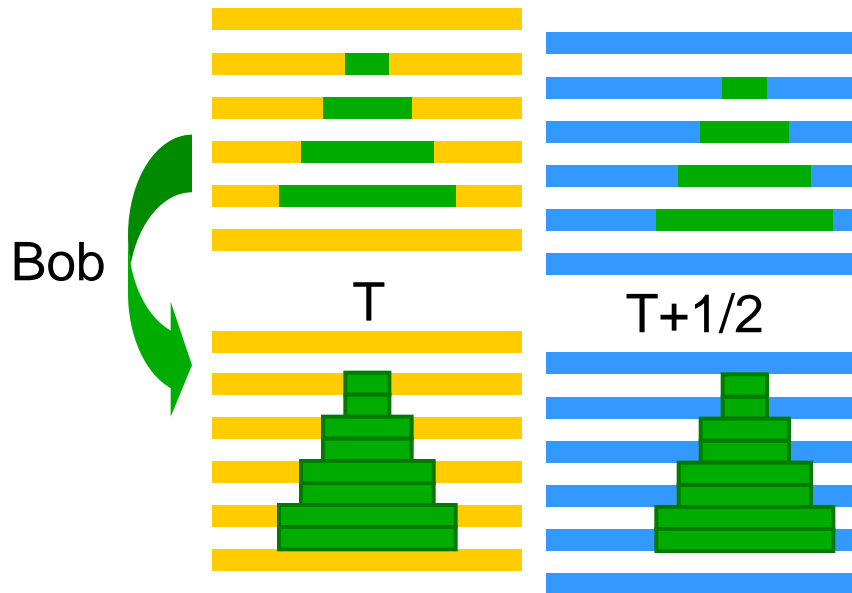
HDTV 1080p: 1920 x 1080

- Supports standard-resolution conversions
- Nearest neighbor or bilinear filtering
- Clipping

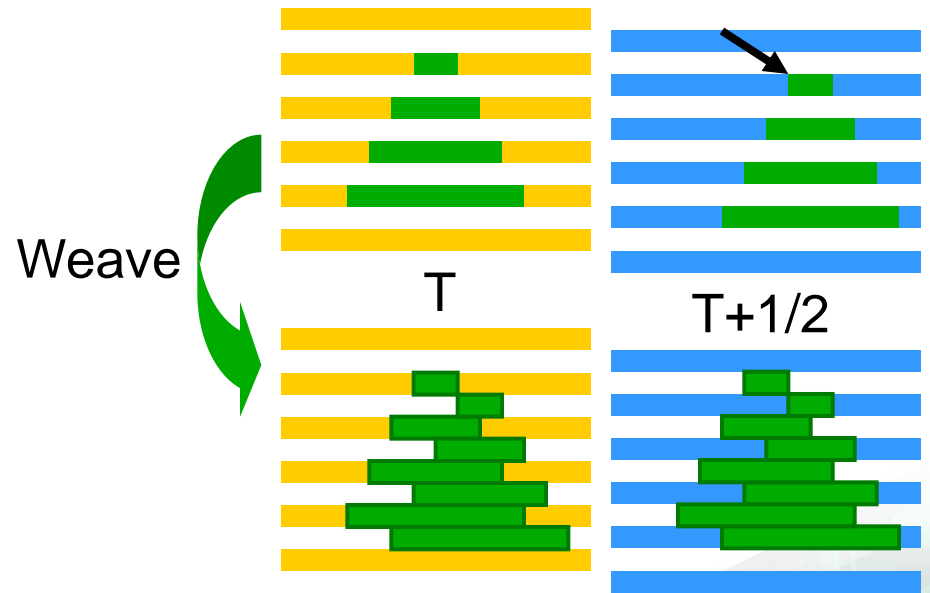
Deinterlacing

- “Bob” and “Weave” supported

“Bob” – 1 Field



“Weave” – 2 Fields



Line Buffer Compiler

- Provides line buffers, making efficient use of FPGA internal memories
- Optimized for typical SD and HD resolutions
- Any number of bits per color plane
 - Choose line length, width, number of lines

Model-Based Design for Video Processing

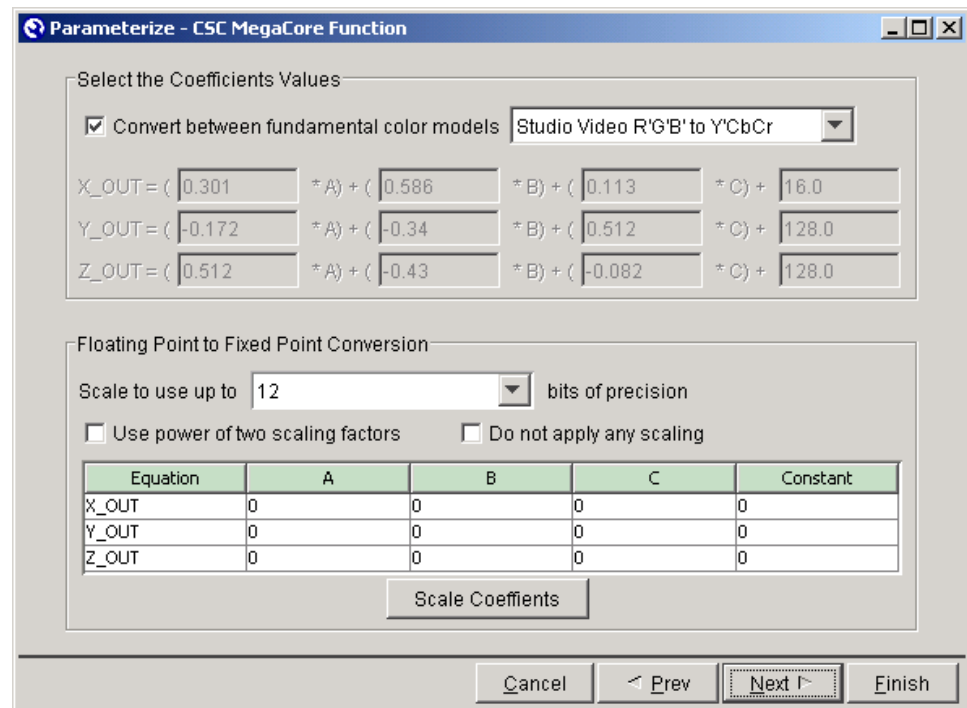
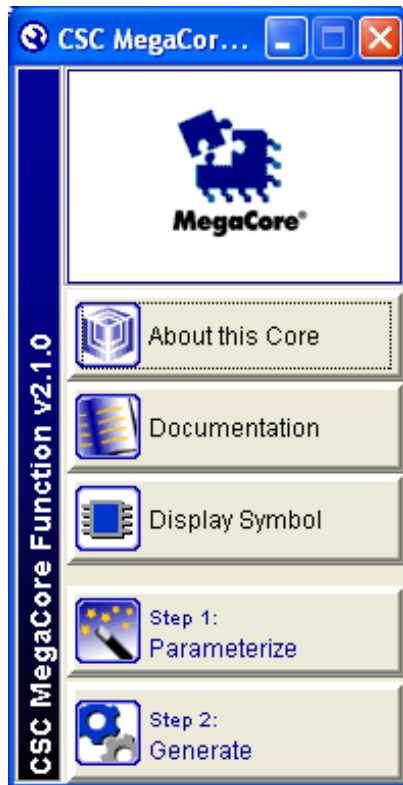
Design Flow Starting with Model-Based Design

- DSP Builder for data path
 - Design
 - Simulation
 - Creation of an SOPC Builder component
- SOPC Builder for system integration
 - External RAM controllers
 - Sources and sinks
 - Processor integration
 - Nios[®] II or external processor
- Compile in Quartus[®] II software

Configure Blocks with GUI

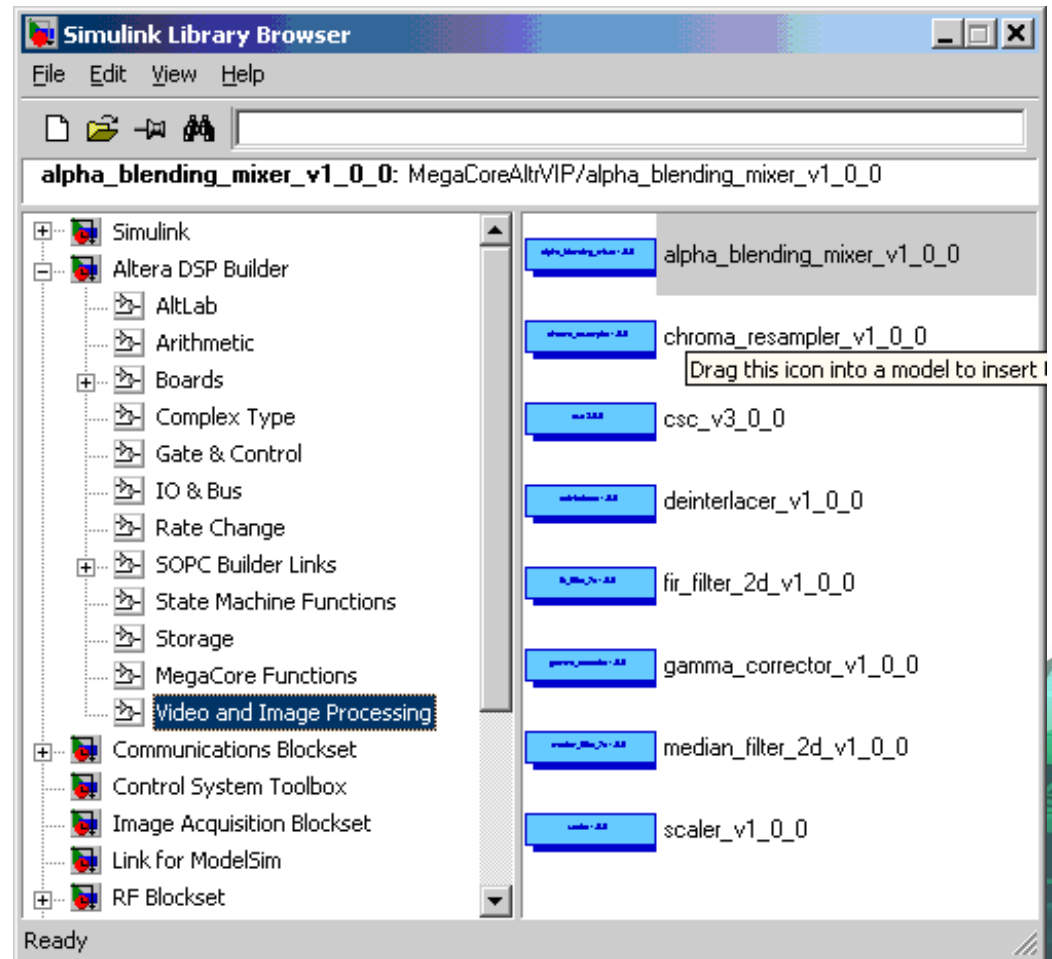
■ IP Toolbench

- Launched from Quartus II software or directly in DSP Builder



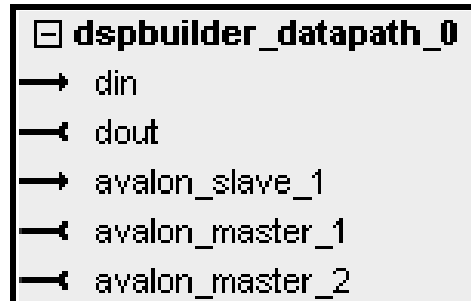
DSP Builder Video Library

- Alpha blending mixer
- Chroma resampler
- Color space converter
- Gamma corrector
- Deinterlacer
- 2D FIR filter
- 2D median filter
- Scaler



SOPC Builder System Integration

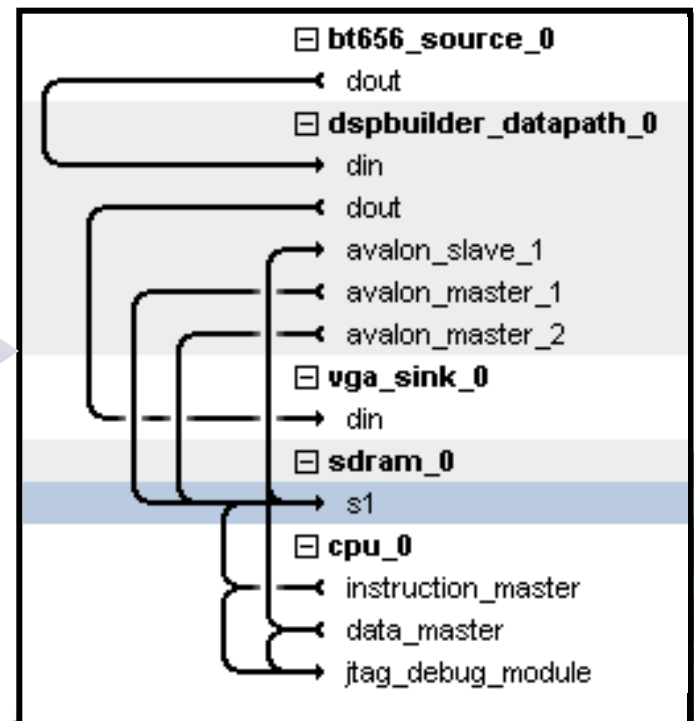
DSP Builder Data Path



Add

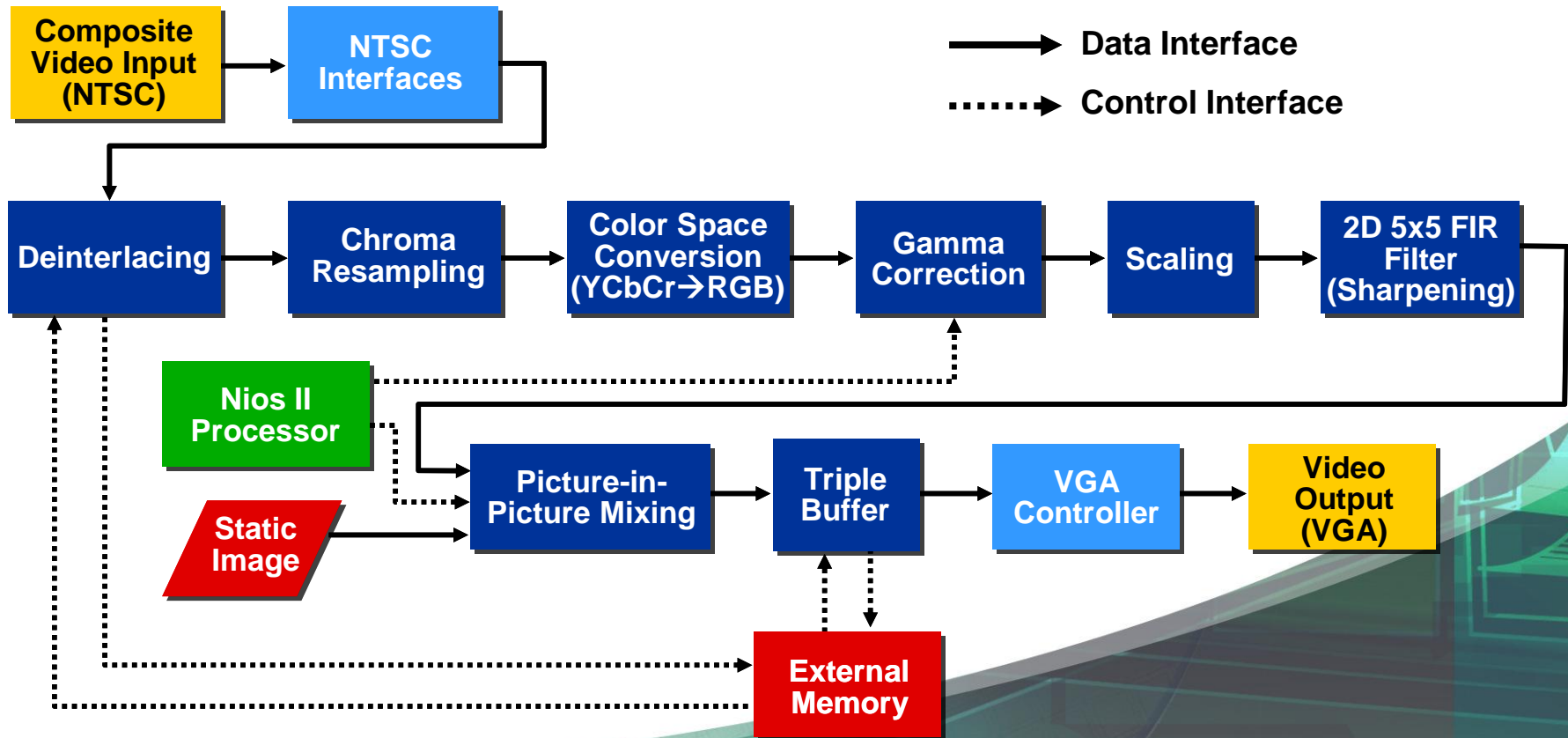
- Sources
- Sinks
- Arbitrated DDR, SDR
- Control

SOPC Builder System



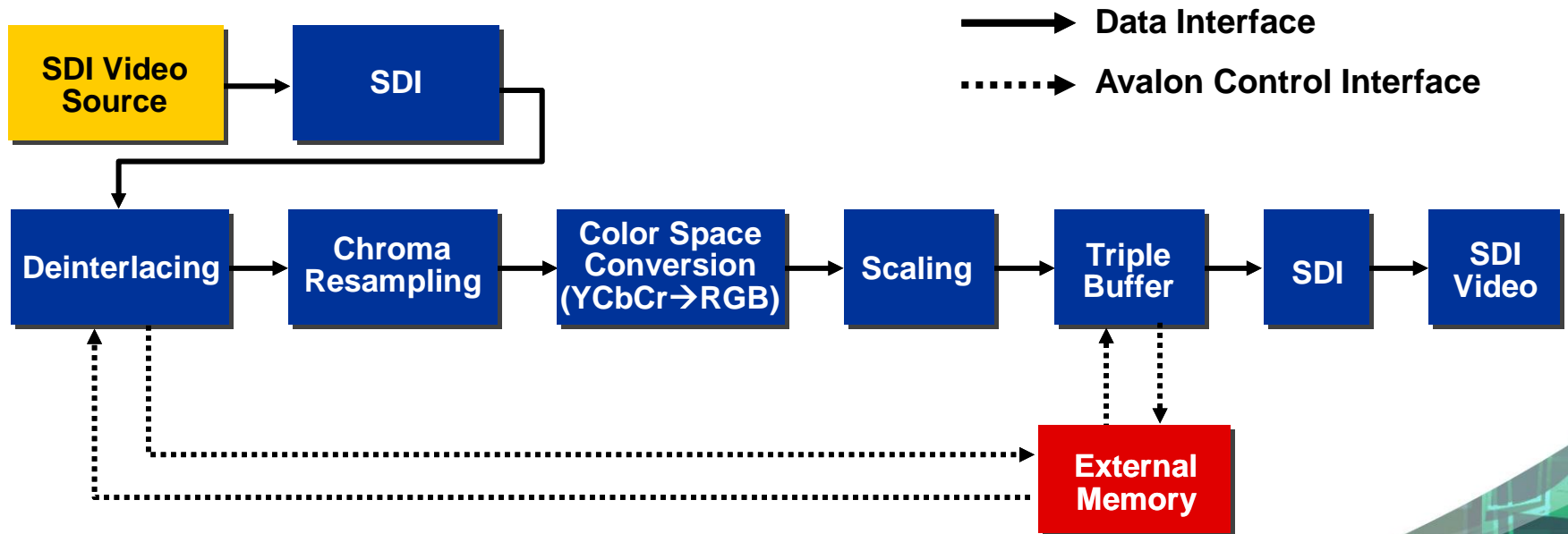
Example 1: Single Input Video Channel

- Composite video input
- VGA output

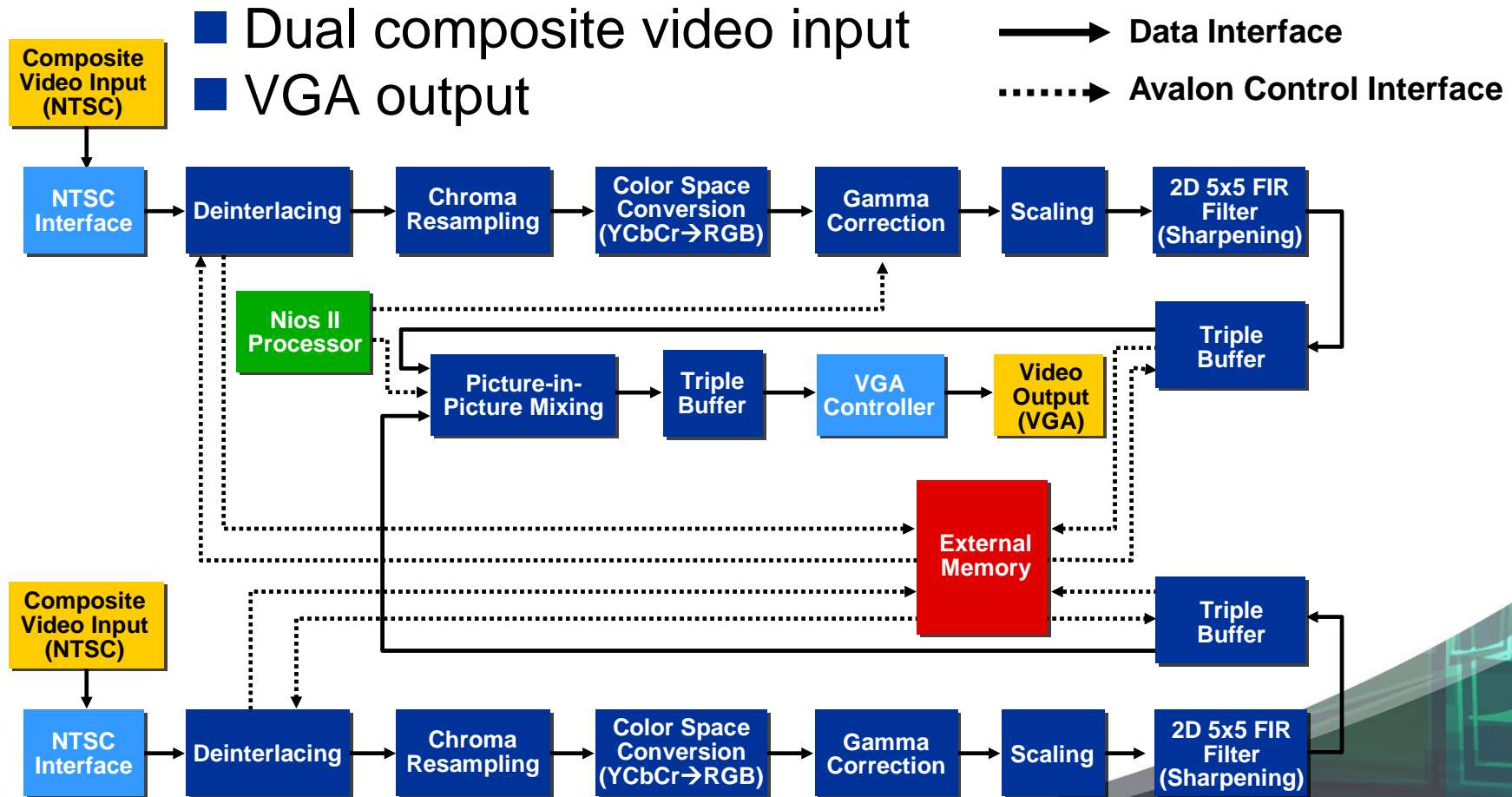


Example 2: Single Input Video Channel

■ SDI video input/output



Example 3: Multiple Video Channel Input

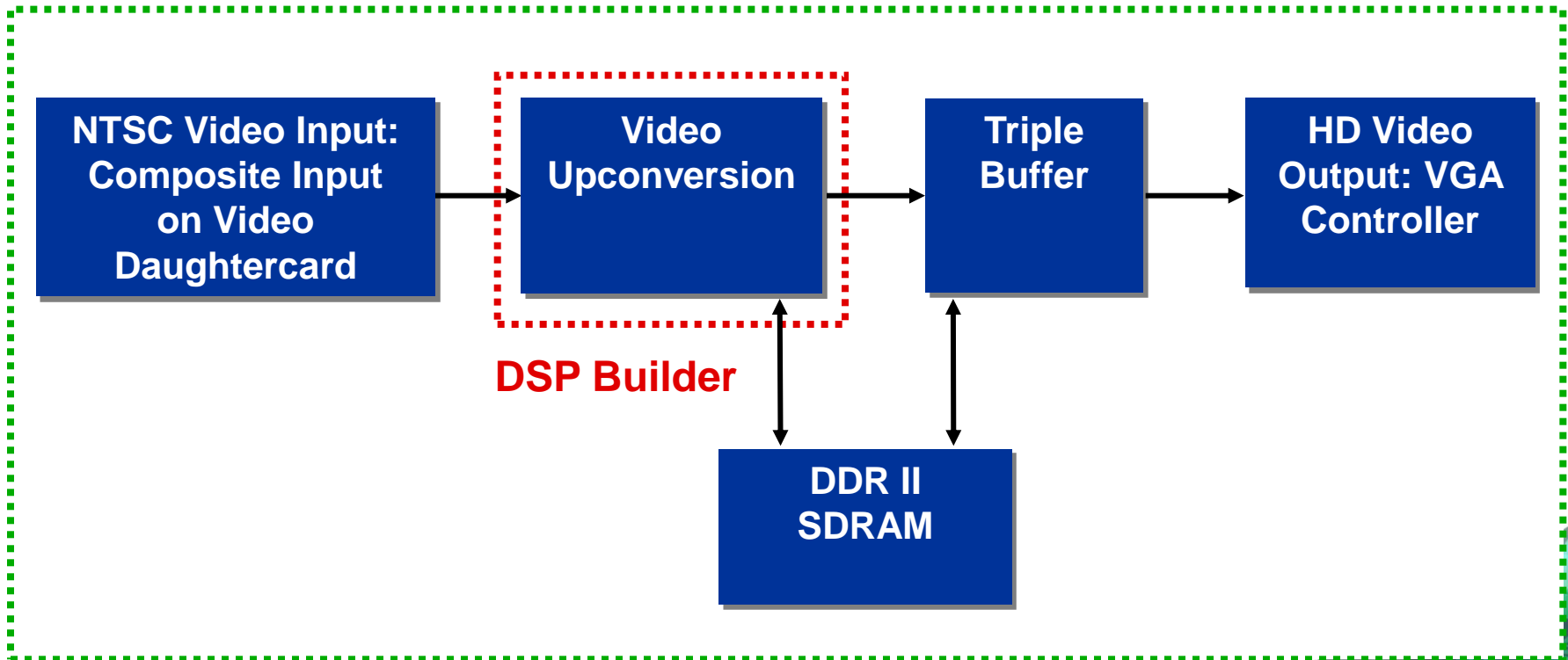


Video and Image Processing (VIP) Example Design

Example of a Video System

- System block diagram
- DSP Builder
 - Implementation
 - Simulation
 - Conversion to HDL
- SOPC Builder integration
- Program hardware platform

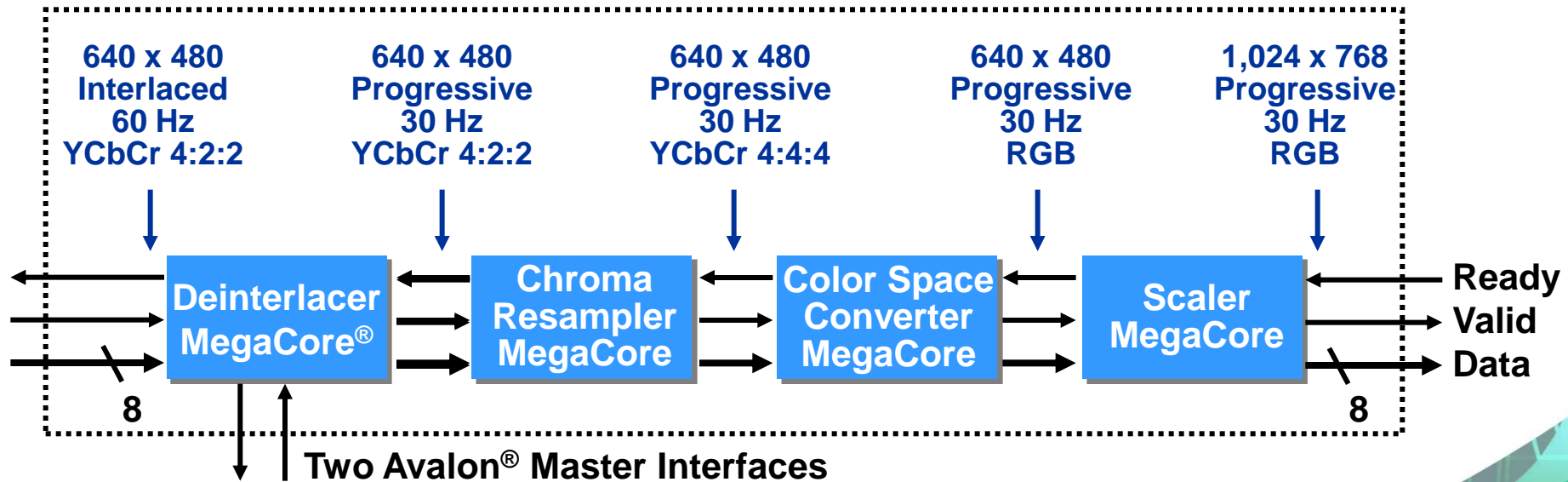
VIP Upconversion System



SOPC Builder

Video Upconversion Data Path

- Entire data path is assembled in DSP Builder



DSP Builder Implementation - Deinterlacer

Parameterize Deinterlacer

Parameterize - Deinterlacer MegaCore Function

Image Data Format

Image resolution : 640x480 Pixels

Bits per pixel per color plane : 8 Bits

Number of color planes in sequence : 2 Planes

Behavior

Deinterlacing method : Weave

Base address of frame buffers : 0x11000000

Cancel Finish

Up to 1920 x 1080
Supported

Bob and Weave
Supported

DSP Builder Implementation: External Memory for Deinterlacer

Function Block Parameters: External RAM

S-Function (mask) (link)

This is a simulation model of an external RAM block. It can be used to store and retrieve data from a range of addresses. It is designed specifically to work with the DSP Builder Video and Image Processing blocks, but may be used for other purposes.

As it is a simulation only block, it will not generate HDL when SignalCompiler is run.

Parameters

=====

Data width - the number of bits used for the data. (For 8,16 or 32 bits, use a Simulink double type. For 64 or 128 bit data, use a Simulink fixed-point type. No other values are supported)

Address width - number of bits used for address (between 1 and 32)

Wait states per write - choose a fixed number of wait states for each write transfer between 0 and 10)

Maximum latency - set the latency for pipelined read transfer (between 1 and 255)

Size, offset - to use a range of addresses, choose an offset (start address) and size (number of addresses). The size added to the offset must be less than $2^{\text{address width}}$.

Output contents - if this is one, an extra output is added which displays the contents of the memory at every stage.

Parameters

Data Width
64

Address Width
32

Wait States Per Write
0

Maximum Latency
1

Size
40000000

Offset
16777000

Output Contents
0

OK Cancel Help Apply

Parameterize External Memory (Simulation-Only Model)

DSP Builder Implementation: Chroma Resampler

Parameterize - Chroma Resampler MegaCore Function

Image Data Format

Image resolution : 640x480 Pixels

Bits per pixel per color plane : 8 Bits

Color Plane Configuration : Three color planes in sequence

Behavior

Conversion format : 4:2:2 to 4:4:4

Horizontal interpolation : 2D Linear

Vertical interpolation : 2D Linear

Cancel Finish

DSP Builder Implementation: Color Space Converter

Parameterize - Color Space Converter MegaCore Function

General Coefficients

Image Data Format

Image resolution : 640x480 Pixels

Bits per pixel per color plane : 8 Bits

Color Plane Configuration

☒ Three color planes in sequence

☐ Three color planes in parallel

Precision

Word Length

Word length corresponds to the number of bits used by the multiplier.
Word length consists of an integer part and a fractional part.
Please refer to the Video and Image Processing Suite User Guide for details.

Word length : 18 Bits

Integer part of word length : 11 Bits

Fractional part of word length : 7 Bits

Overflow behavior : Saturate

Underflow Behavior : Saturate

Cancel < Prev Next > Finish

Parameterize - Color Space Converter MegaCore Function

General Coefficients

Compile Time Coefficients

Color model conversion : Y'CbCr: SDTV to Computer R'G'B'

Din and dout refer to the input and output channels respectively.

dout_0 = 1.164 * din_0 + 0 * din_1 + 1.596 * din_2 + -222.912

dout_1 = 1.164 * din_0 + -0.391 * din_1 + -0.813 * din_2 + 135.488

dout_2 = 1.164 * din_0 + 2.018 * din_1 + 0 * din_2 + -276.928

Cancel < Prev Next > Finish

DSP Builder Implementation: Scaler

Parameterize - Scaler MegaCore Function

Image Data Format

Input image resolution : 640x480 Pixels

Output image resolution : 1024x768 Pixels

Bits per pixel per color plane : 8 Bits

Number of color planes in sequence : 3 Planes

Behavior

Interpolation method : 2D Linear

Clipping

☐ Enable image clipping

Width : 64 Pixels X offset : 0 Pixels

Height : 64 Pixels Y offset : 0 Pixels

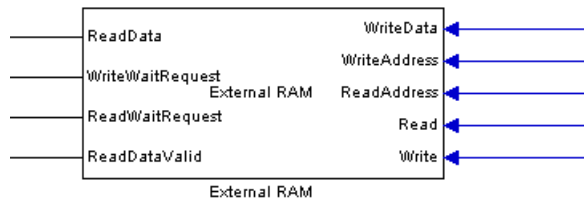
Cancel Finish

DSP Builder Implementation: Libraries Generated

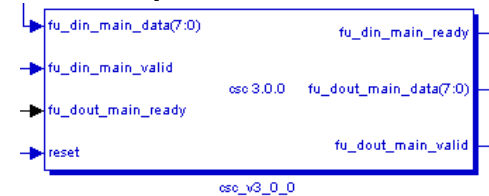
Deinterlacer



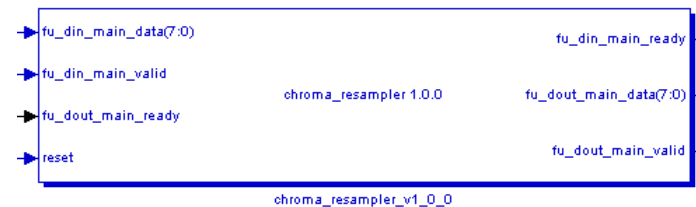
External Memory (Simulation)



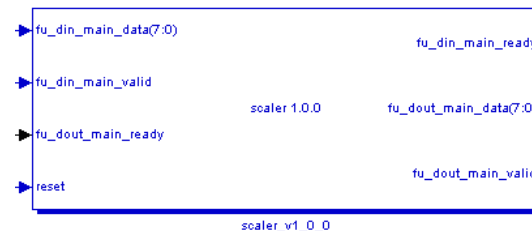
Color Space Converter



Chroma Resampler

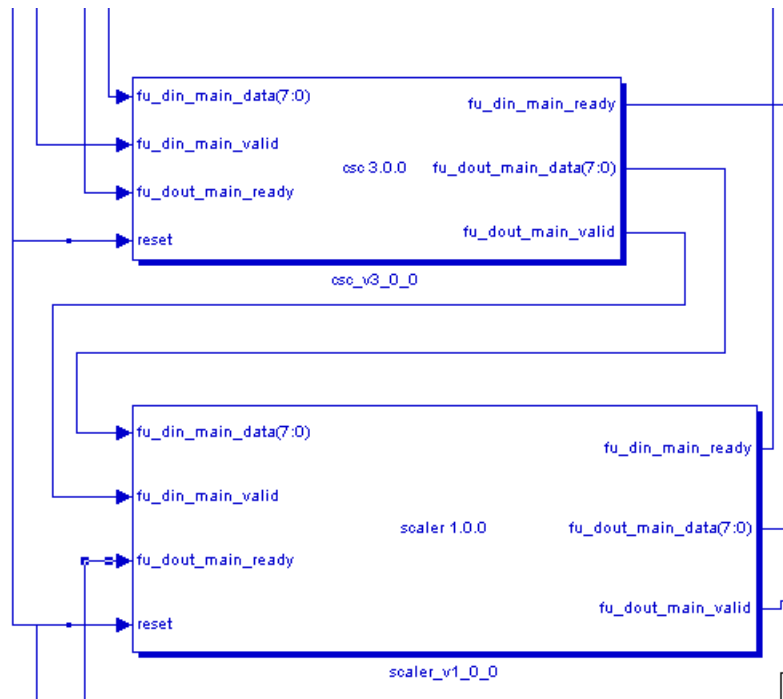


Scaler



DSP Builder Implementation: Connecting Functions

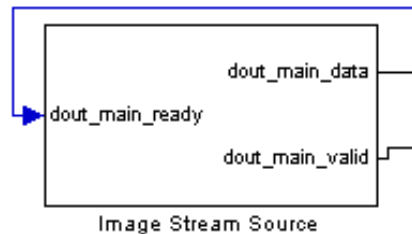
- Connecting library functions is simple due to standard interface and protocol



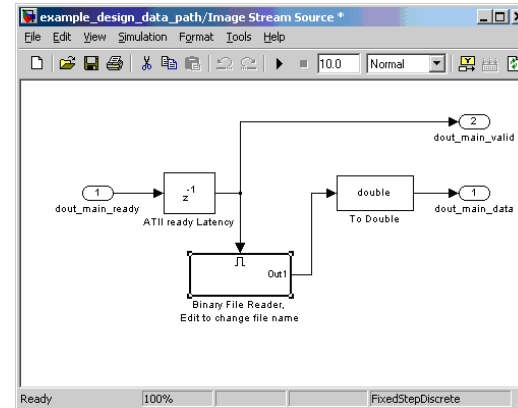
**Connections Between the
Color Space Converter and Scaler**

Simulation: Video Input

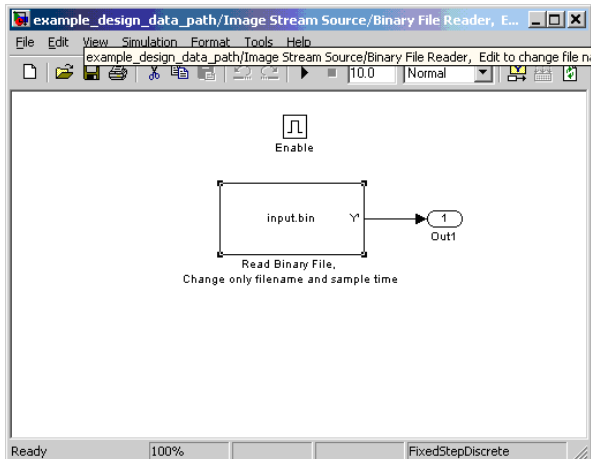
1



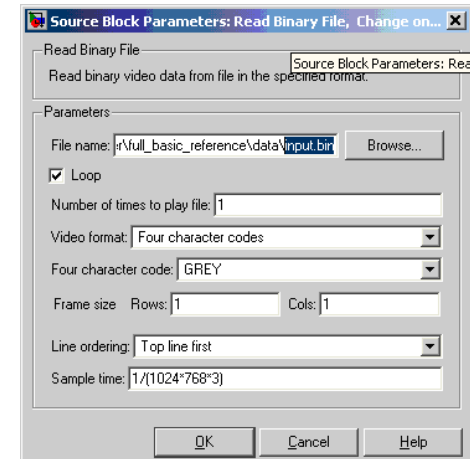
2



3

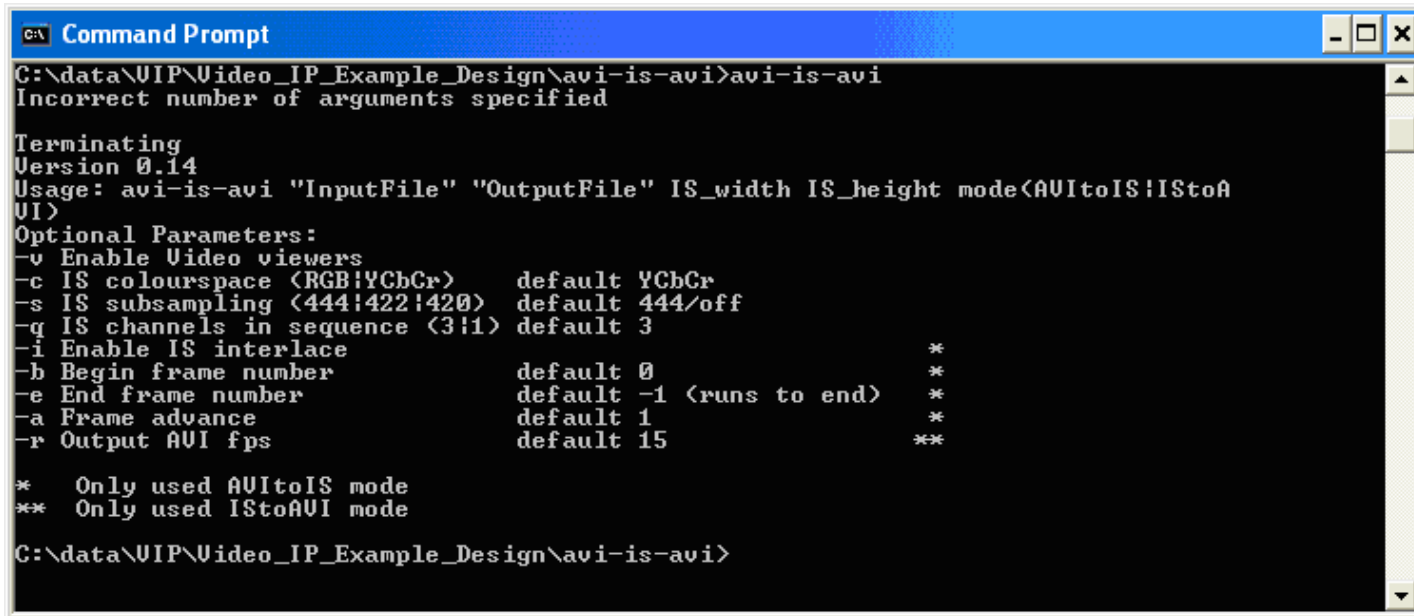


4



Simulation: Generate Video Binary File

- Command Line Utility converts AVI file to a binary file for use within DSP Builder environment
- Also converts binary output to an AVI file for convenient playback



```
C:\> Command Prompt
C:\data\VIP\Video_IP_Example_Design\avi-is-avi>avi-is-avi
Incorrect number of arguments specified

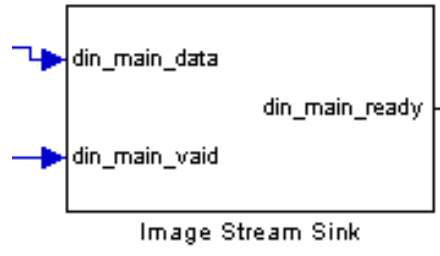
Terminating
Version 0.14
Usage: avi-is-avi "InputFile" "OutputFile" IS_width IS_height mode(AVItoIS:IStoA
VI)
Optional Parameters:
-v Enable Video viewers
-c IS colourspace (RGB|YCbCr)      default YCbCr
-s IS subsampling (444|422|420)    default 444/off
-q IS channels in sequence (3|1)  default 3
-i Enable IS interlace
-b Begin frame number             default 0
-e End frame number               default -1 (runs to end)
-a Frame advance                   default 1
-r Output AVI fps                 default 15

*   Only used AVItoIS mode
**  Only used IStoAVI mode

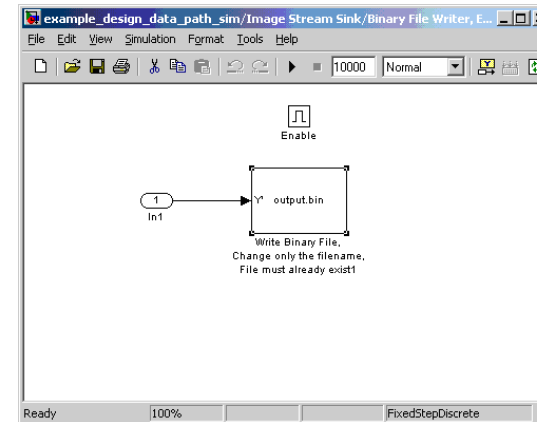
C:\data\VIP\Video_IP_Example_Design\avi-is-avi>
```


Simulation: Video Output

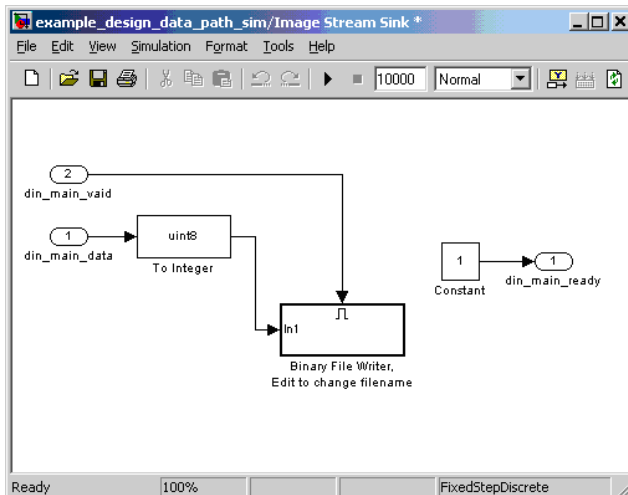
1



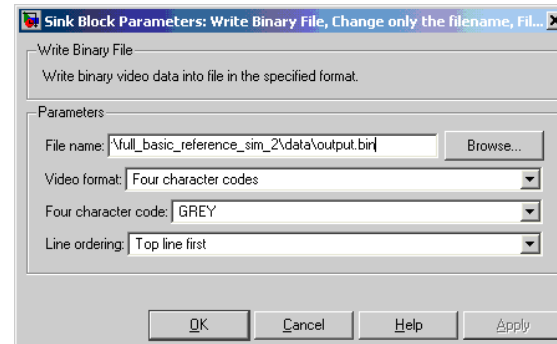
2



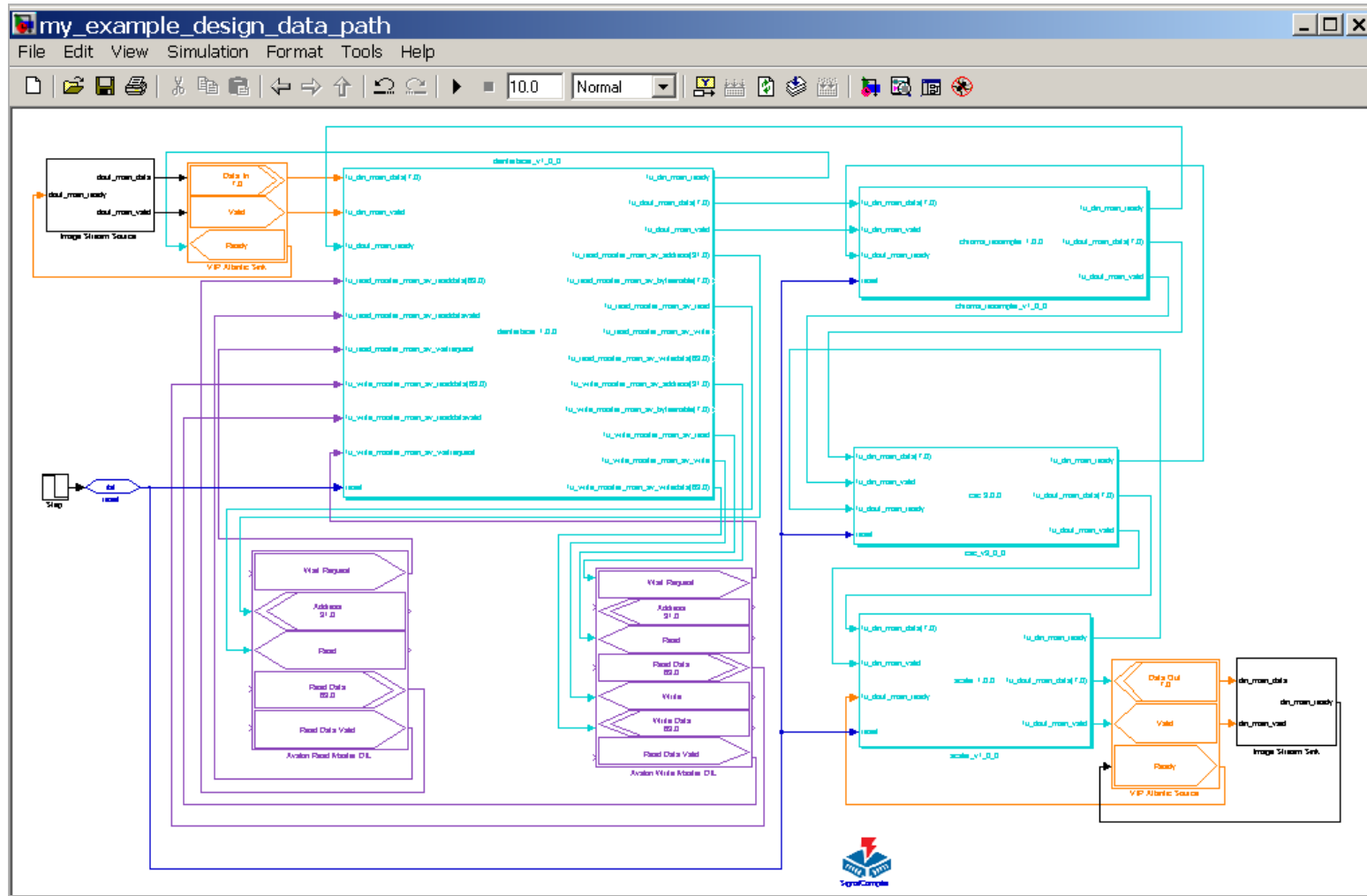
3



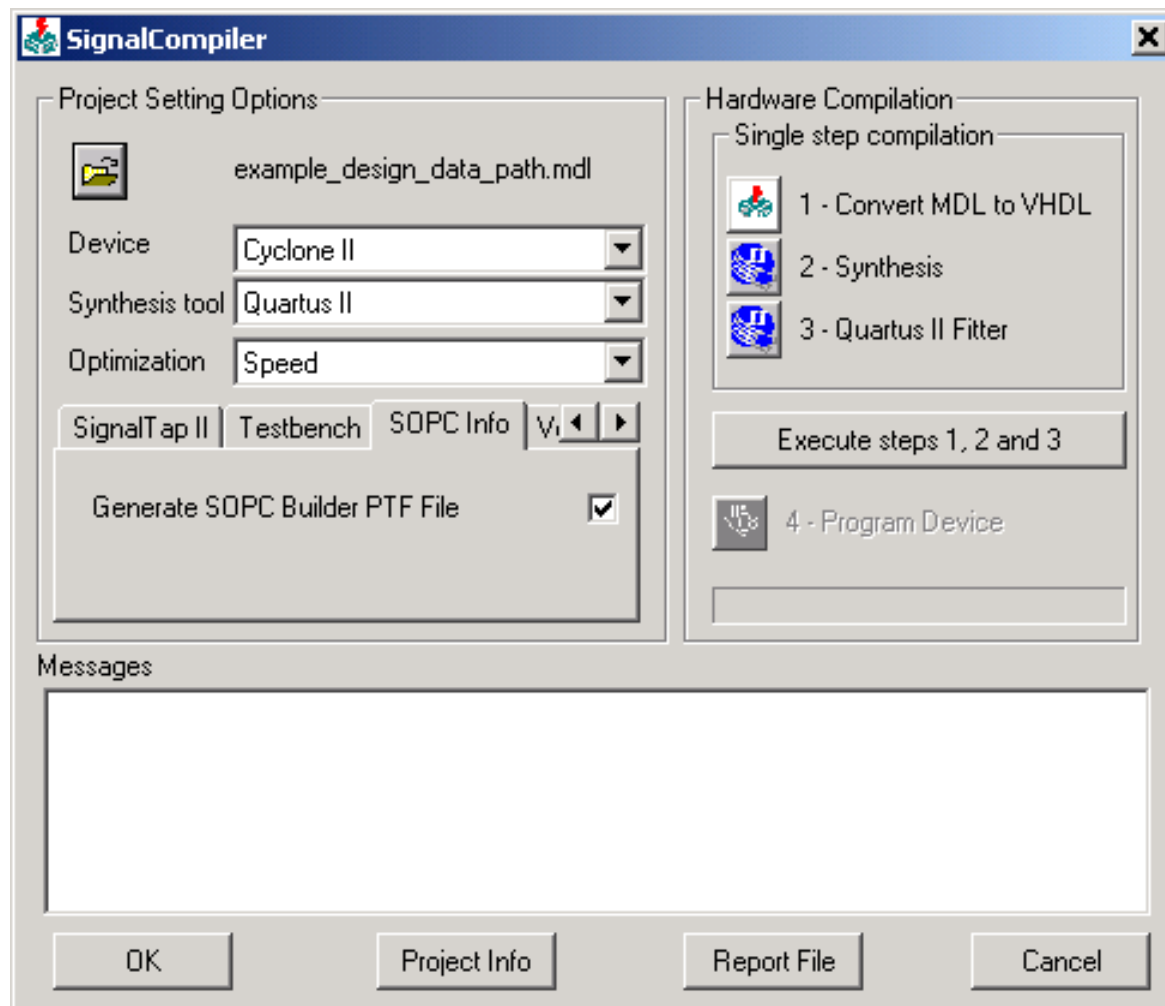
4



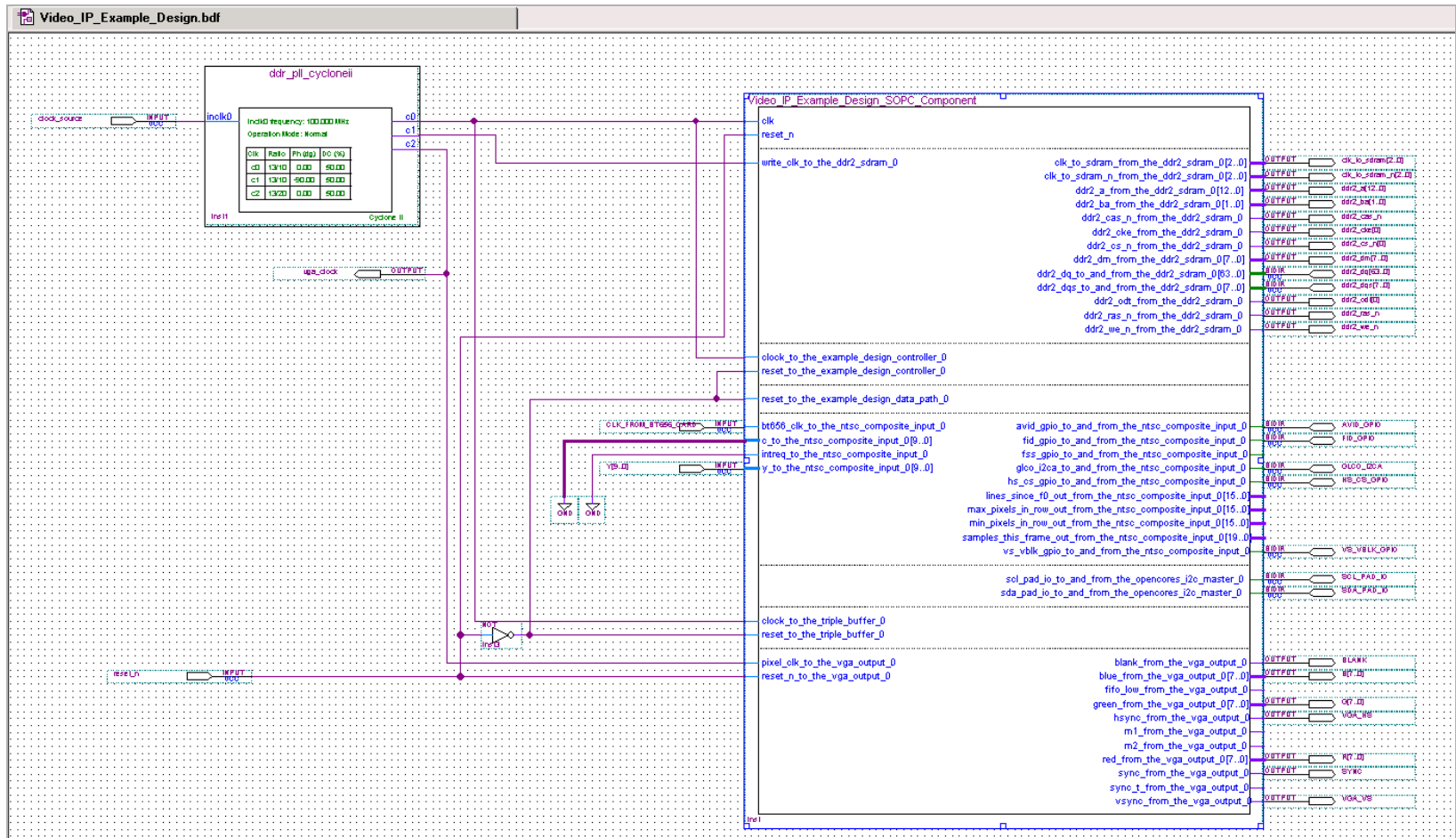
Simulation: Upconversion Subsystem



Convert to VHDL: Signal Compiler



Top-Level Design File in Quartus II



System Integration: SOPC Builder

Altera SOPC Builder - Video_IP_Example_Design_SOPC_Component

File Module System View Help

System Contents System Generation

Altera SOPC Builder

- Create New Component.
- Atlantic Components
- Avalon Components
 - Bridges
 - Communication
 - Display
 - EP1C20 Nios Developn
 - EP1S10 Nios Developn
 - EP1S40 Nios Developn
 - EP20K200E Nios Develo
 - EP2C35 Nios Developn
 - EP2S60 DSP Board Str
 - EP2S60 Nios Developn
 - Ethernet
 - Interfaces and Periph
 - Legacy Components
 - Math Coprocessors
 - Memory
 - Cypress CY7C13
 - DDR SDRAM Con
 - DDR2 SDRAM Co
 - EPCS Serial Flas
 - Flash Memory (C
 - On-Chip Memory
 - SDRAM Controlle
 - AMD 29LV800 Fl
 - IDT71V016 SRA
 - IDT71V416 SRA
 - Legacy SDRAM C
 - Microcontrollers
 - Other

All Available Components

Add... Check

Device Family: Cyclone II ☐ HardCopy Compatible

| Use | Module Name | Description | Input Clock | Base | End |
|-------------------------------------|-----------------------------|---|-------------|------------|------------|
| <input checked="" type="checkbox"/> | example_design_controller_0 | Example Design Controller | clk | | |
| <input checked="" type="checkbox"/> | master | Master port | | | |
| <input checked="" type="checkbox"/> | opencores_i2c_master_0 | OpenCores I2C Master | clk | | |
| <input checked="" type="checkbox"/> | s1 | Slave port | | | |
| <input checked="" type="checkbox"/> | ntsc_composite_input_0 | NTSC Composite Input | clk | | |
| <input checked="" type="checkbox"/> | VIPAtlanticSource | Source port | | | |
| <input checked="" type="checkbox"/> | stop_go_control | Slave port | | | |
| <input checked="" type="checkbox"/> | example_design_data_path_0 | (NOT INSTALLED) | clk | | |
| <input checked="" type="checkbox"/> | AvalonReadMasterDIL | Master port | | | |
| <input checked="" type="checkbox"/> | AvalonWriteMasterDIL | Master port | | | |
| <input checked="" type="checkbox"/> | VIPAtlanticSource | Source port | | | |
| <input checked="" type="checkbox"/> | VIPAtlanticSink | Sink port | | | |
| <input checked="" type="checkbox"/> | triple_buffer_0 | Triple Buffer | clk | | |
| <input checked="" type="checkbox"/> | din | Sink port | | | |
| <input checked="" type="checkbox"/> | dout | Source port | | | |
| <input checked="" type="checkbox"/> | read_master | Master port | | | |
| <input checked="" type="checkbox"/> | write_master | Master port | | | |
| <input checked="" type="checkbox"/> | vga_output_0 | VGA output | clk | | |
| <input checked="" type="checkbox"/> | VIPAtlanticSink | Sink port | | | |
| <input checked="" type="checkbox"/> | ddr2_sdram_0 | DDR2 SDRAM Controller MegaCore Function - ... | clk | 0x10000000 | 0x1FFFFFFF |

▲ Move Up ▼ Move Down

NTSC
BT.656

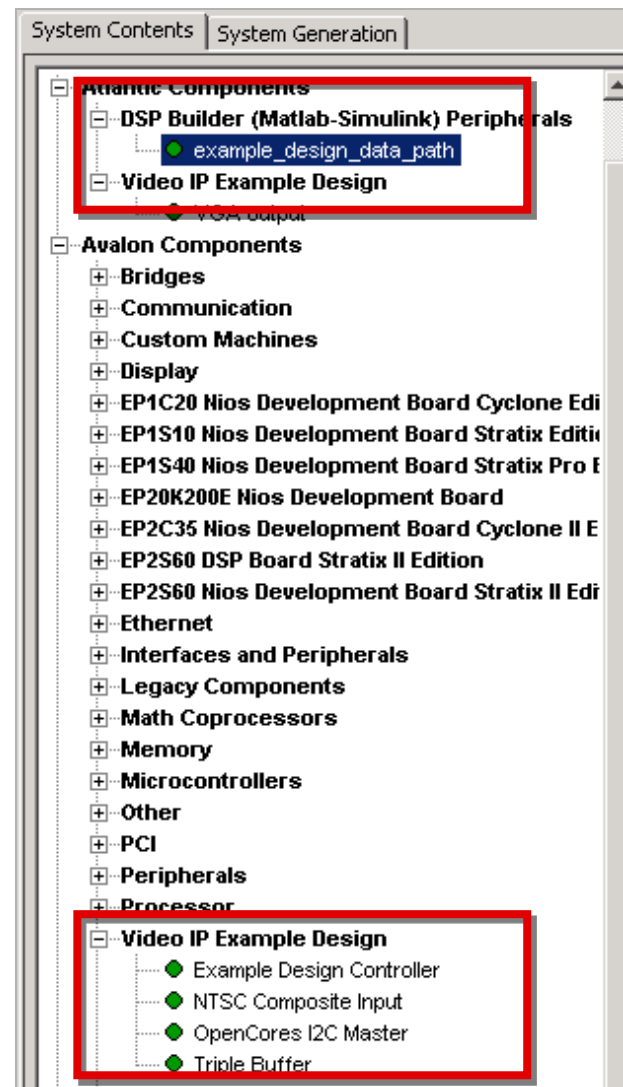
DSP Builder
- Data Path

Buffer

VGA Out
DDR2

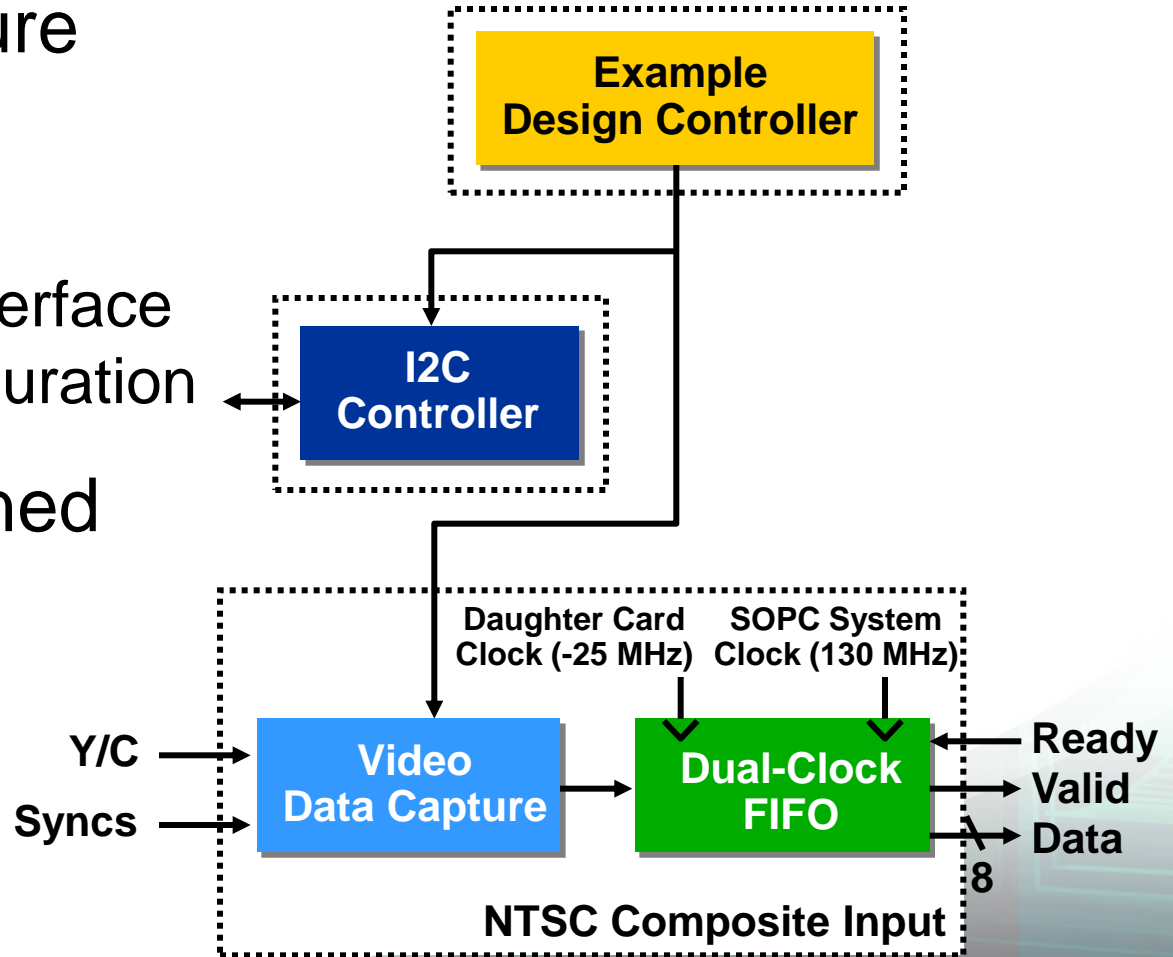
Custom Hardware

- Generated custom video interfaces IP
 - Available within reference design package



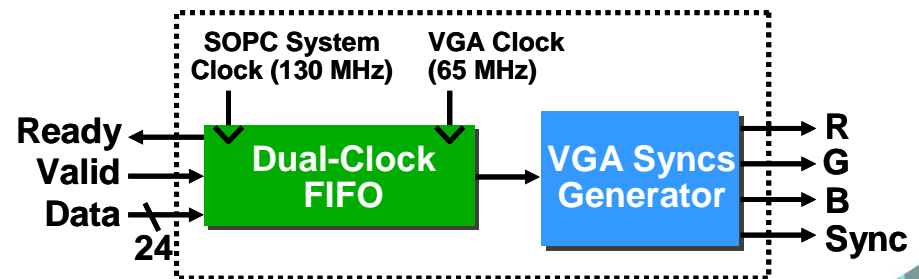
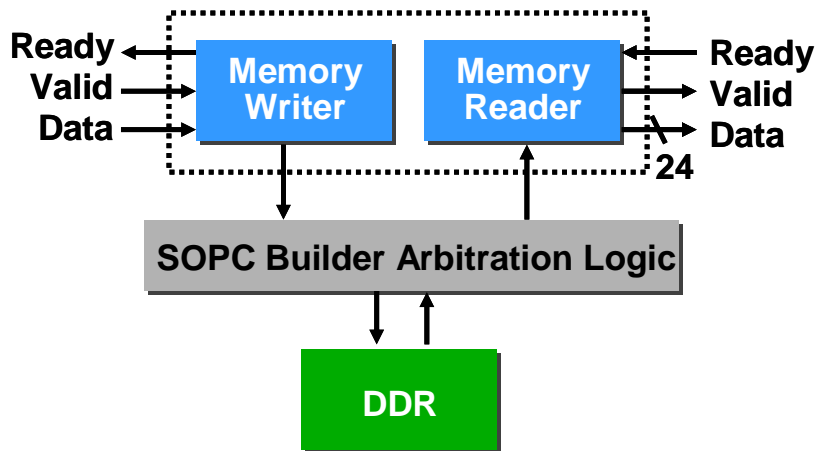
■ Video data capture with TI TVP5146 decoder

- Controller designed in HDL
 - Imported into SOPC Builder

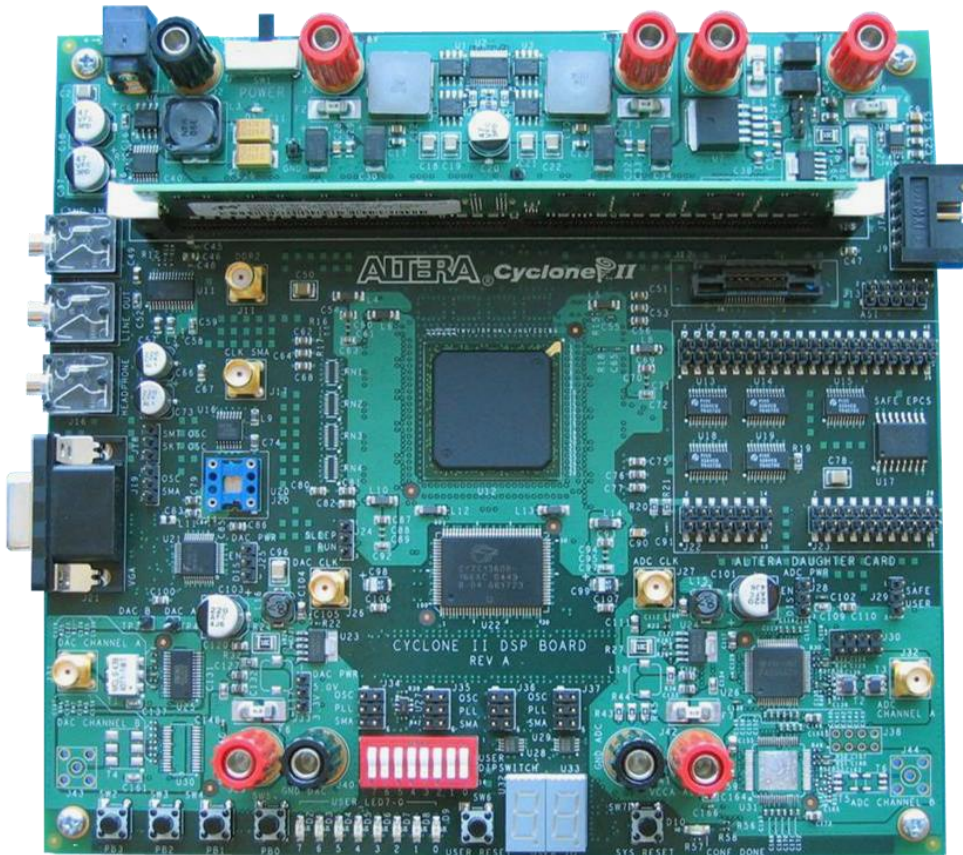


Triple Buffer and VGA Output

- Allows inputs and output to run asynchronously and at different frame rates
 - Video output: 1,024 x 768 progressive at 30 frame/s
 - VGA output: must run at least 60 fps
- HDL design, imported into SOPC Builder



Video Development Kit, Cyclone II Edition



- Device: EP2C70
- Bundled software:
 - Quartus II development kit edition
 - DSP Builder
 - MATLAB/Simulink evaluation software
 - Altera OpenCore® Plus evaluation IP
- Includes video input daughter card

Video Input Daughter Card

■ Features:

- Dual composite video inputs (NTSC & PAL)
- Compatible with other Altera development boards that feature a Santa Cruz connector



Download to Hardware

■ Resource utilization

- 9,500 logic elements, 48 M4K, 11 multipliers
- Fits in EP2C15 device

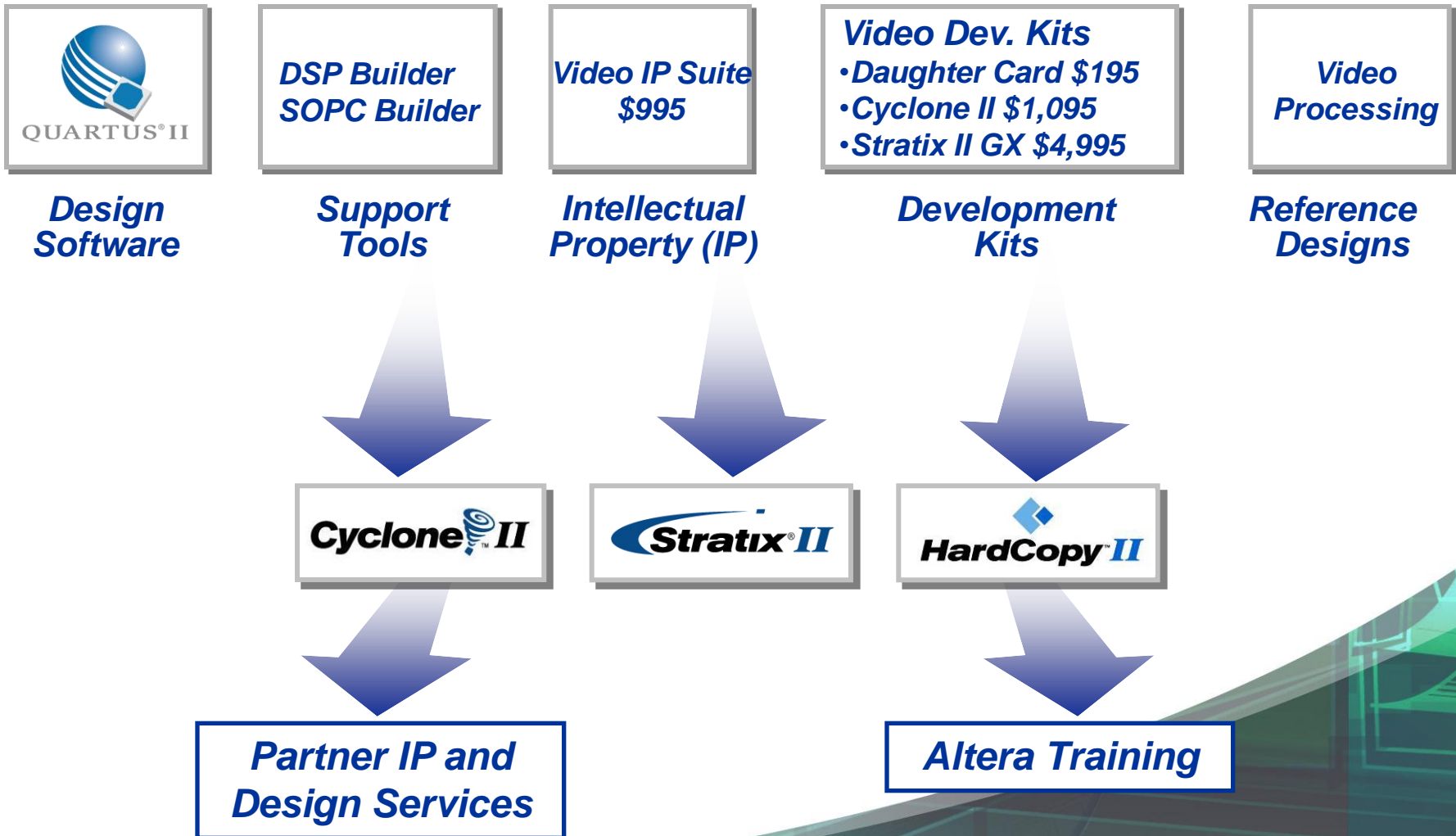
■ Program Video Development Kit, Cyclone II Edition

■ Hardware debug

- JTAG/SignalTap[®] logic analyzer

Getting Started

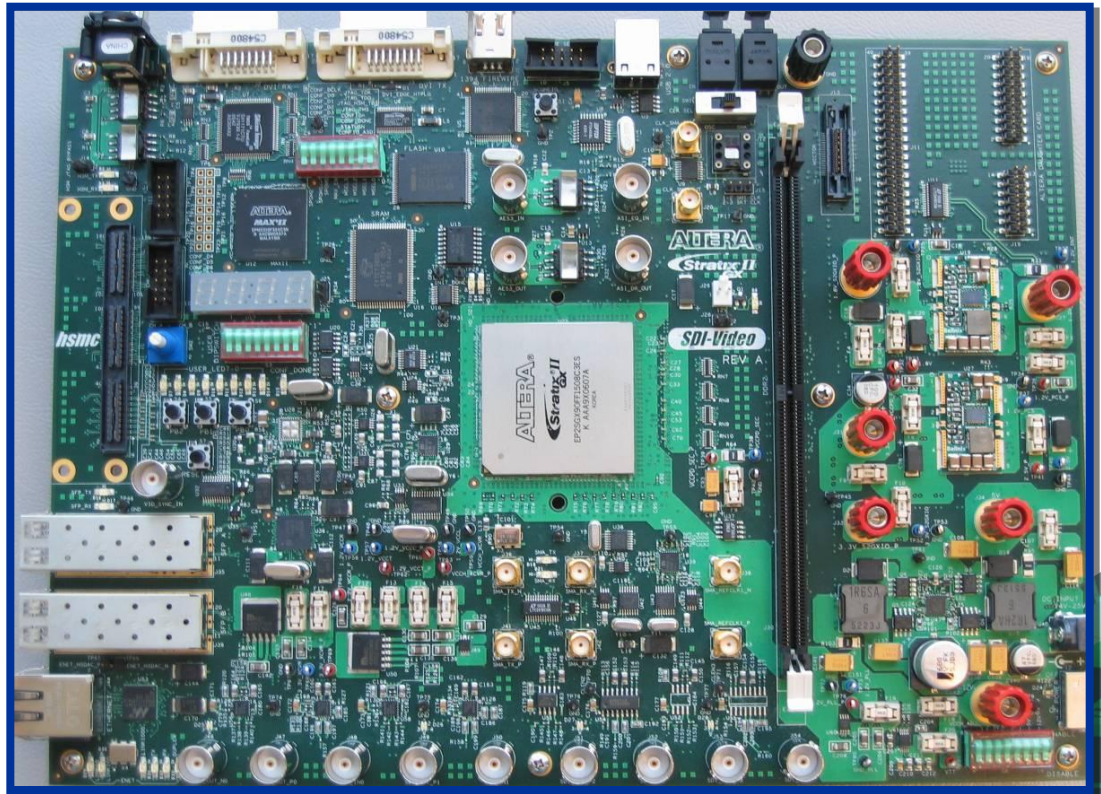
Altera Video Solutions



Audio Video Development Kit, Stratix II GX Edition

- Device: EP2SGX90
- Video interfaces:
 - 4 SDI/HD-SDI channels
 - DVI
- Audio interfaces:
 - AES3/EBU, SPDIF
- High-speed data interfaces:
 - ASI
 - FireWire (IEEE1394)
 - USB 2.0
 - 10/100/1000 Ethernet
- Bundled with SDI and video processing

reference design



Get Started Now

| Product | Description | Ordering Code | Price |
|---|---|-------------------|---------|
| Video and Image Processing Suite | 9 video and image processing IP cores | IPS-VIDEO | \$995 |
| Video Development Kit, Cyclone II Edition | Cyclone II DSP board + video input daughtercard | DK-VIDEO-2C70N | \$1,095 |
| Video Input Daughter Card | 2 composite video inputs (NTSC/PAL Support) | DC-VIDEO-TVP5146N | \$195 |
| Audio Video Development Kit, Stratix II GX Edition | Stratix II GX video board with ASI, SDI, DVI, Gigabit Ethernet, FireWire, USB2.0, S/PDIF, AES | DK-VIDEO-2SGX90N | \$4,995 |


```
nbit_adder: adderx
    GENERIC MAP (x => n)
    PORT MAP (AddSubR_n, G, H, M, carry_in);
multiplexer: mux2to1
    GENERIC MAP (x => n)
    PORT MAP (A, B, Z, S, carry_in);
AddSubR_n <= (OTHERS => AddSubR_1)
M <= Z XOR AddSubR_n
carry_out XOR G(n-1) XOR H(n-1) XOR M(n-1);
```

Thank You

Q & A