Enhance System Performance and Productivity by Leveraging DSP and Embedded Technologies in FPGA Designs

Agenda

- Embedded and digital signal processing (DSP) design challenges and solutions
- DSP coprocessing
- Nios® II C-to-Hardware (C2H) Acceleration Compiler
- Quartus® II software highlighted features
- Conclusion

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Product Evolution

1985

Mobile phone

2007

Phone, diary, email, SMS, web browser, alarm clock, calendar, voice recorder, radio, MP3 player, camera, etc…

Constant Demand for New Features; Higher Performance and Lower Costs

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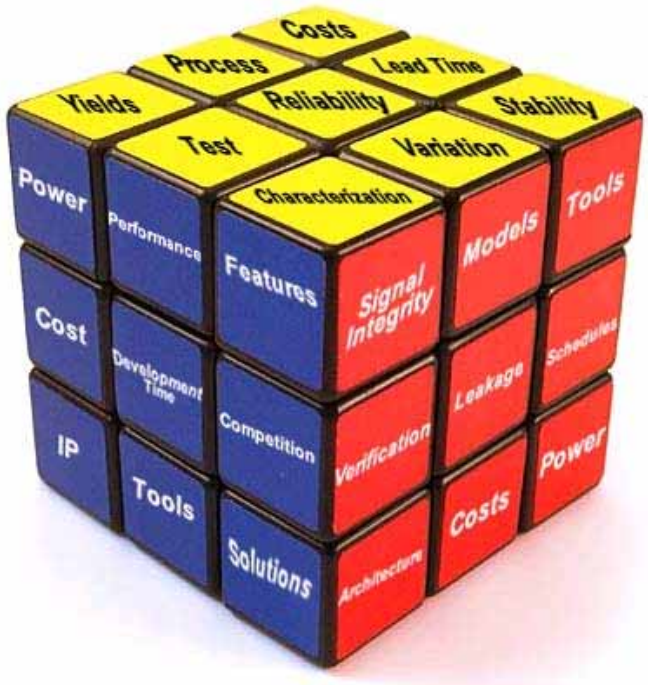
Embedded and DSP Design Challenges

Productivity



Performance

Flexibility

FPGAs Tackle These Challenges Head On

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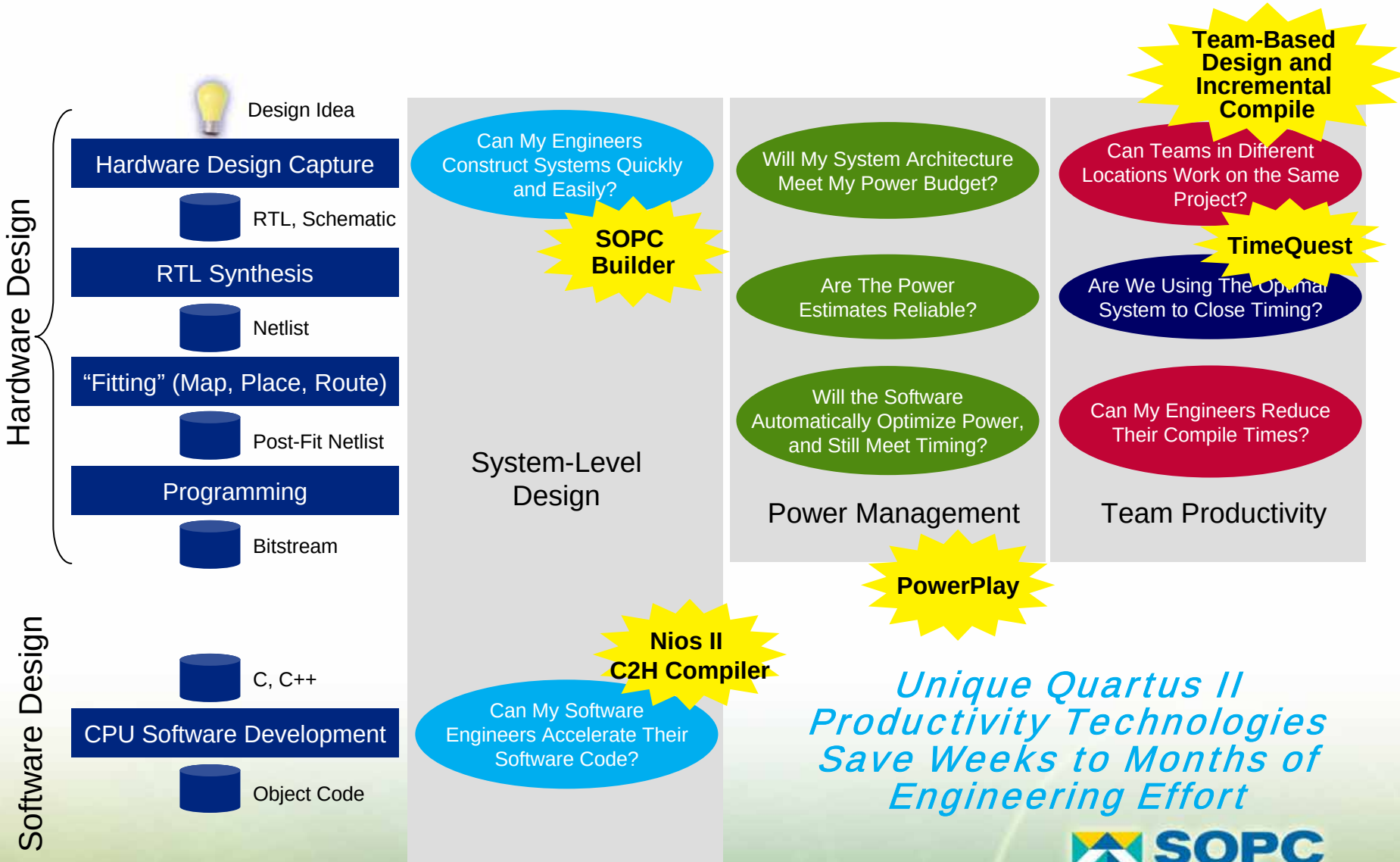
Solution on Productivity–Tool



Unique Quartus II Productivity Technologies Save Weeks to Months of Engineering Effort

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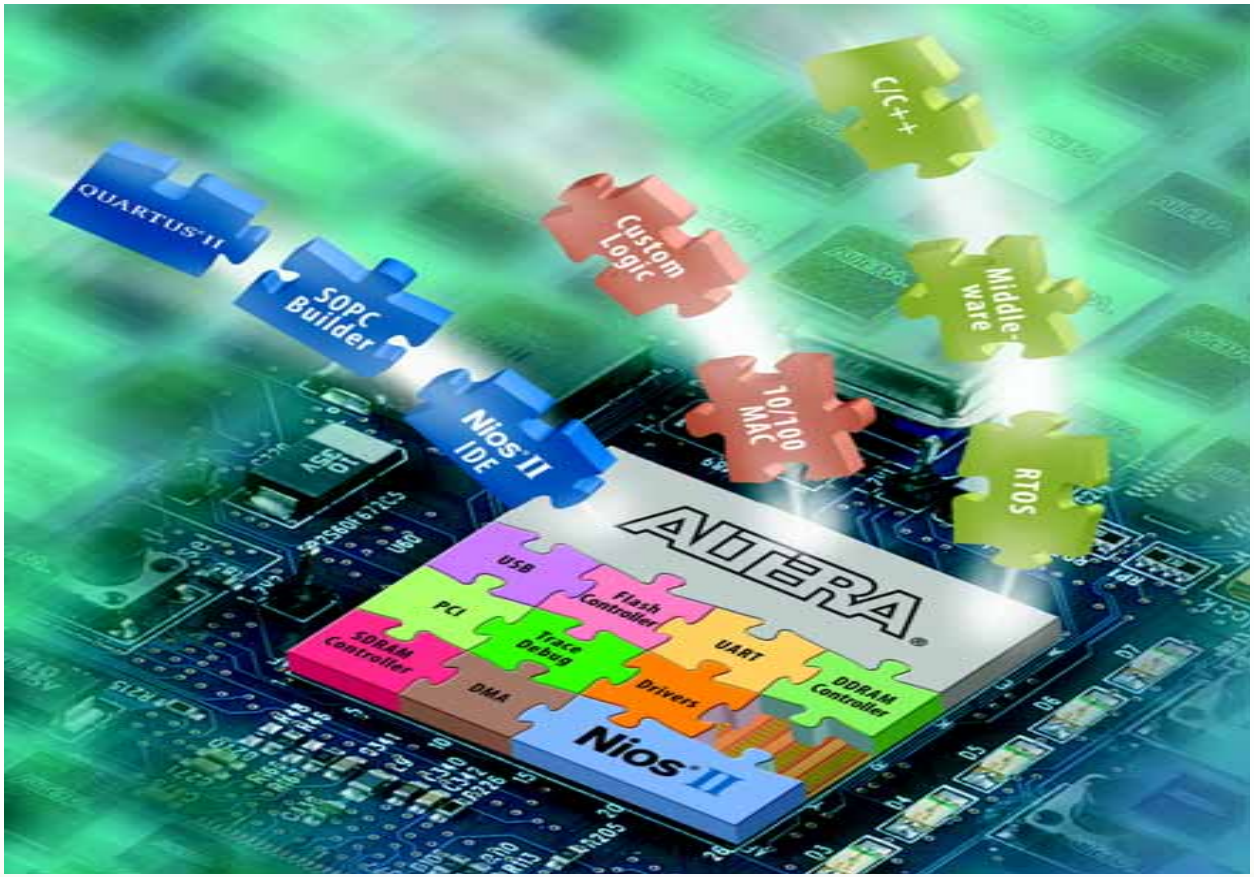
Solution on Flexibility–FPGAs



FPGA is the Poster Child for Flexibility;
Rapidly Prototype System and Feature Fill Over Time

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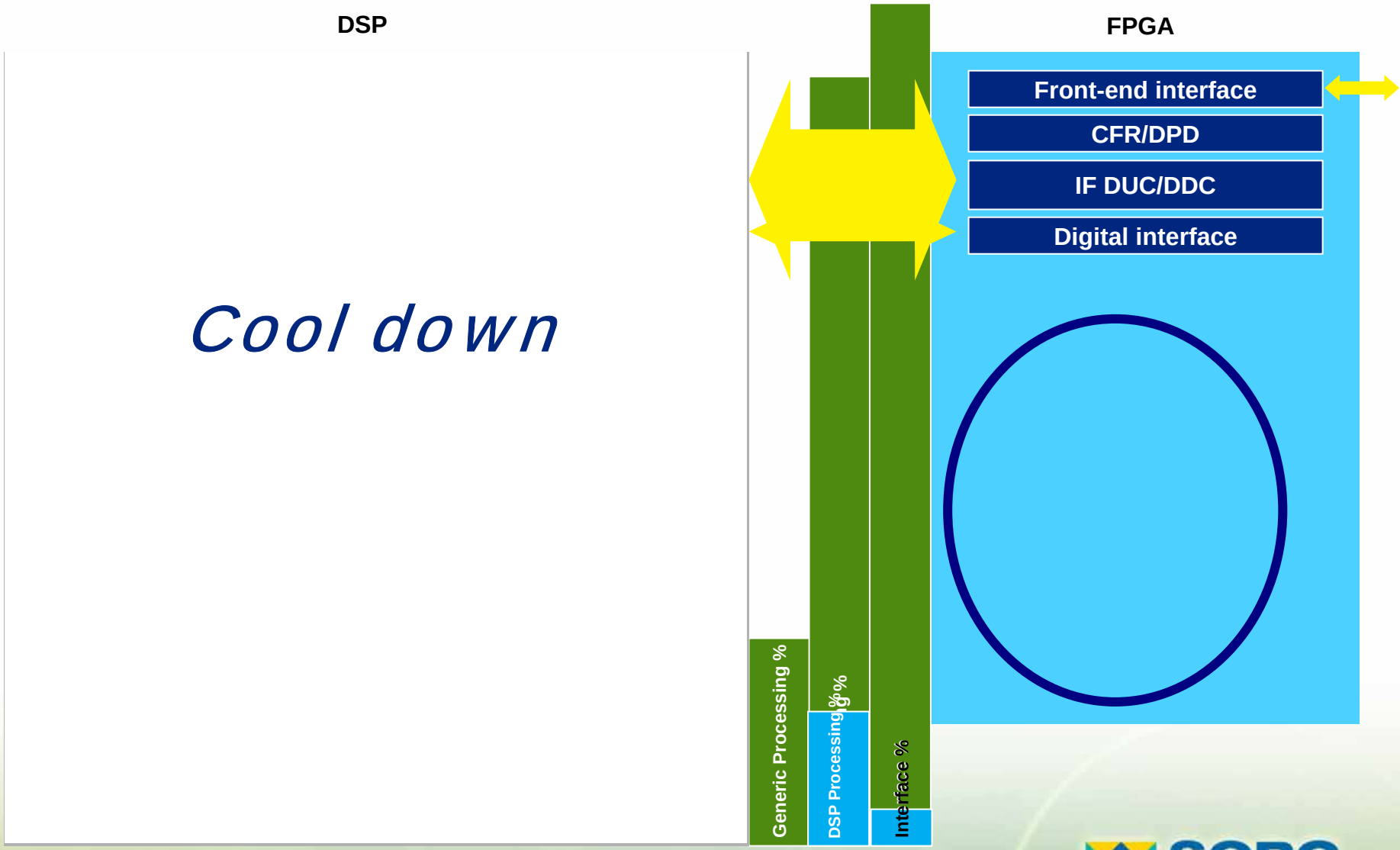
Solution on Performance (1): FPGA Single Chip

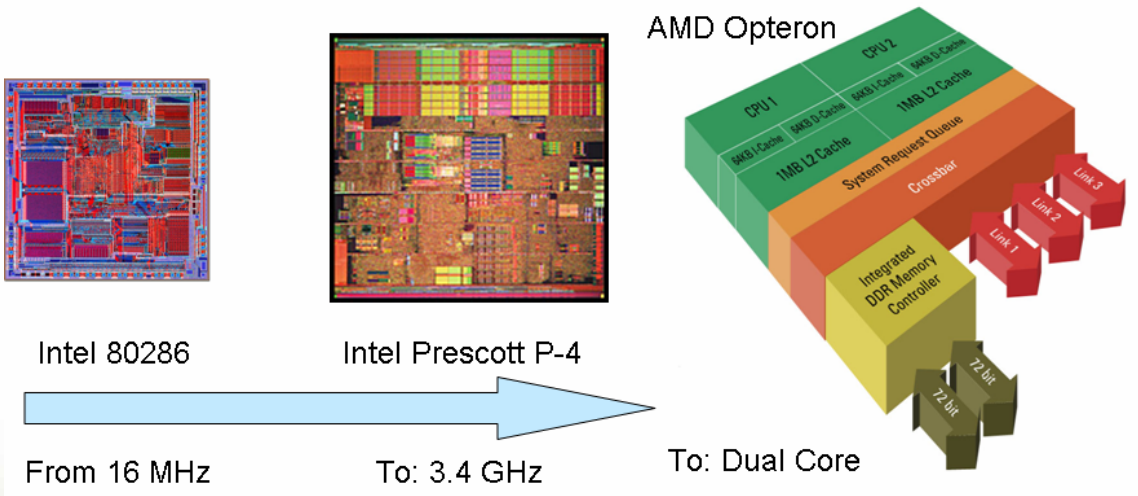
Solution on Performance (2): DSP+FPGA Coprocessing



DSP Coprocessing

CPU Challenges

- Processor speedup isn't there
- Performance limited by power
- Memory bandwidth limitations
- Single-core performance reaching a limit



Multi-core announcements by Intel, AMD, ARM, and others

Processor Model Challenges For HPC

- Memory bandwidth limited by package and pin count
- Multiple caches required to keep the microprocessor busy
- Multi-processor cache coherency problem eats up performance gains
- Most of the power consumption is in the cache and related controllers
- But many HPC applications derive little or no benefit from cache

Source: Prof. John Wawrzynek, BWRC, UC Berkeley

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Overall Customer Requirements

- **Performance**: 10X – 100X algorithm and 3X – 50X application acceleration
- **Productivity**: Simplicity of the tool chain; reduce the effort
- **Power**: Better performance-to-power ratio
- **Price**: Compared to alternatives

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Performance—FPGA Algorithm Acceleration

- 10X-100X at algorithm level
- Typically 3X-50X at application level
- Varies by vertical
  - 10X for medical imaging
  - 20-50X for financial

Application	Processor only	FPGA Crocessing	Speed Up
Hough and inverse Hough processing	12 minutes processing time Pentium 4-3 GHz	2 seconds of processing time @ 20 MHz	370x faster
AES 1MB data processing/crypto rate *Encryption* *Decryption*	 5,558 ms/1.51 Mbps 5,562 ms/1.51 Mbps	 424 ms/19.7 Mbps 424 ms/19.7 Mbps	13x faster
Smith-Waterman search34 from FASTA	6461 sec processing time (Opteron)	100 sec FPGA processing	64x faster
Multi-dimensional hypercube search	119.5 sec (Opteron 2.2 GHz)	1.06 sec FPGA @ 140 MHz	113x faster
Callable Monte-Carlo analysis (64,000 paths)	100 sec processing time (Opteron 2.4 GHz)	10 sec of processing @ 200 MHz FPGA	10x faster
BJM financial analysis (5M paths)	6300 sec processing time (Pentium 4-1.5 GHz)	242 sec of processing @ 61 MHz FPGA	26x faster
Mersenne Twister random number generation	10M 32-bit integers/sec (Opteron-2.2 GHz)	319M 32-bit integers/sec	3x faster

Source: AMD

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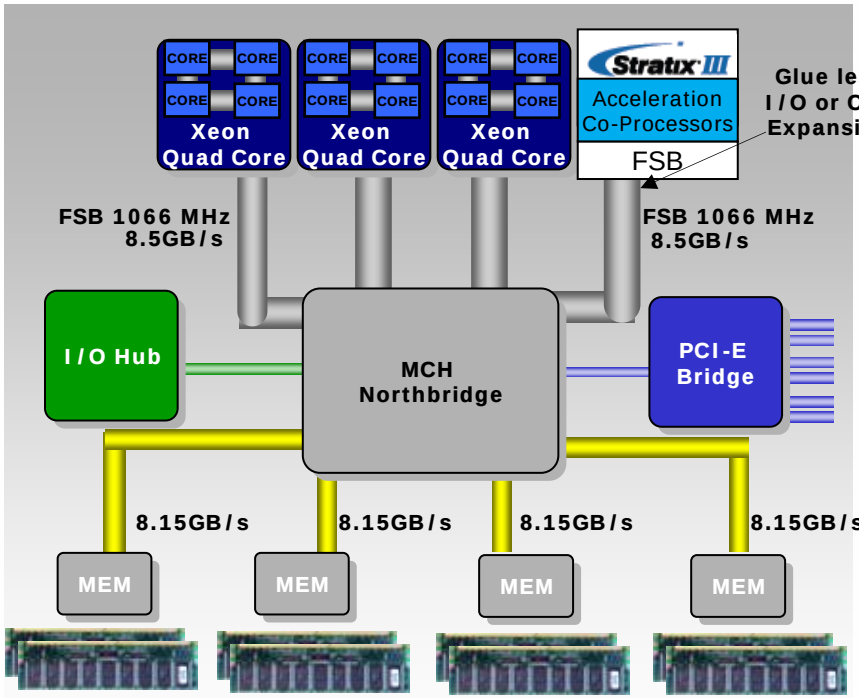
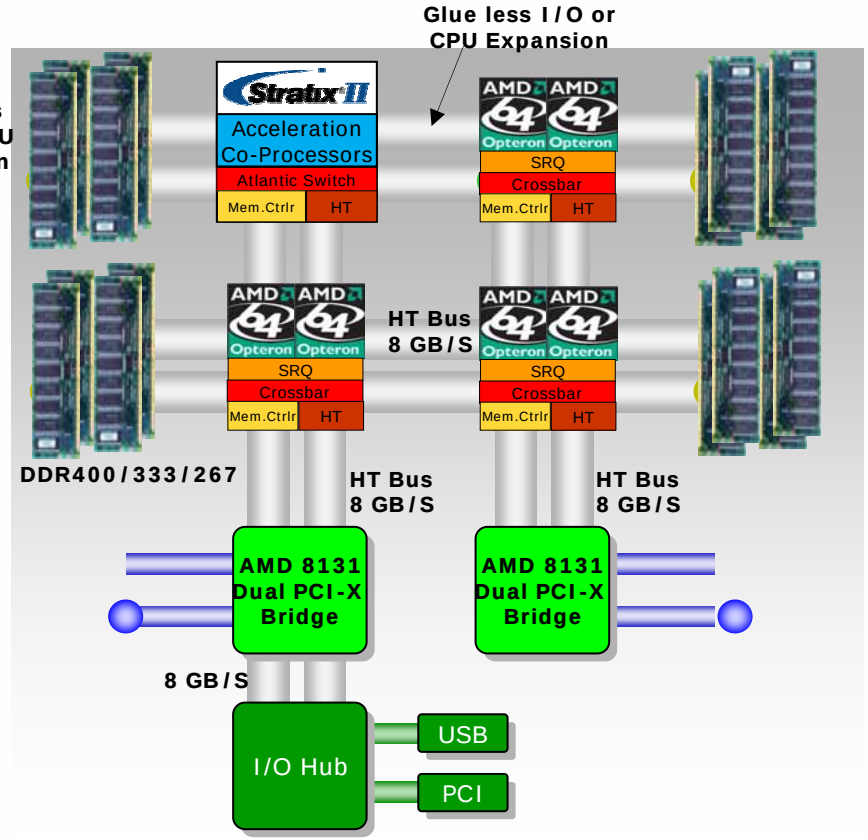
Co-Processing Architectures





Intel Xeon® Architecture

- Uses Front Side Bus (FSB) Interconnect
- Latest North Bridge has FSB interface for each CPU
- Xeon Quad Core presentation available: http://www.intel.com/pressroom/kits/quadcore/qc_pressbriefing.pdf

AMD Opteron™ Architecture

- Uses HyperTransport Interconnect
- Industry-standard AMD64 technology
- Socket modules available for Opteron
- AMD Torrenza web site: http://enterprise.amd.com/us-en/AMD-Business/Technology-Home/Torrenza.aspx

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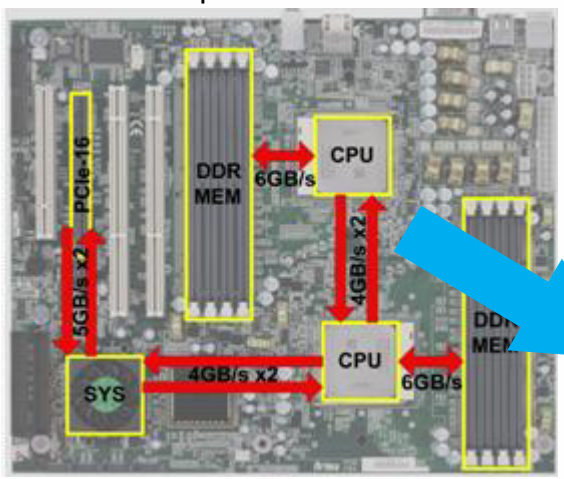
Commercially Available Platform

XtremeData, Inc.
COMPUTING REDEFINED

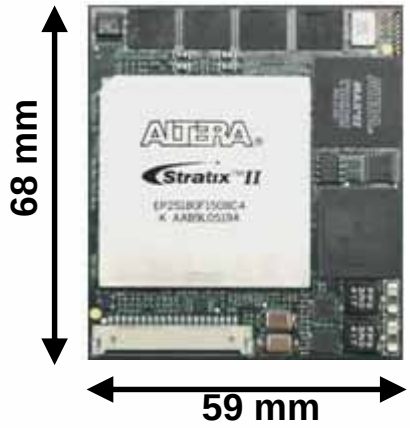
AMD Opteron Motherboard:



X86 HPC Solution

Idea: build a simple, minimalist board with interfaces to HyperTransport and memory: (patent pending)

Drop-in replacement for an AMD Opteron with *no* changes to motherboard!



Simply remove Opteron and replace with FPGA board!

- FPGA uses all motherboard resources meant for CPU:
  - HyperTransport links, memory interface, power supply, heat-sink
- Usable with any AMD Opteron (or future Intel CSI-enabled CPUs) server
- Usable in rack-mount or high-density, “blade” server systems, where
  - Plug-in boards are not feasible

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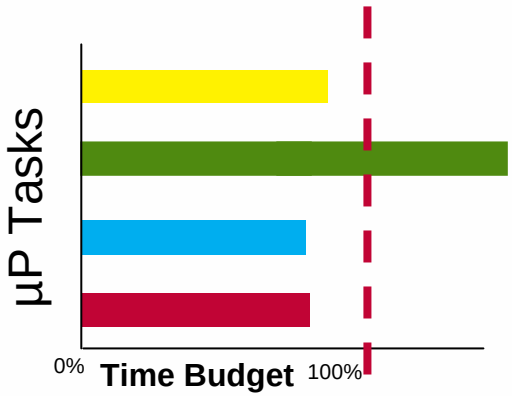
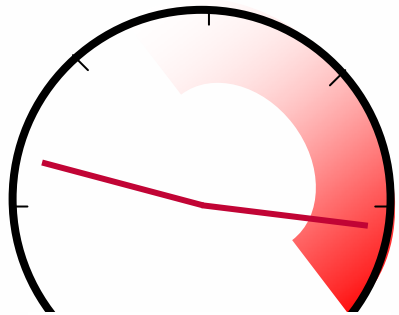
C2H (C to Hardware) Tool

Boosting Software Performance



Your Application

Faster Processor



Clock Frequency (MHz)

If you choose a faster processor

- *More expensive **$$$$***
- *Consumes more power*
- *Requires board redesign*

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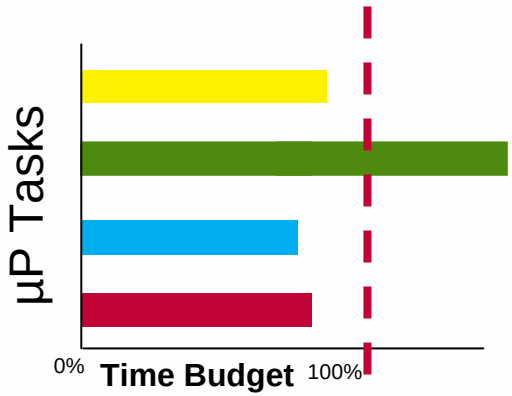
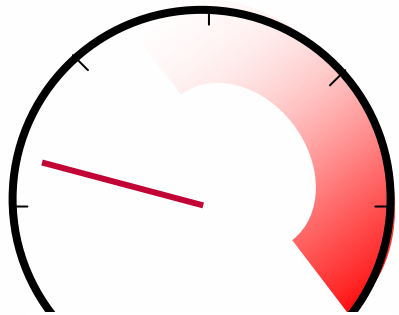
Boosting Software Performance



Your Application



Nios II Clock Frequency (MHz)

Multiply software performance.
Accelerate only what's necessary.
Don't pay for performance you don't need.

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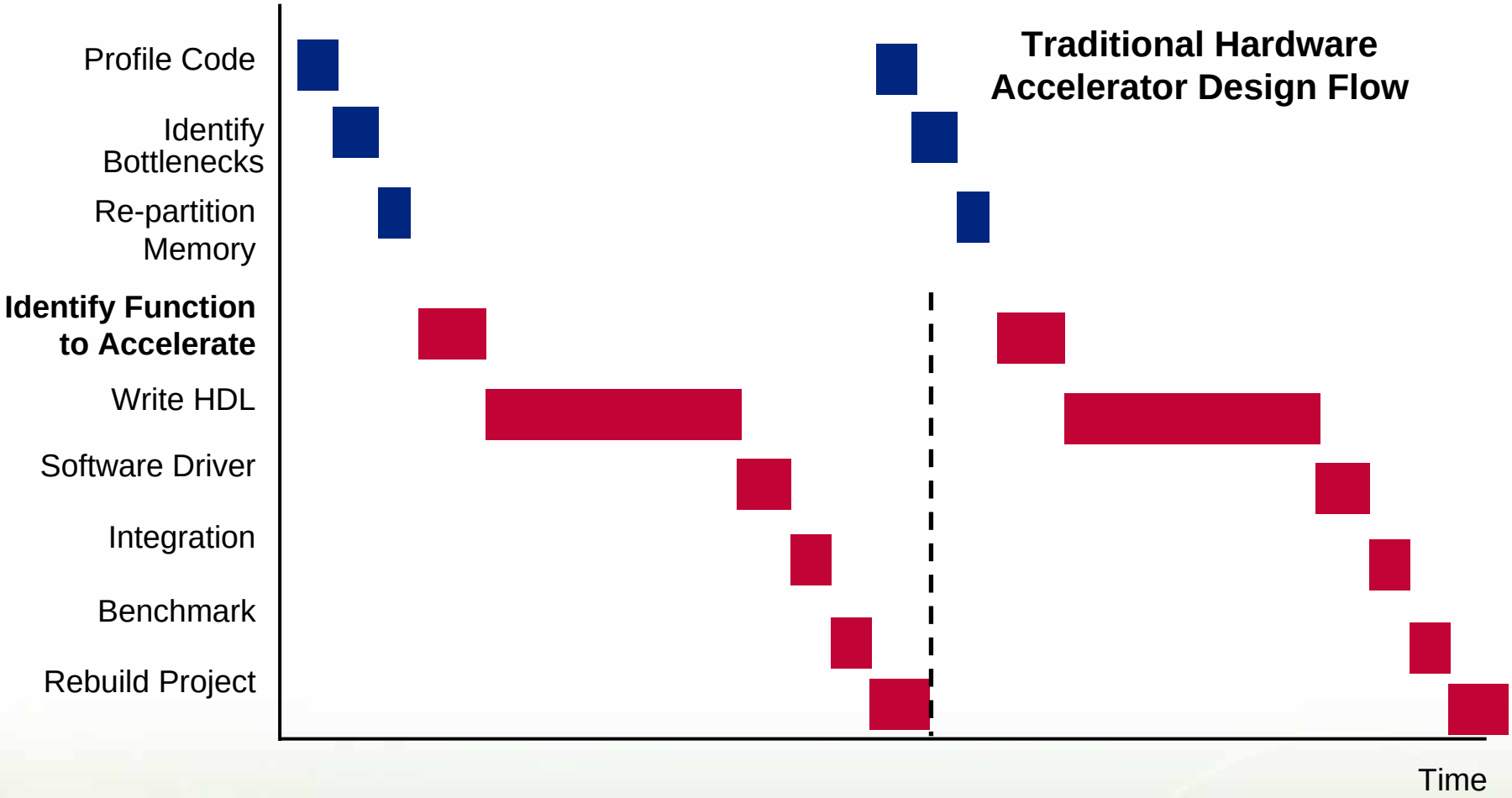
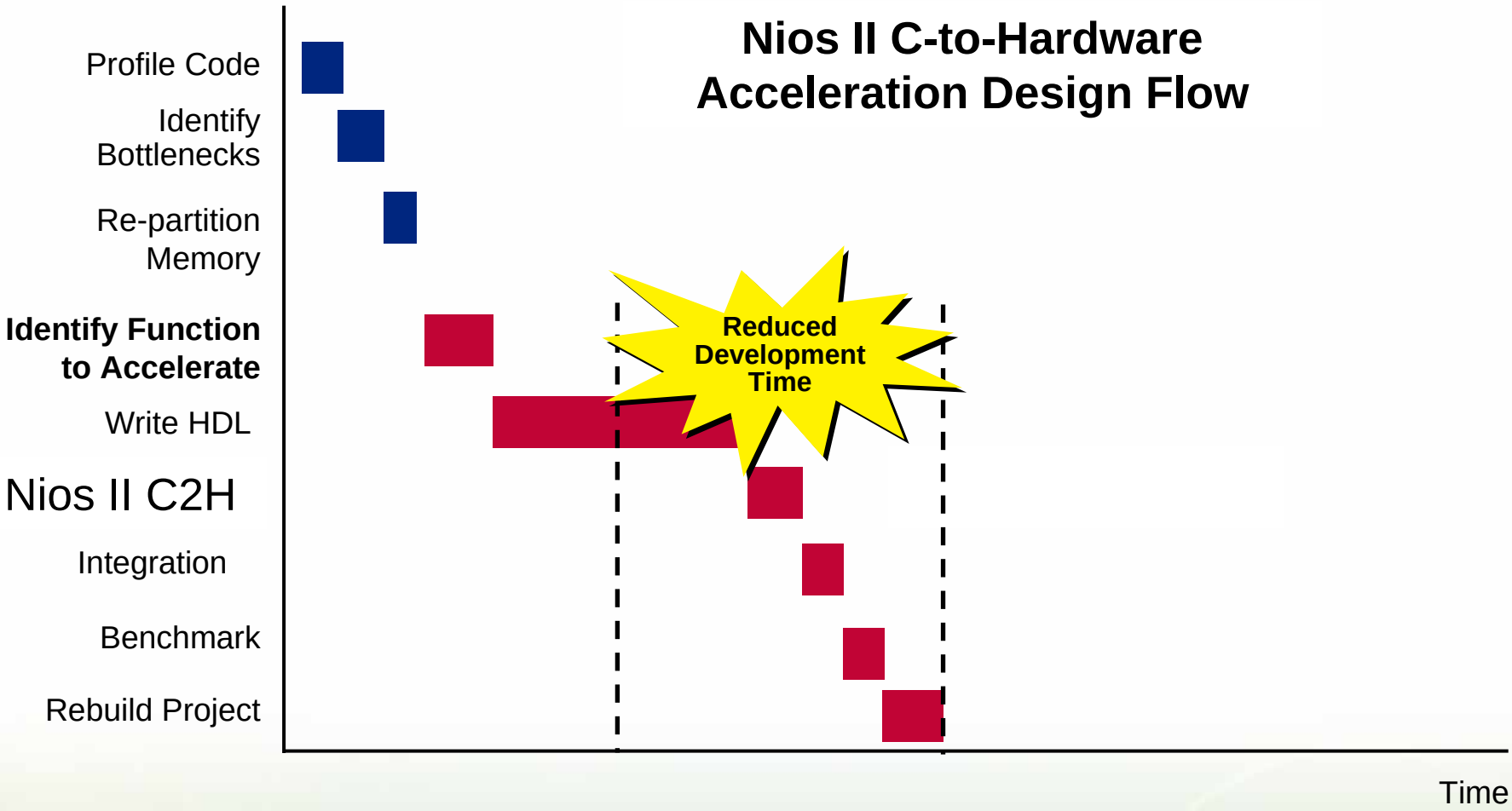
Hardware Acceleration Flow

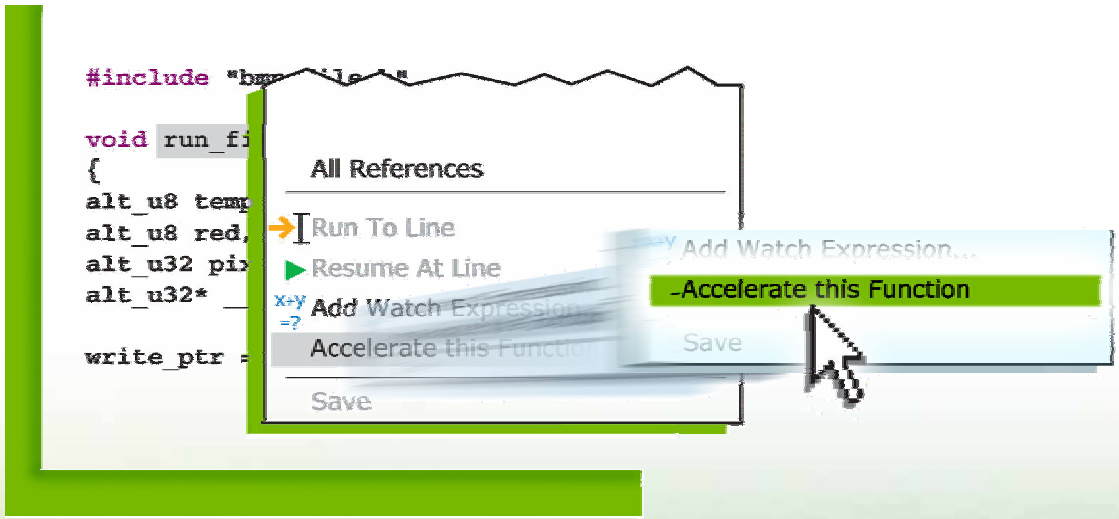


Hardware Acceleration Flow



Nios II C-to-Hardware Acceleration Compiler

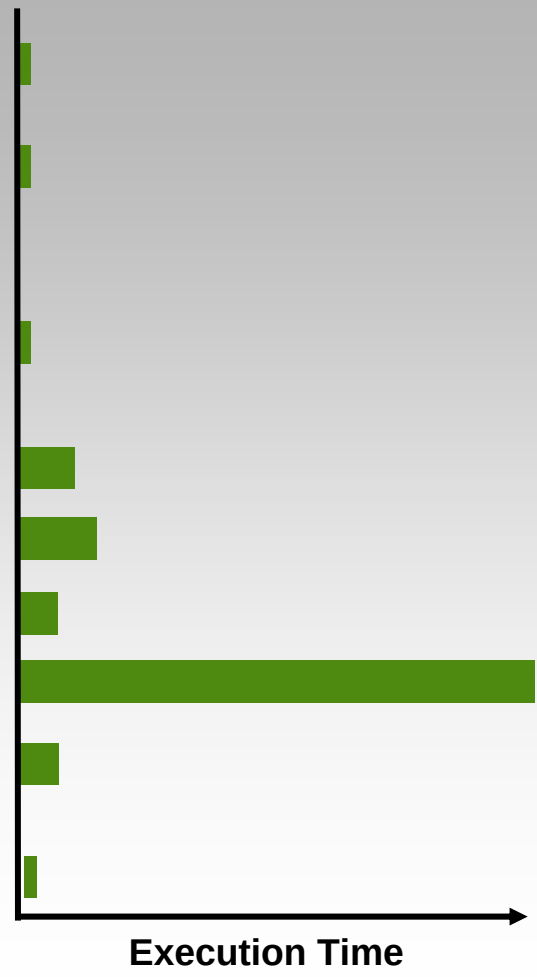
- Productivity tool that automates creation and integration of hardware accelerators
- Streamlines C acceleration—you don't have to know how to design hardware
- Integrated in familiar Eclipse-based Altera® Nios II Integrated Development Environment (IDE)



Right Click to *Accelerate*

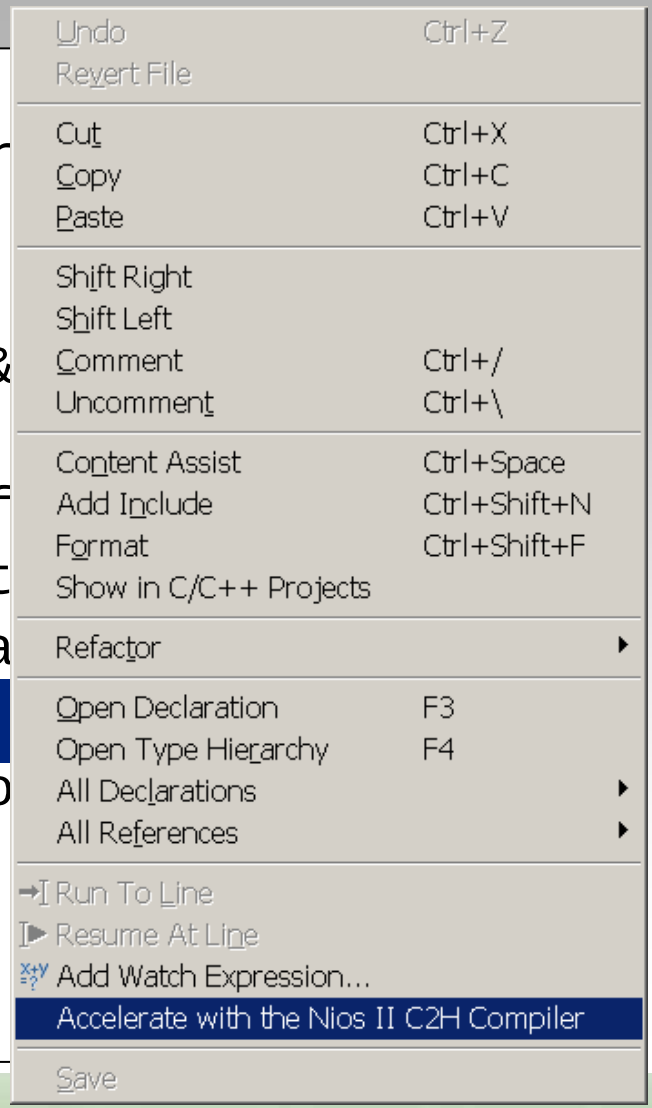
Step 1: Identify Software Bottlenecks

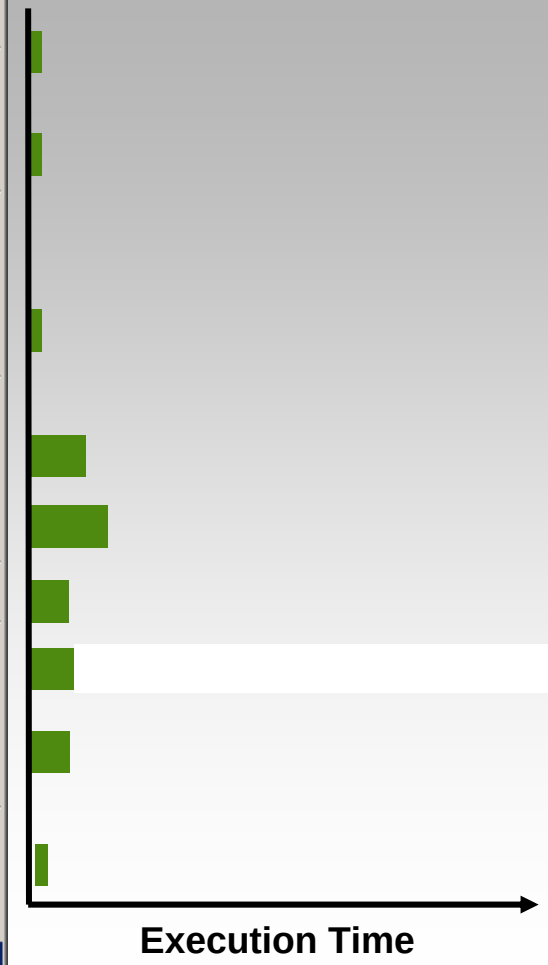
```
main ()
{ …variable declarations…
  init();

  while (!error && got_data())
  {
    do_user_interface();
    gather_statistics();
    if (got_new_data())
      d_transform(in_buf, out_buf);
    check_for_errors();
  }
  cleanup();
}
```



Step 2: Right Click to *Accelerate*

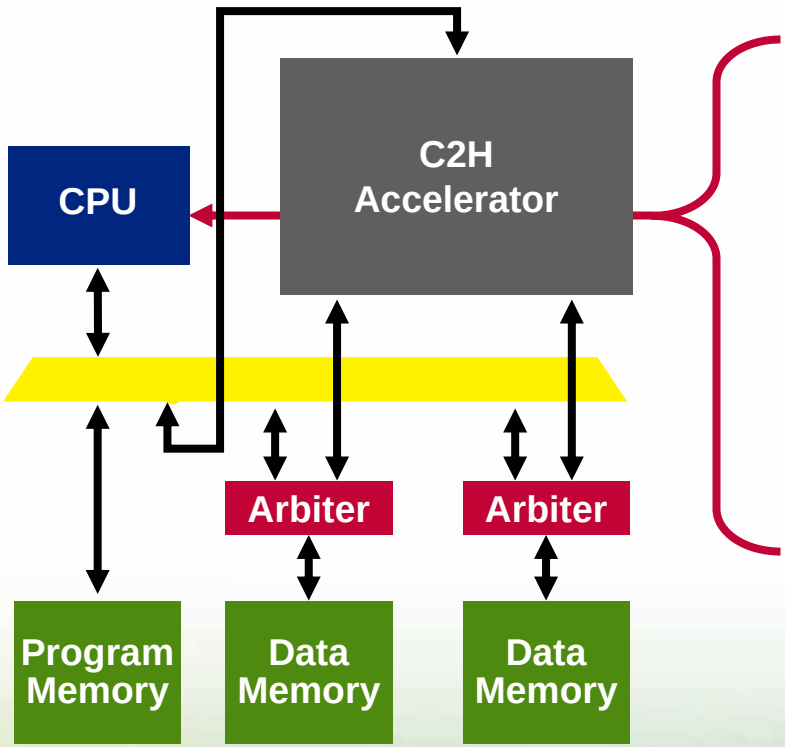
```
main ()
{ …variable declar
  init();

  while (!error &&
  {
    do_user_interf
    gather_statist
    if (got_new_da
      d_transform
    check_for_erro
  }
  cleanup();
}
```





What Does Nios II C2H Compiler Do?

- Generates a custom hardware accelerator from an ANSI C function



*c2h_dma.c

```
13
14
15int do_dma( int * __restrict__ dest_ptr,
16           int * __restrict__ source_ptr,
17           int length )
18{
19  int i;
20
21  for( i = 0; i < (length / 4); i++ )
22  {
23    *dest_ptr++ = *source_ptr++;
24  }
25  return( 0 );
26}
27
```

C2H: Nios C-to-Hardware Acceleration Compiler

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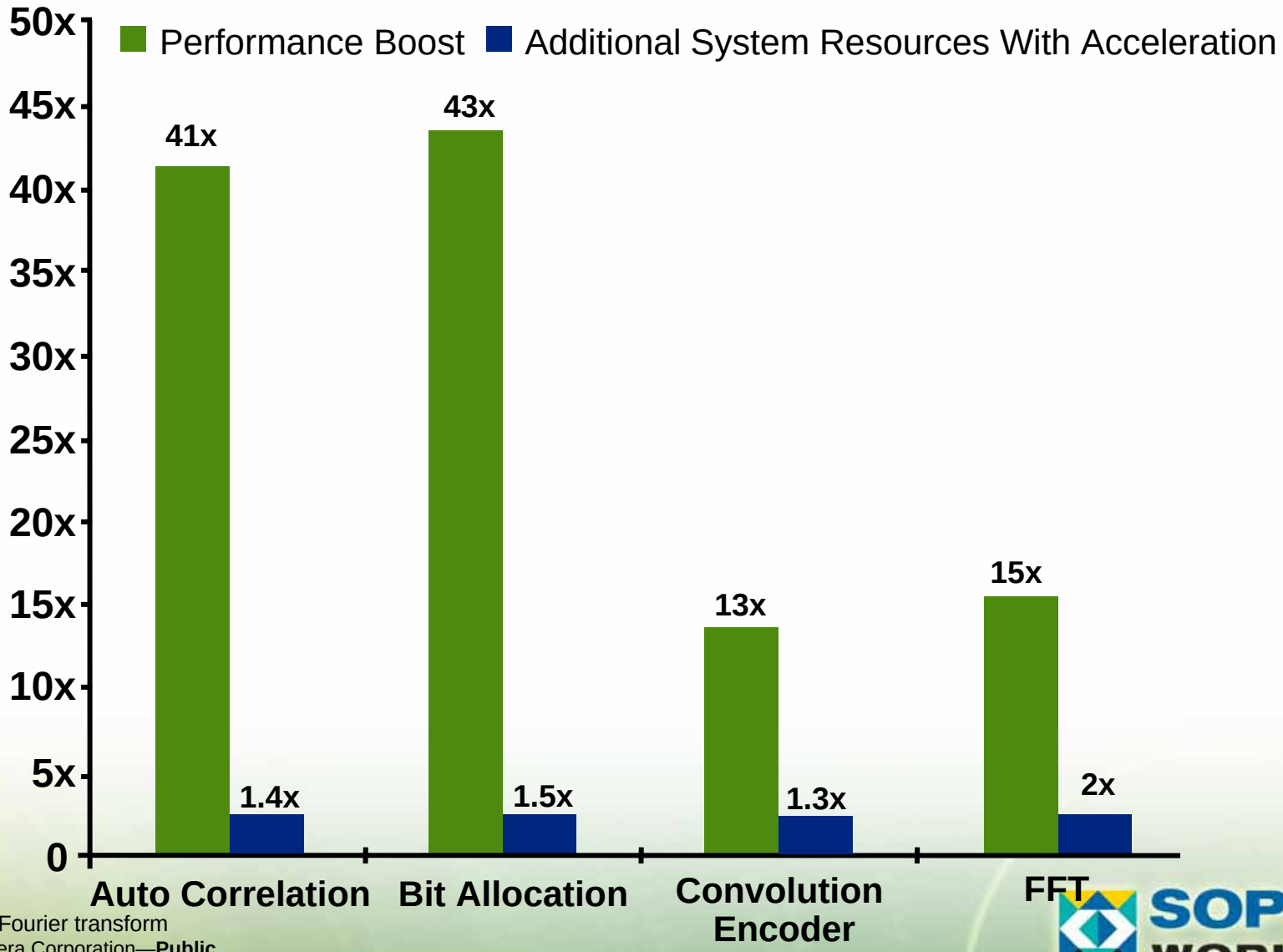
Dramatic Performance Boost



FFT: fast Fourier transform

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EEMBC Image Rotate

(95 MHz)

Software-implemented image rotate:

3773 iterations/second

> $100

Hardware-accelerated image rotate

3926 iterations/second

Performance

Cost

1.4-GHz Processor

ALTERA Cyclone II

Nios II processor

Accelerator

No compiler optimization

Compiler optimization, 1200 LEs for Nios II/s processor, 1200 LEs for accelerator

As fast as a 1.4-GHz processor for $1.42 of logic in a Cyclone® II FPGA

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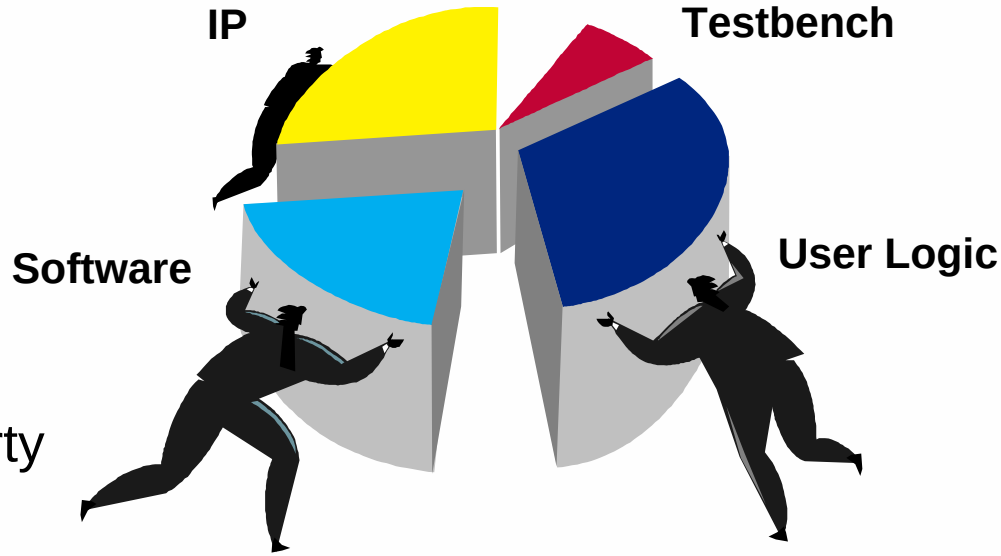
Quartus II Highlighted Features

- SOPC Builder
- PowerPlay
- TimeQuest

SOPC Builder – The Tool

- Automates block-based design
  - System definition
  - Component integration
  - System verification
  - Software generation
- Fast and easy
- Supports design reuse
  - 3rd Party intellectual property (IP) Cores
  - Internally developed IP



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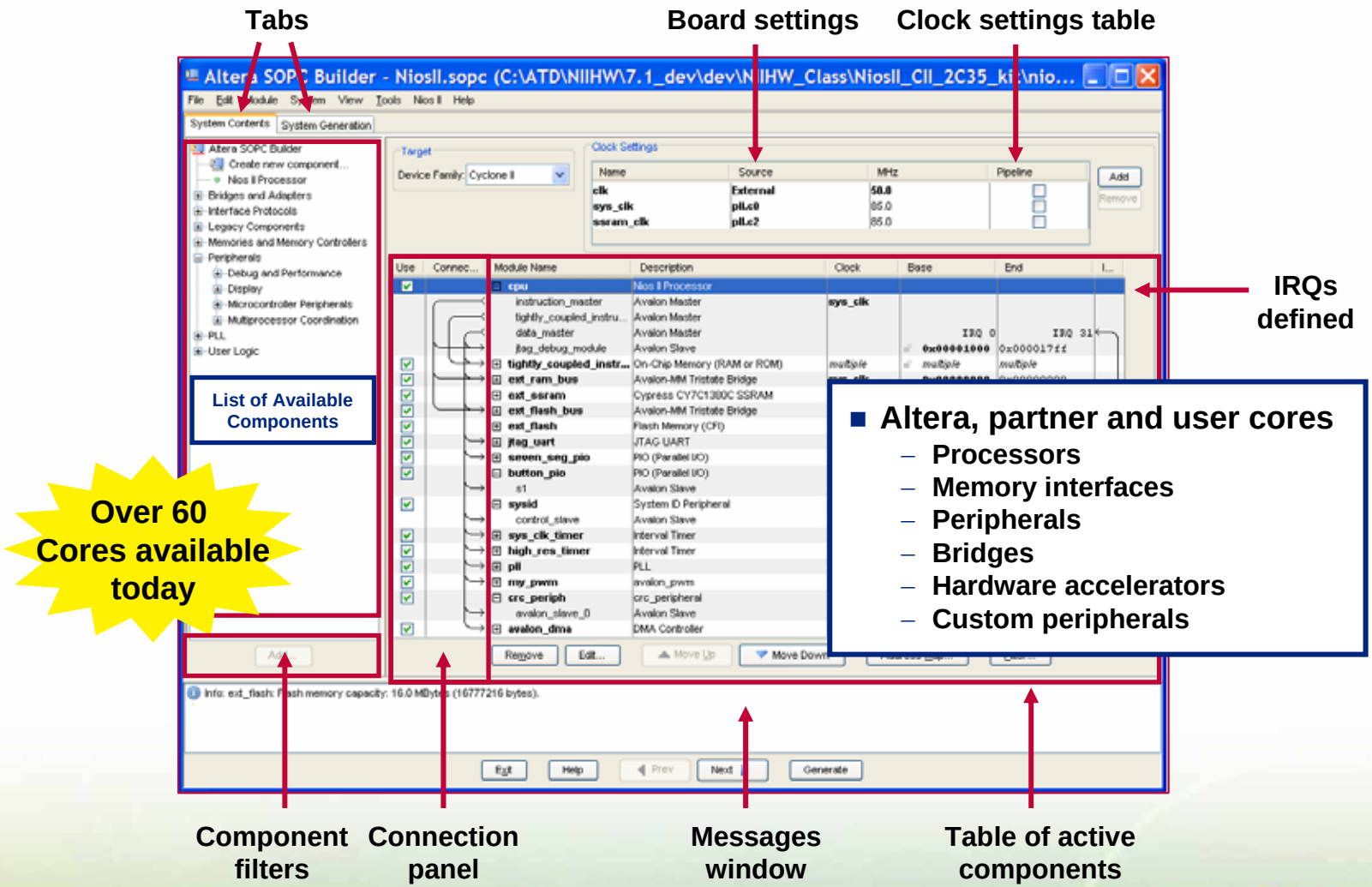
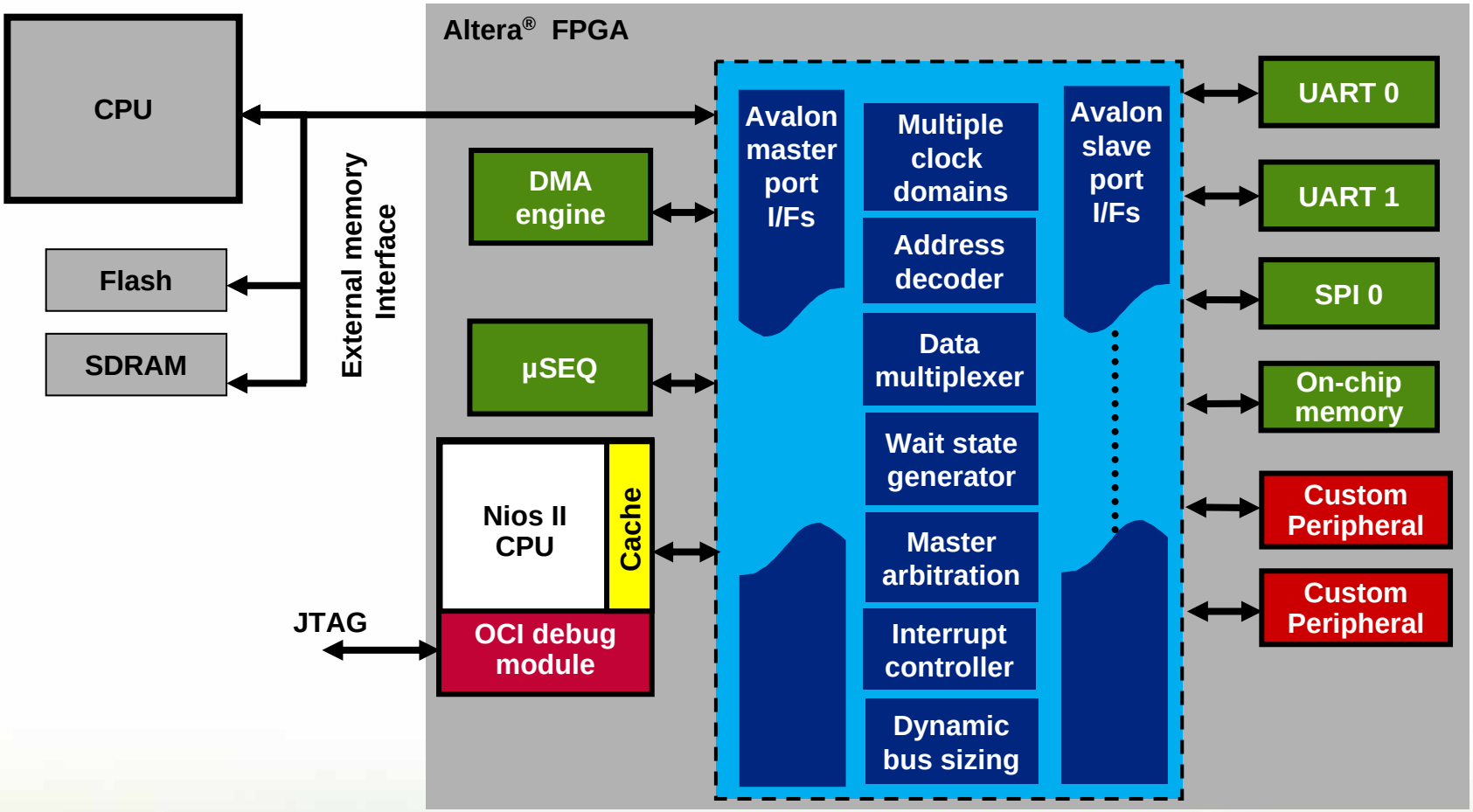
SOPC Builder Tool at a Glance

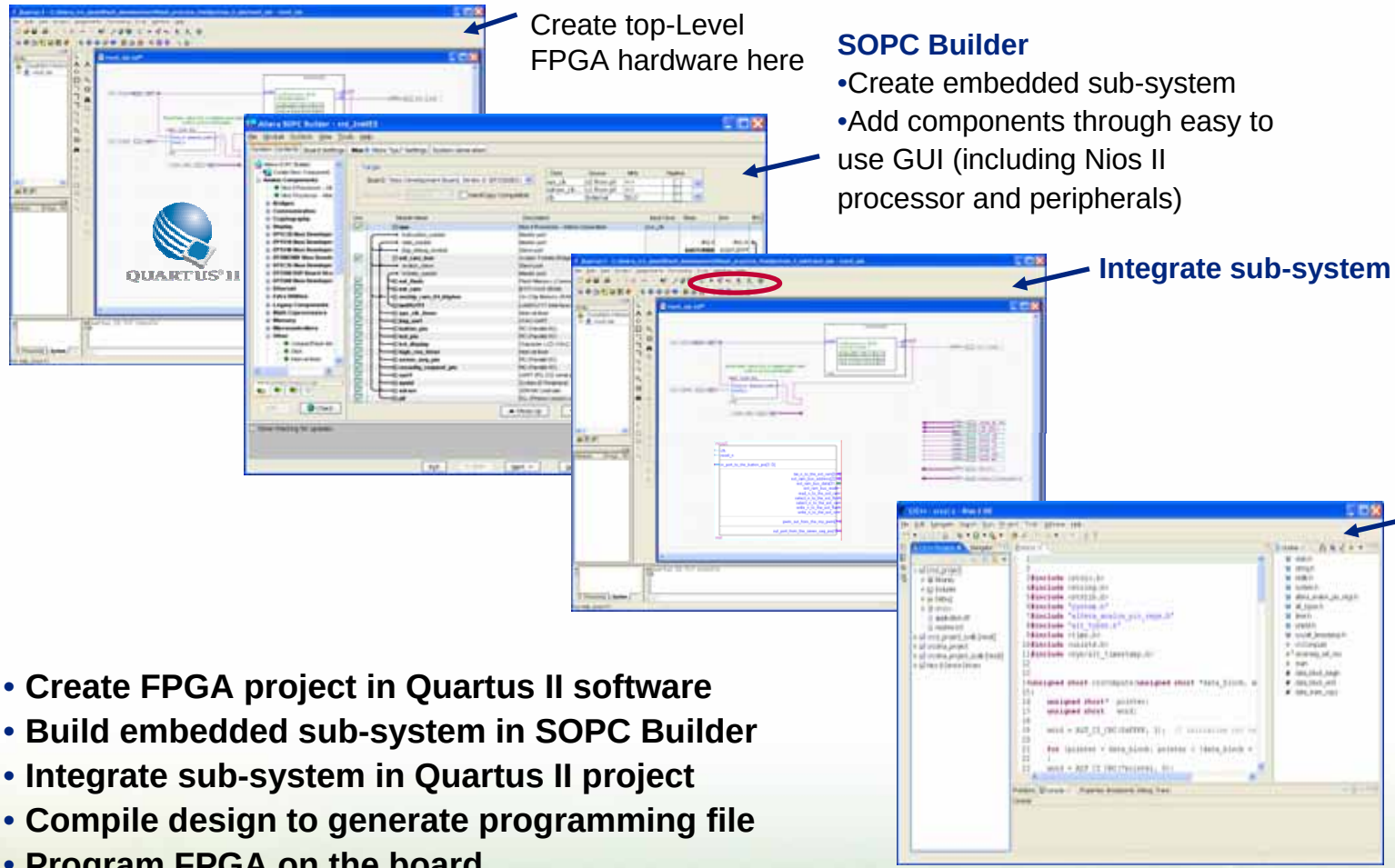


SOPC Builder Generated System



Designer Only Needs to Worry About Peripheral Interface

Design Tool Flow



Quartus II software
Create top-Level FPGA hardware here

SOPC Builder
- Create embedded sub-system
- Add components through easy to use GUI (including Nios II processor and peripherals)

Integrate sub-system

Nios II IDE
- Write software for Nios II micro-processor here

- **Create FPGA project in Quartus II software**
- **Build embedded sub-system in SOPC Builder**
- **Integrate sub-system in Quartus II project**
- **Compile design to generate programming file**
- **Program FPGA on the board**
- **Create software and run on the processor on the FPGA**

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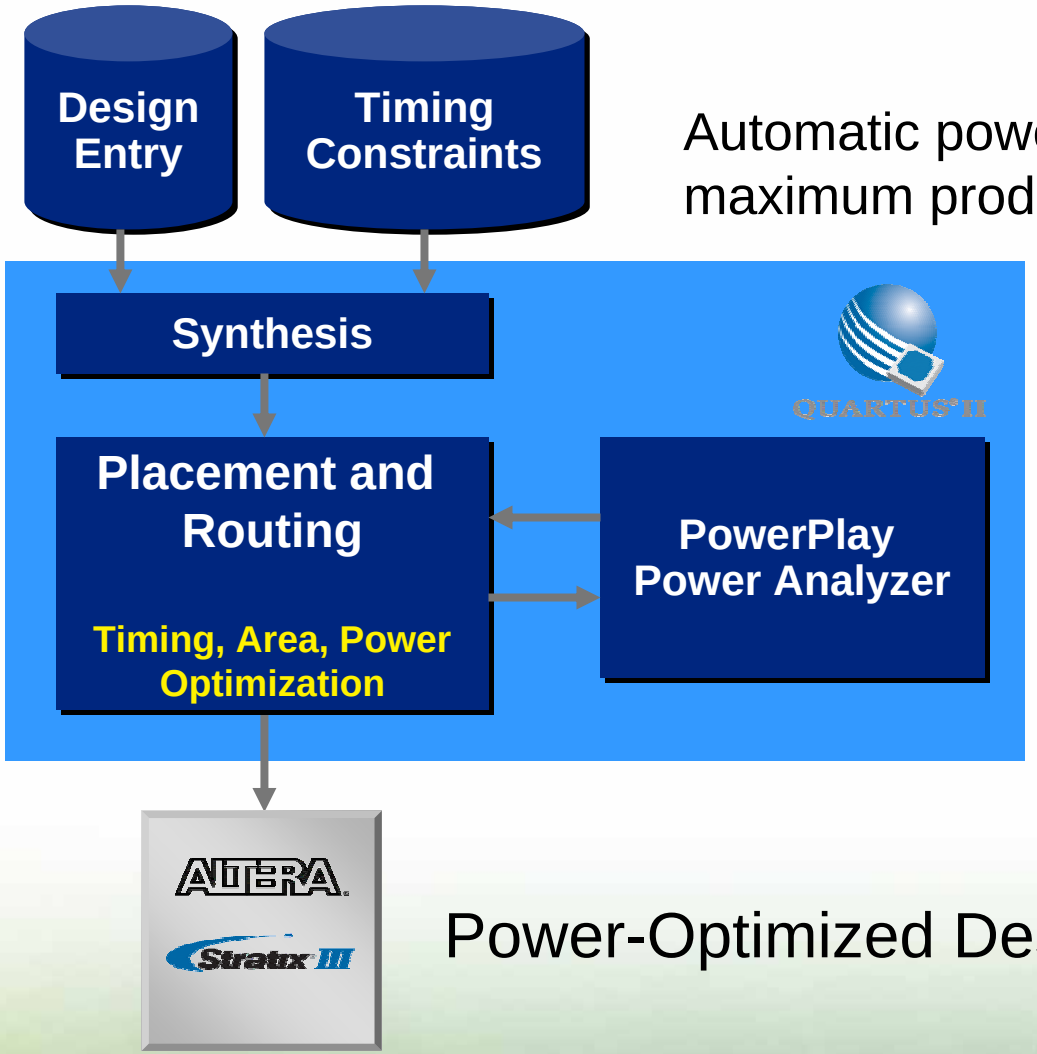
Quartus II Software: PowerPlay



Automatic power reduction for maximum productivity

Timing is always met, then power optimizations are implemented

Power-Optimized Design ☑

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PowerPlay Power Analyzer

- Provides single interface for vectorless and simulation-based power estimation
- Uses improved power models
  - Based on HSPICE and silicon correlation
- Executing power analysis
  - Processing menu ⇒ Start ⇒ Start PowerPlay Power Analyzer
  - Scripting

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Three Parts to Good Power Estimates

1. Accurate toggle rate data on each signal
2. Accurate power models of device circuitry
3. Knowledge of device operating conditions

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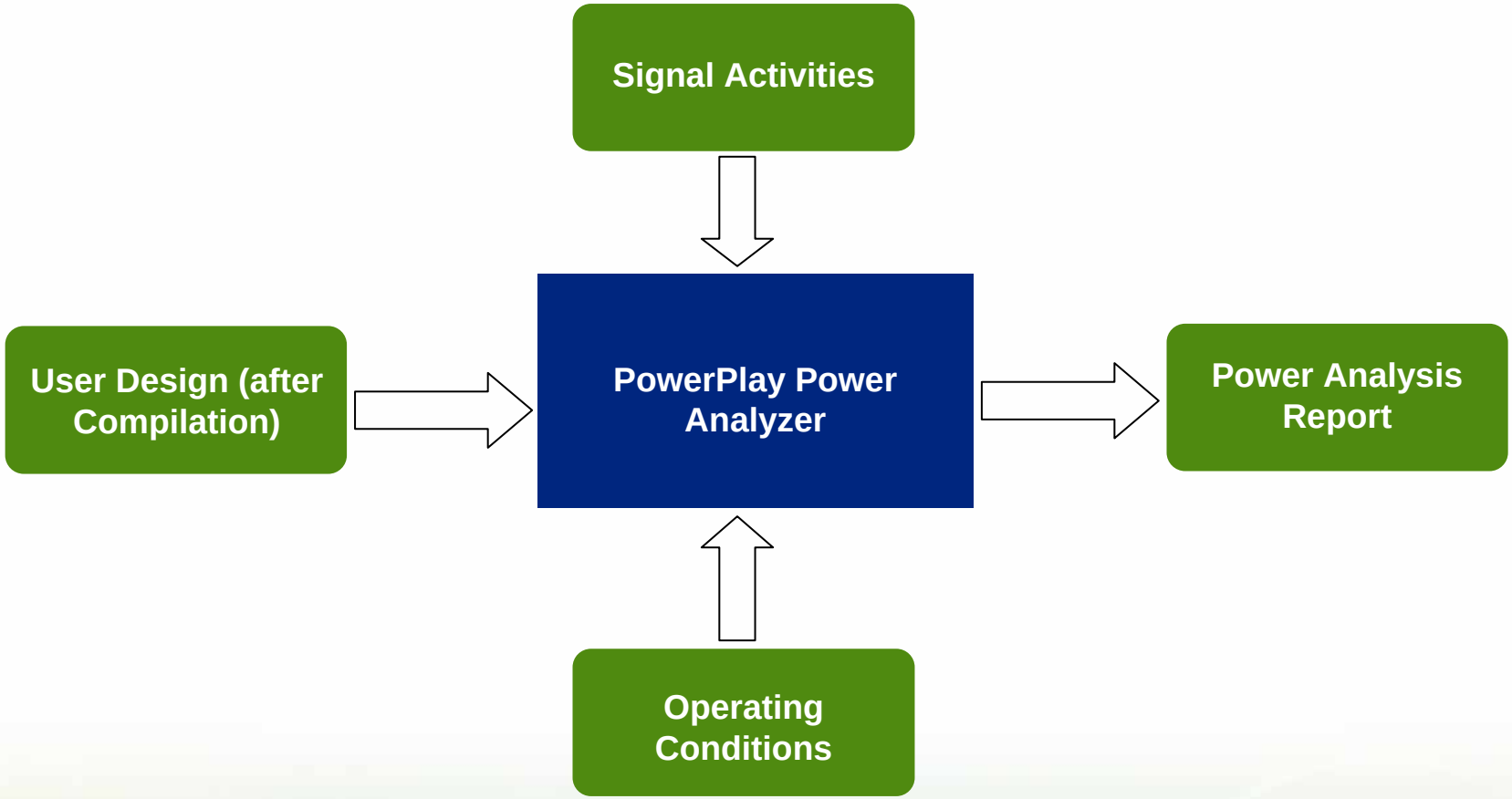
PowerPlay Power Analyzer



PowerPlay Power Inputs

- Signal activity file (.SAF)
  - ASCII text file generated by Quartus II software
- VCD
  - Generated by Quartus II software and 3rd-party simulators
- "Power Toggle Rate" and "Power Static Probability" assignments
  - Use Assignment Editor or Tcl file
  - Apply to specific entities/nodes
- Default toggle rate (12.5%)
  - Percentage of clock periods in which signal transitions
  - May also express as an absolute number of transitions per second

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Other Input Data Used

- Operating conditions
- Clock timing assignments
  - Used to calculate internal signal activities
- Vectorless estimation
  - PowerPlay automatically derives signal activity for a node
  - Based on activity rates of signals feeding a node and functionality
  - Requires input signal activity data
- Capacitive loading
- Termination
- I/O standard

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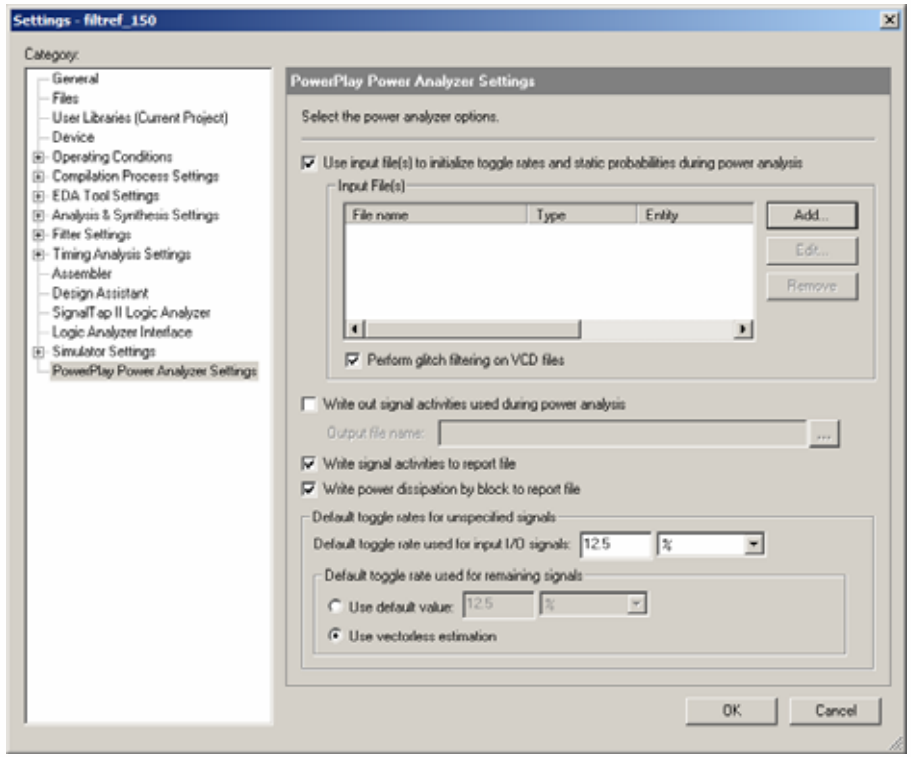
PowerPlay Power Analyzer Settings

- Enter single or multiple SAF/VCD files
  - Allows simulation of subdesigns separately
  - Enable glitch filtering to increase accuracy
    - Also recommend enabling glitch filtering during simulation
- Enter default toggle rates for inputs
- Enter toggle rate for rest of design
- Enable/disable vectorless estimation

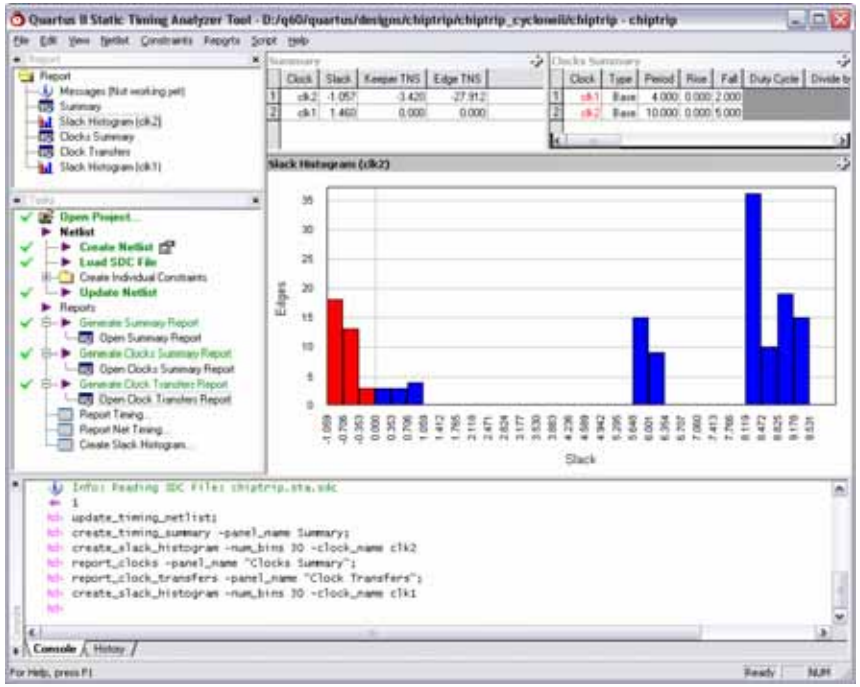


Faster TimeQuest Timing Analyzer

- Improves productivity with faster timing closure
  - Improved compile times
  - Reduced memory usage
  - Improved timing constraint conversion from Altera's classic timing analyzer to Synopsys design constraint (SDC)

TimeQuest Timing Analyzer

- Timing analysis
  - New, easy-to-use timing analyzer
  - Complete GUI environment for creating timing constraints and reports
  - Native support for SDC (Synopsis Design Constraints)



Only 65-nm FPGA Vendor with Native SDC Support

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Top 5 Reasons to Use TimeQuest

- Easier to use: TimeQuest provides an easier to use GUI and interactive reporting for analyzing timing
- Industry standard: SDC format is an established industry standard
  - Simpler and more concise timing format
- More powerful: SDC allows for faster, easier description and analysis of advanced design constructs
  - DDR (other source sync.), complex clocks
- Designs run faster: TimeQuest more precisely analyzes timing behavior—gain 3-5% performance at 65 nm
- Interoperability: allows for easy migration of SDC constraints for ASIC and HardCopy® designs

Quartus II Reference

- Quartus II handbook
  - www.altera.com/literature/lit-qts.jsp
- Quartus II online demos
  - www.altera.com/quartusdemos
- Quartus II downloads
  - www.altera.com/download
- Technical support
  - www.altera.com/mysupport

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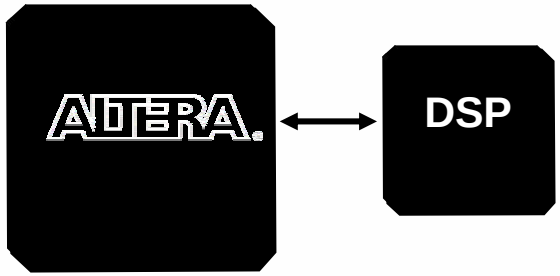
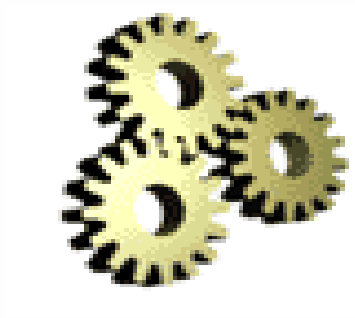
Conclusion

FPGAs, Tools, and DSP–Coprocessing Enhances Performance Together





Stratix Series

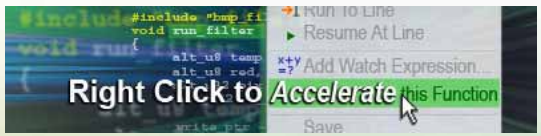
HardCopy Series

Arria Series

Cyclone Series

QUARTUS II

SOPC Builder



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Conclusion

- Embedded and DSP design challenges– productivity, performance, and flexibility
- DSP coprocessing, C2H tools, and new features in Quartus II help tackle those challenges
  - Coprocessing provides unparalleled performance improvement
  - C2H tools provide ability to create performance-enhancing hardware automatically (simply *Right Click to Accelerate*) without leaving the C domain
  - Quartus II SOPC Builder automates block-based design easily and efficiently; Powerplay automates power reduction for maximum productivity; Timequest facilitates timing analysis for 65-nm era and beyond

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Thank You!