Model-Based Design for Video/Image Processing Applications

The MathWorks

© 2007 Altera Corporation—**Public**

Agenda

- Model-Based Design
- From MATLAB and Simulink to Altera FPGA
  - Step-by-step design and implementation of edge detection algorithm
  - NTSC-to-HD video converter design
- Roadmap for Model-Based Design and next steps

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

The MathWorks Mission

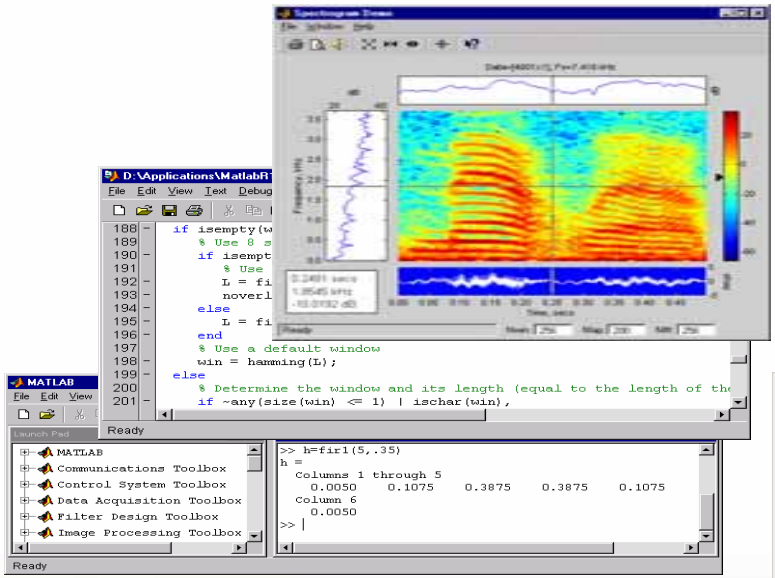
Accelerating the Pace of Engineering and Science

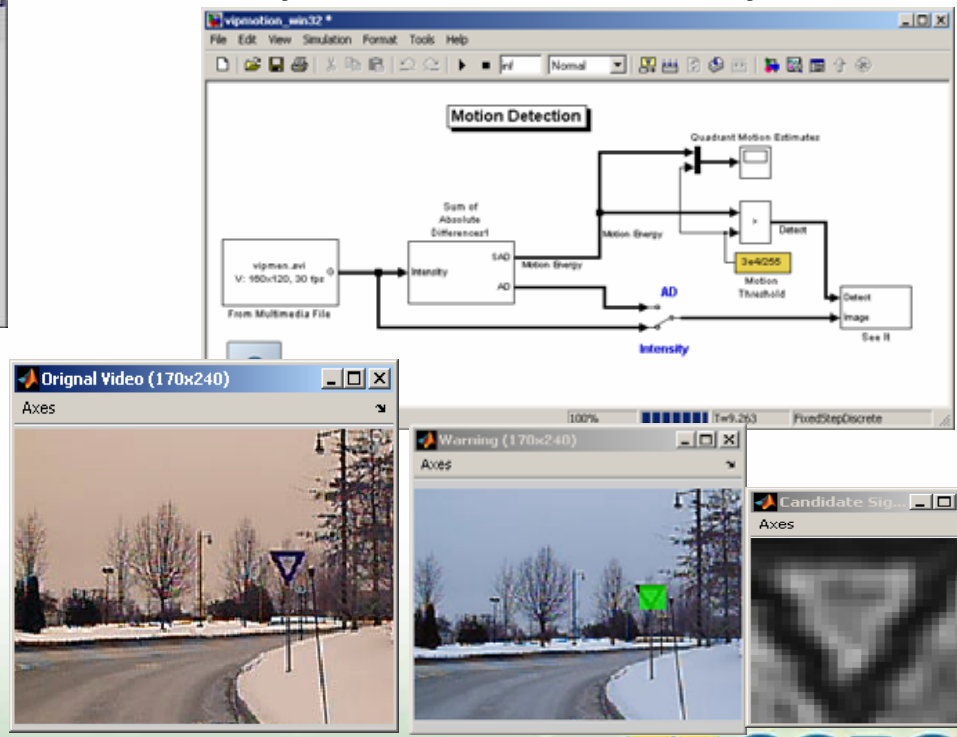
MATLAB®

The leading environment for technical computing

SIMULINK®

The leading environment for modeling, simulating, and implementing dynamic and embedded systems





© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

The MathWorks

IDT-Newave Reduces Semiconductor Design Time by Months

Realtek Cuts Development Time by 50%, Takes the Lead in New-Generation High Definition Audio (HDA) CODECs

SOPC WORLD

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Session Goal:

Solutions to Address Today's Design Challenges

- Breaks in conventional design flows
- Verification of complex FPGA designs

- Solution - Model-Based Design
  - Integrated environment for simulation, implementation, testing, and verification of complex systems
  - Path to implementation on FPGA devices and digital signal processing (DSP) processors

Deliver better products in less time

SOPC WORLD

© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Agenda

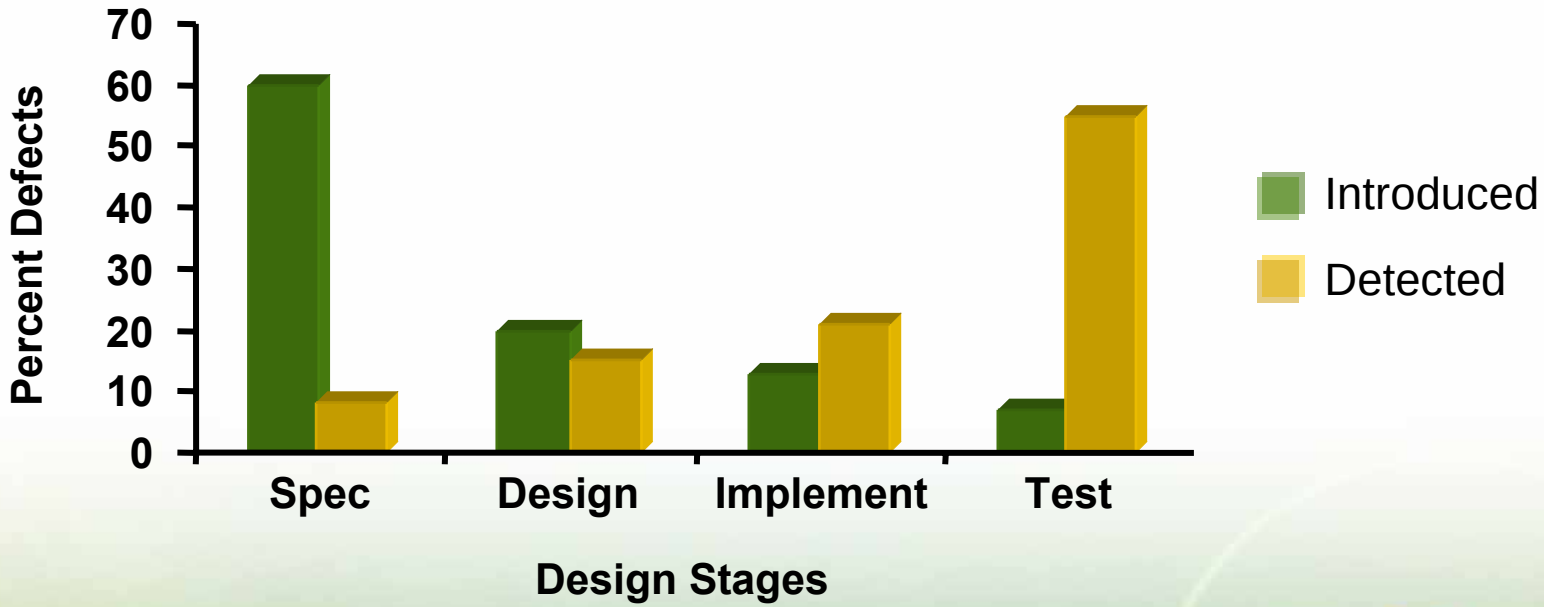
- Model-Based Design
- From MATLAB and Simulink to Altera FPGA
  - Step-by-step design and implementation of edge detection algorithm
  - NTSC-to-HD video converter design
- Roadmap for Model-Based Design and next steps

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Design Failure and Time-to-Market in Embedded Systems

- Survey of ~1000 developers across multiple industries:
  - 54% of projects behind schedule
  - < 1/3 were within 10% of intended performance/feature requirements
  - >30% failed to meet 50% of performance/feature requirements



Source: Embedded Market Forecasters, July 2003

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

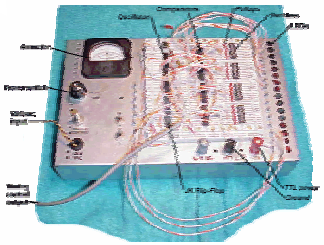
SOPC WORLD

Problems with Traditional Workflows

Requirements / Specifications

Text documents prevents rapid iteration

Design



Physical prototypes incomplete, expensive

Implementation

Manual implementation separate tools & human error

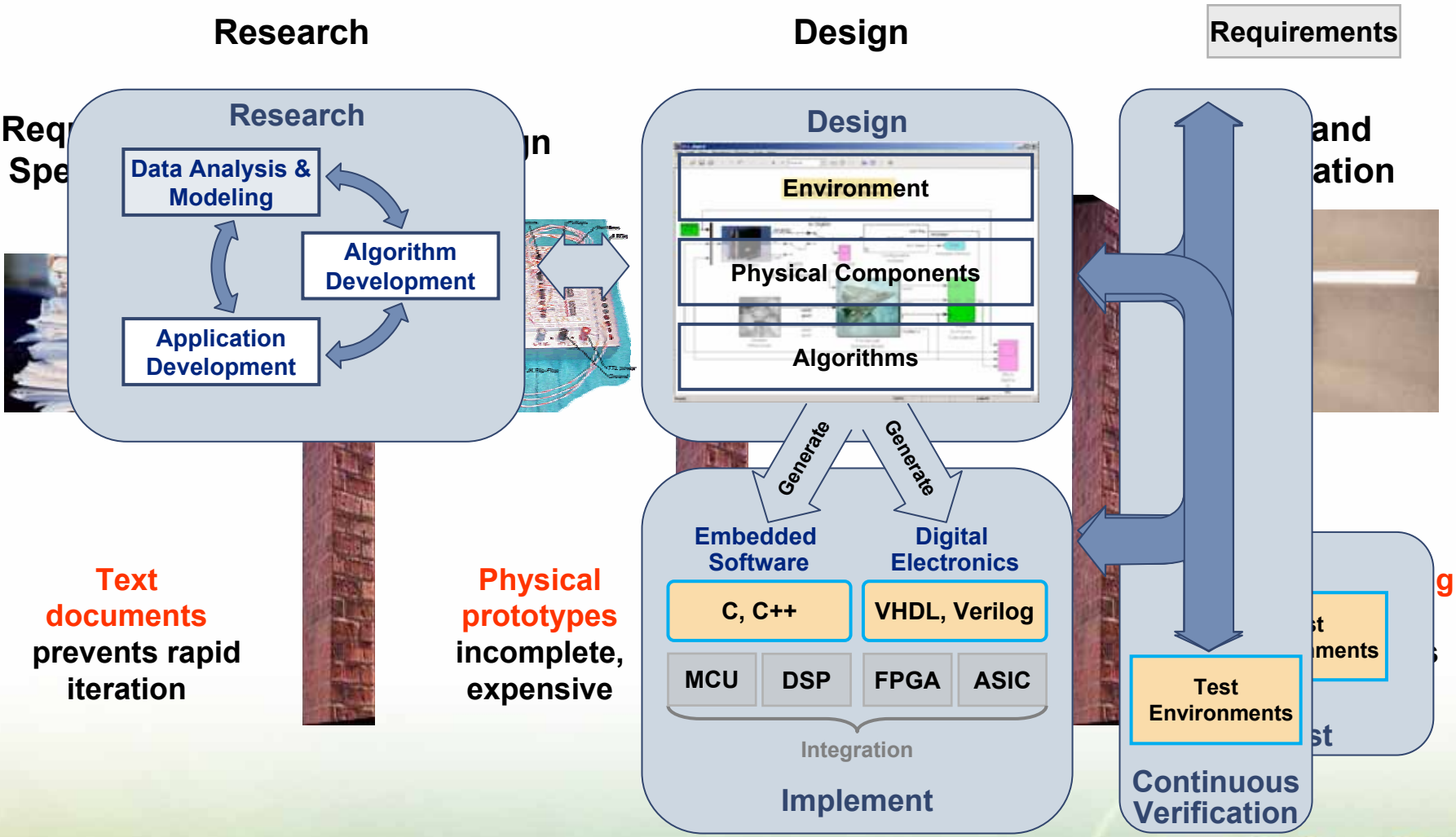
Test and Verification

Traditional testing errors found late in process

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Model-Based Design Workflow

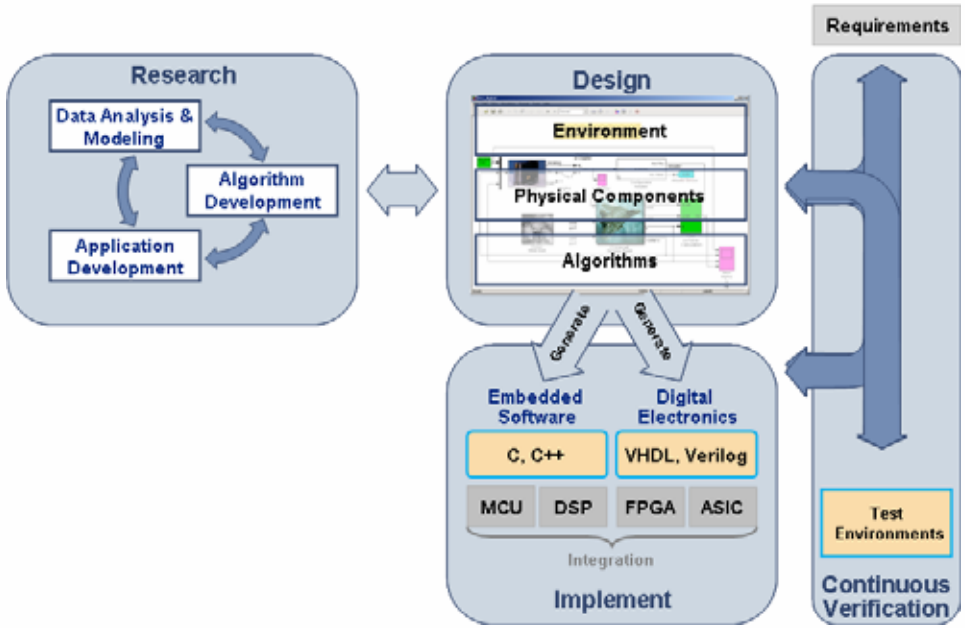


© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

The Benefits of Model-Based Design

- Characteristics
  - Behavioral system modeling immediately
  - Fixed-point modeling for hardware equivalency
  - Automatic HDL code generation
  - HDL and system model co-simulation
- Benefits
  - Validate design specification
  - Rapid design iteration
  - Accelerated time-to-first HDL
  - Verify the implementation to a complete and valid specification.

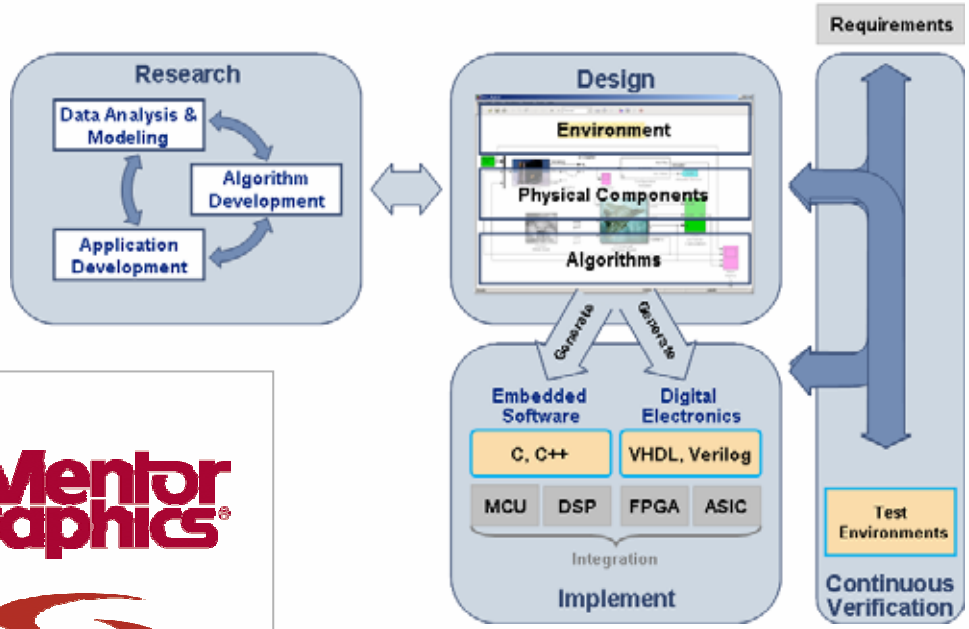


© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Industry Partners for Model-Based Design



Powered By

ALTERA.

Mentor Graphics

cadence

Synplicity

The MathWorks

Texas Instruments

SOPC WORLD

© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Agenda

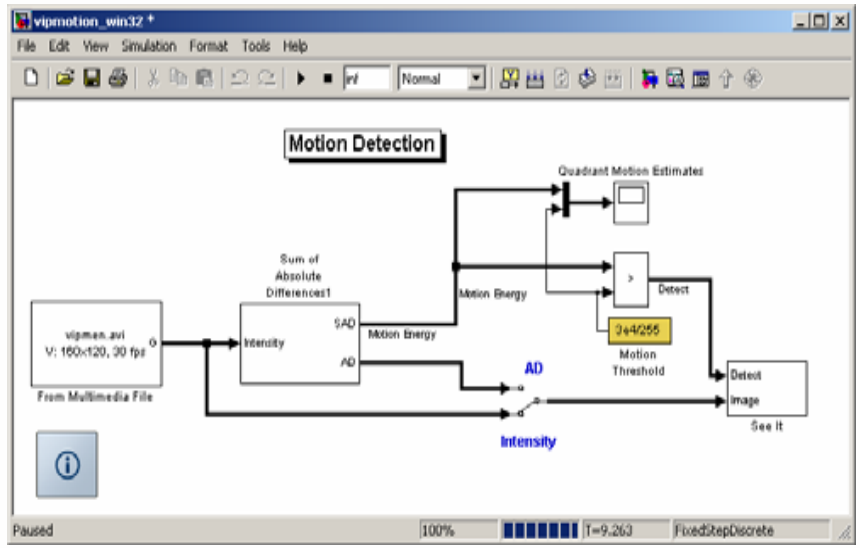
- Model-Based Design
- From MATLAB and Simulink to Altera FPGA
  - Step-by-step design and implementation of edge detection algorithm
  - NTSC-to-HD video converter design
- Roadmap for Model-Based Design and next steps

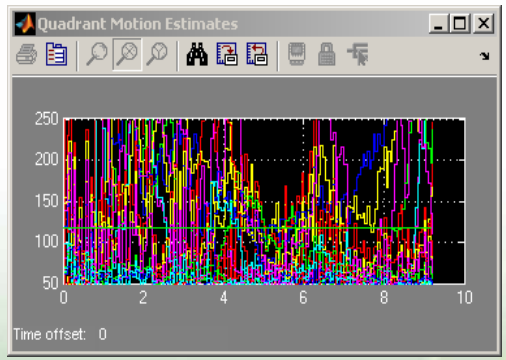
© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

What is Simulink?

- Simulation, modeling, and design environment
- Key features
  - Hierarchical, component-based modeling
  - MATLAB® integration
  - Extensive library of predefined blocks
  - Application-specific libraries
  - Open Application Program Interface (API)



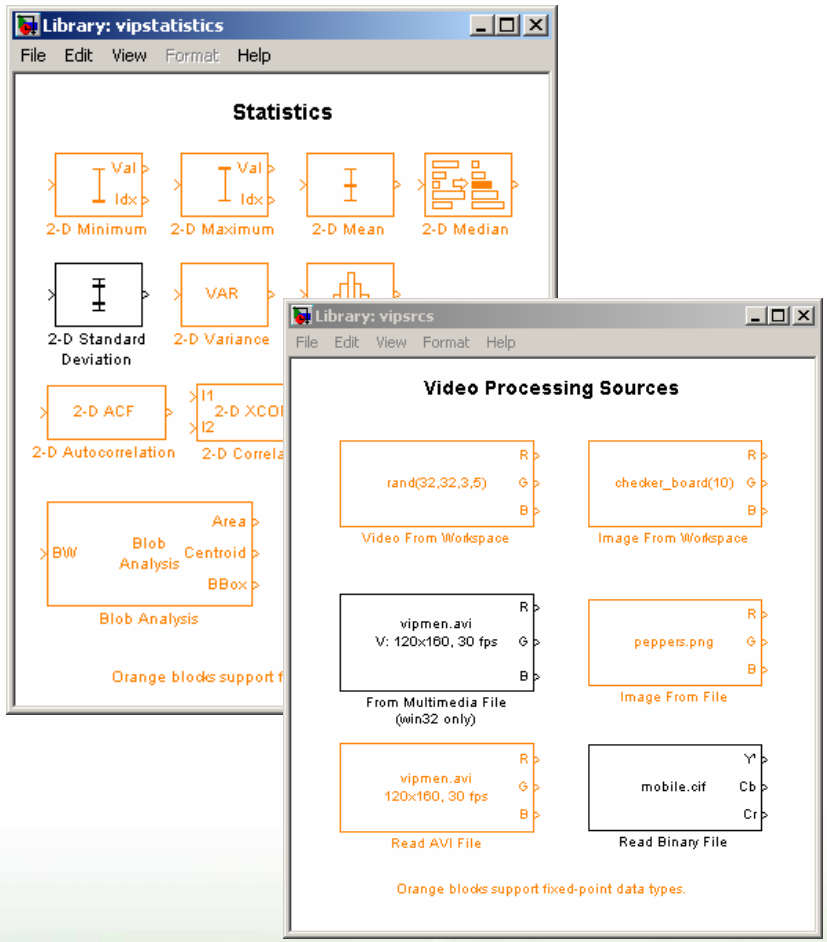


© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Simulink Libraries and Blocksets

Example: Video and Image Processing Blockset

- Analysis and enhancement
- Conversions
- Filtering
- Geometric transforms
- Morphological operations
- Sinks
- Sources – video inputs
- Statistics
- Text and graphics
- Transforms
- Utilities



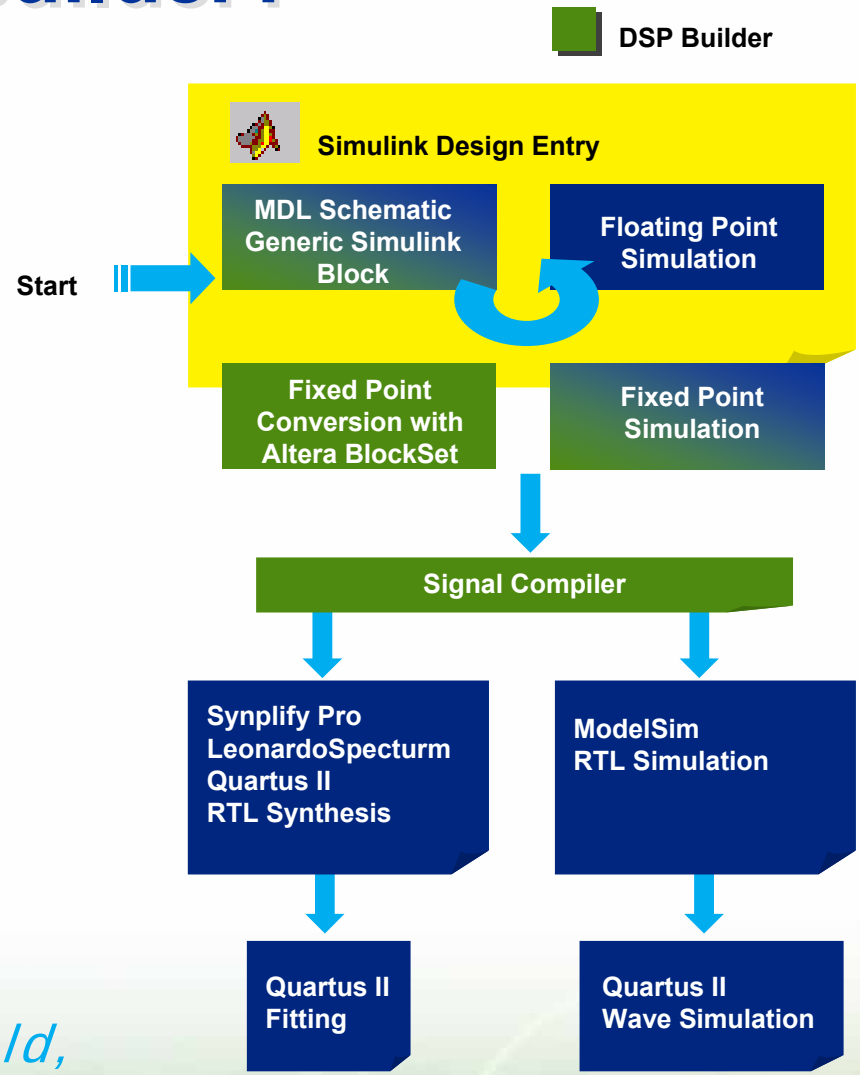
© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

What is Altera DSP Builder?

- Altera's interface between Quartus® II design software and MATLAB/Simulink
- Altera blockset
  - Library of optimized fixed-point Simulink functions
- Altera DSP IP
  - Open Core
- Signal compiler utility
  - Converts between Simulink and Altera domain
- Hardware Debug
  - Hardware-in-the-Loop/ SignalTap® II

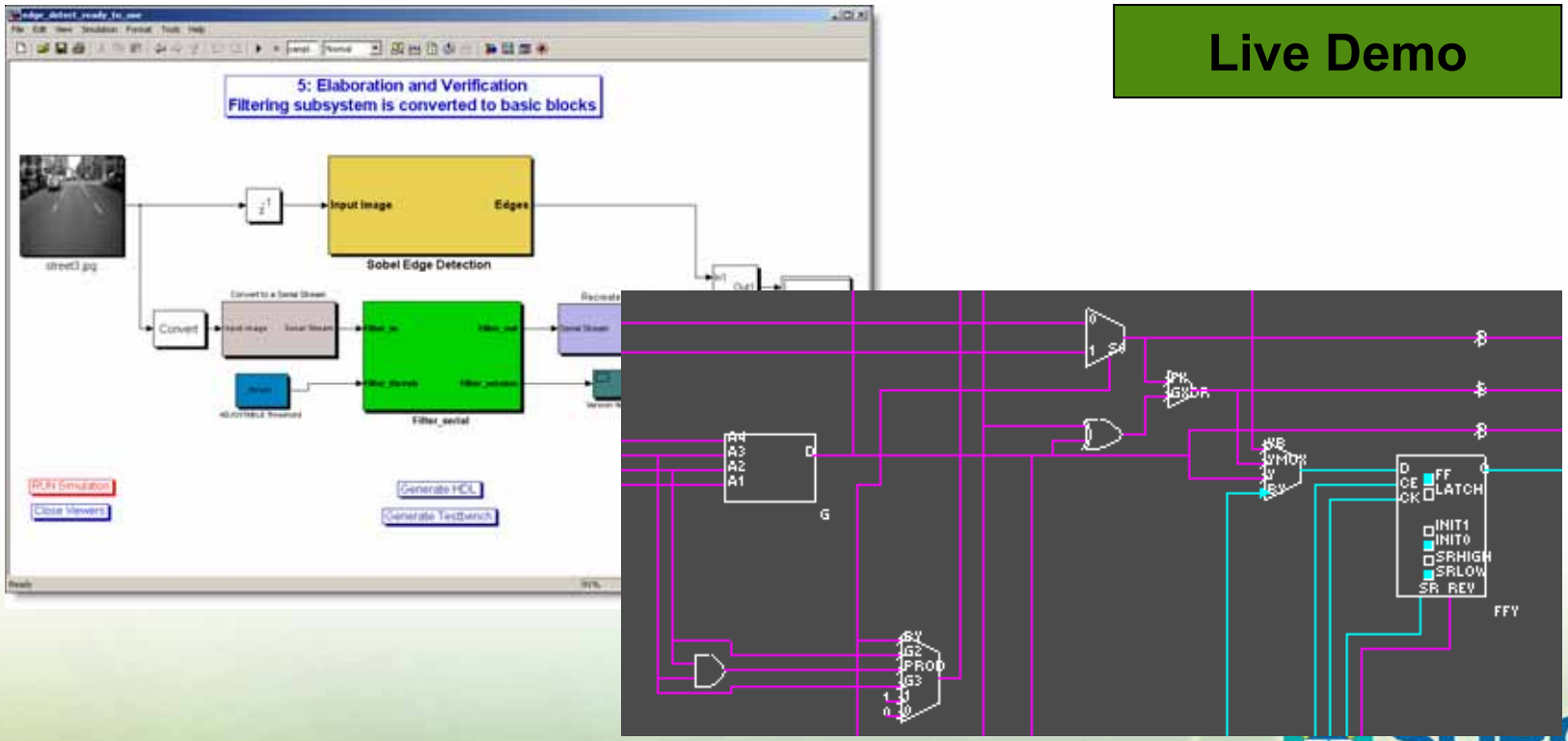


DSP Builder is Developed, Sold, and Supported by Altera

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Case Study

- Implementing Sobel Edge Detection Algorithm on an Altera FPGA



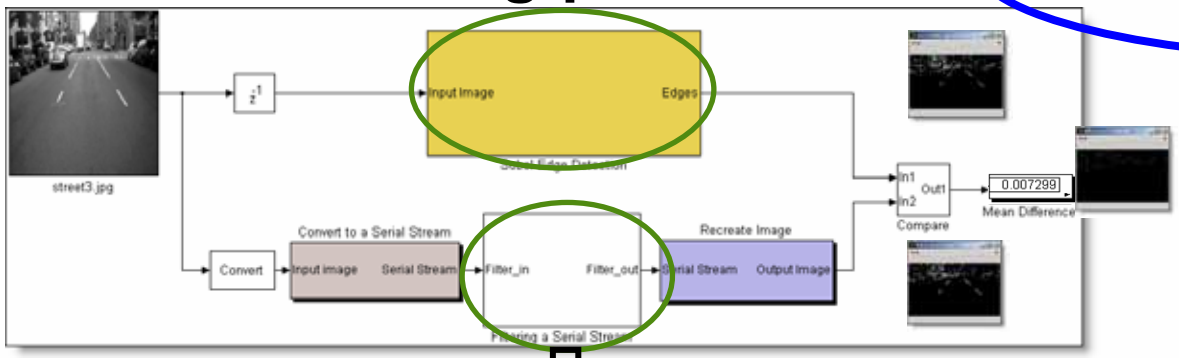
Live Demo

© 2007 Altera Corporation—**Public**

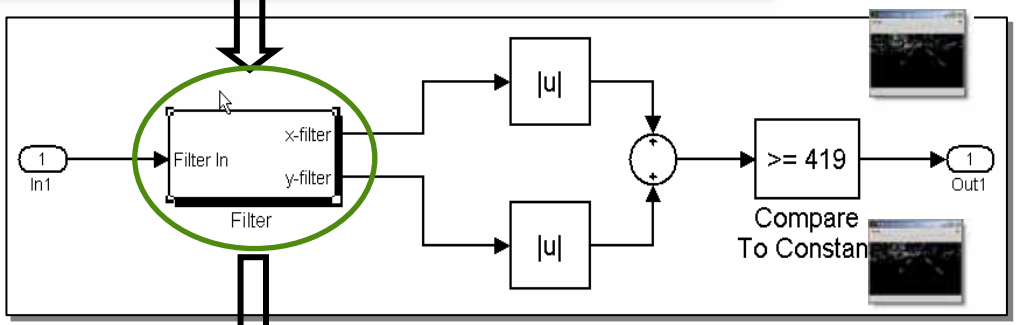
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Edge Detection Case Study

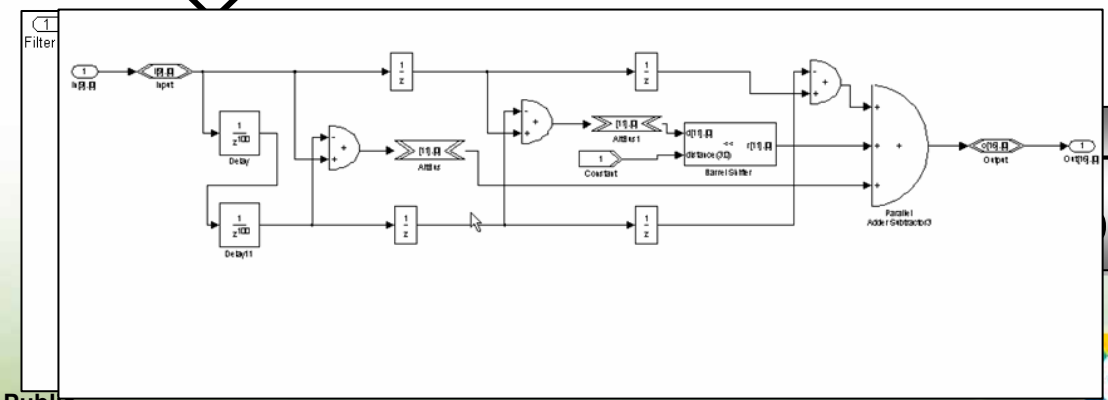
Floating-point model ≡ Fixed-point model = HDL



Floating-point model



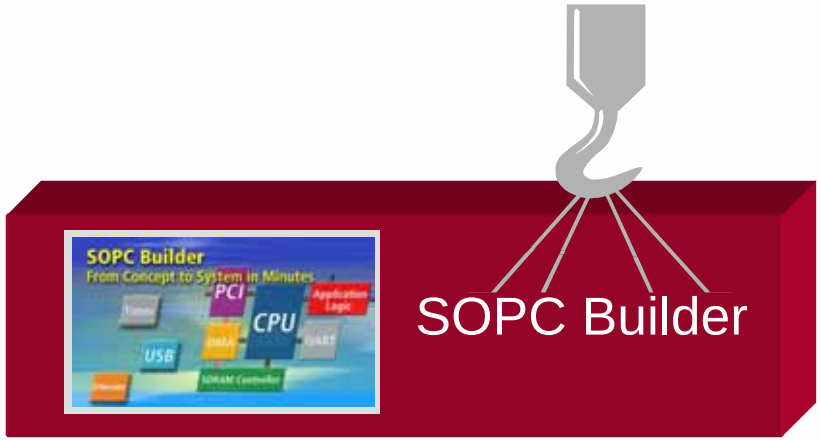
Fixed-point model



Fixed-point DSP Builder

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Completing Design Flow from Simulink to Altera FPGAs



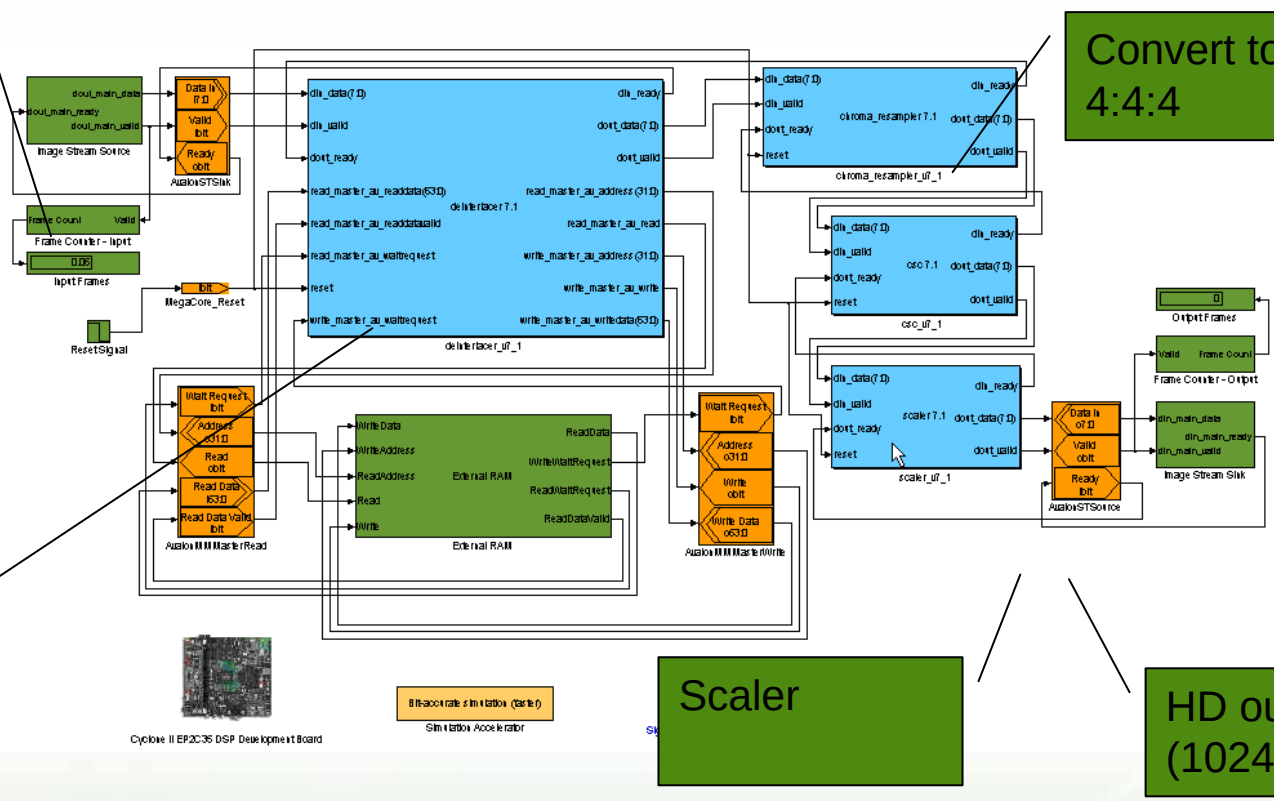
DSP System Development

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Additional Demo at The MathWorks Exhibit: NTSC Video to HD Converter

NTSC interlaced video input (640 × 480)



Convert to 4:4:4

Deinterlacer

Scaler

HD output (1024 × 768)

© 2007 Altera Corporation—**Public**

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

Agenda

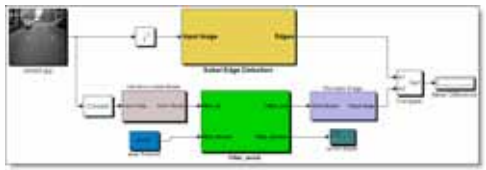
- Model-Based Design
- From MATLAB and Simulink to Altera FPGA
  - Step-by-step design and implementation of edge detection algorithm
  - NTSC-to-HD video converter design
- Roadmap for Model-Based Design and next steps

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Simulink HDL Coder for Automatic HDL Code Generation

- Simulink HDL Coder generates 'correct-by-construction' HDL
  - Matches fixed-point system model
  - Reduces verification burden
    - Produces testbench in minutes
    - Stimulus Response auto-capture
  - Pre- & self-documenting
- The MathWorks and Altera working to support import of HDL from Simulink HDL Coder into DSP Builder



SOPC WORLD

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

In Summary

- Model-Based Design enables faster design times and increased quality
- Simulink for Model-Based Design
  - Single environment to simulate, implement, test, and verify complex video systems
- The Altera / MathWorks partnership
  - Providing Model-Based Design from design capture to hardware implementation
  - Altera DSP Builder provides rapid compilation of designs to Altera semiconductor devices
  - Tighter integration underway between DSP Builder and Simulink HDL Coder

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Next Steps

- Visit the MathWorks booth and talk to our engineers
  - Check out designs and demos
  - Ask for a trial, or schedule a meeting for your company

Thank You!

© 2007 Altera Corporation—**Public**
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation

SOPC WORLD

Thank You!

© 2007 Altera Corporation—**Public**