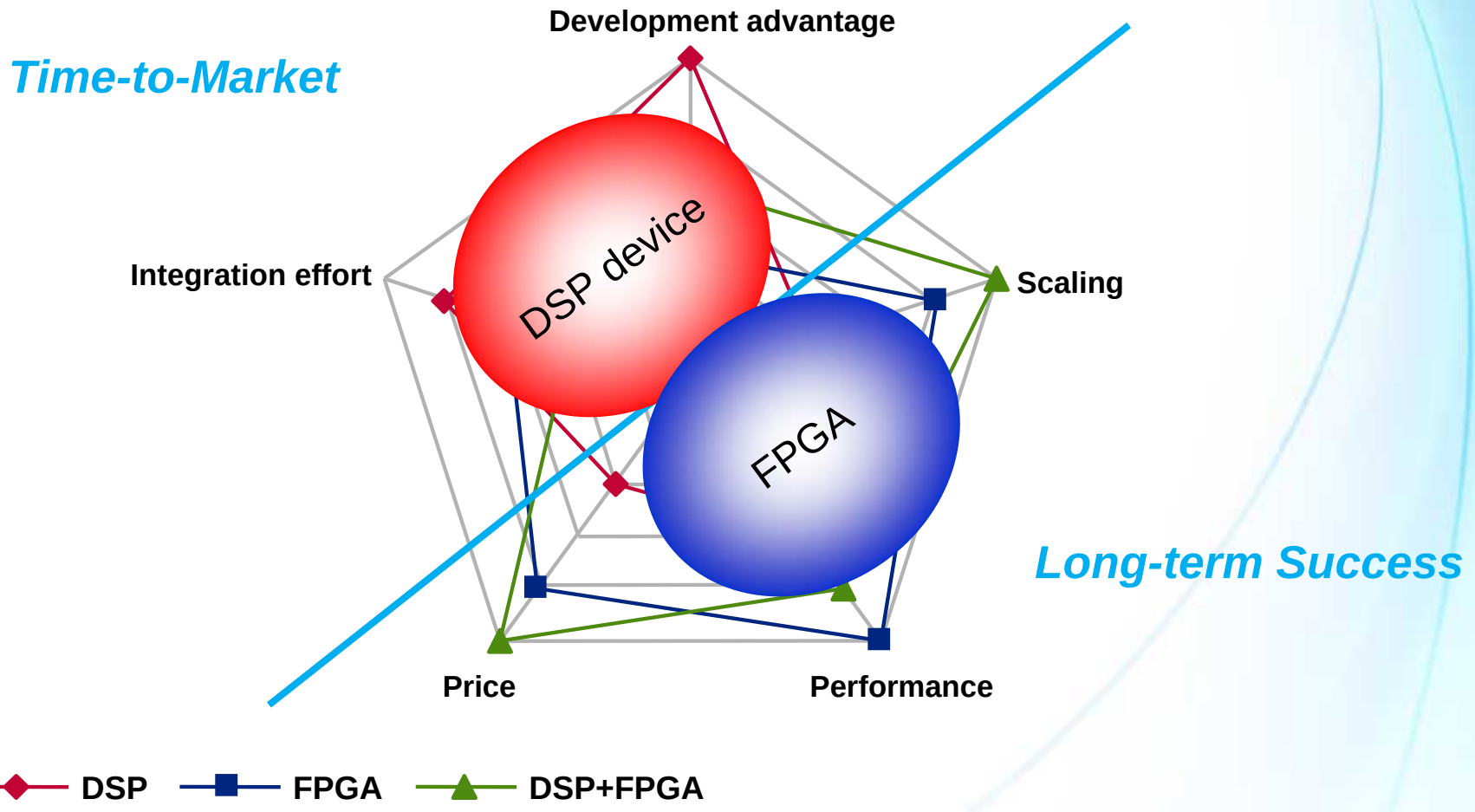
Trends in DSP Technology

Agenda

- General digital signal processing (DSP) challenges and trends
- Why “DSP in FPGA?”
  - Performance
  - Price
  - Power
  - Scalability
  - Other advantages
- Implementation example
- Conclusion

CY7

General DSP Challenges and FPGA Benefits



Slide 3

CY7 This meaning behind this graphic takes a while to grasp

Christine Young, 6/1/2007

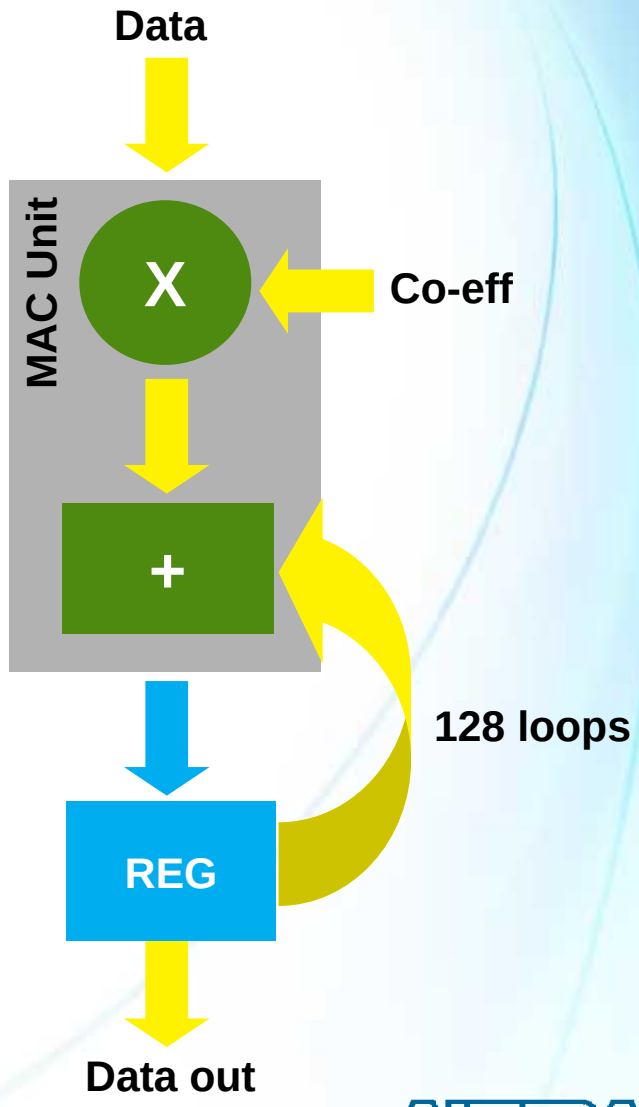
Why “DSP in FPGA?”

Why “DSP in FPGA”?

- Performance
  - Real-time video processing
  - H.264 encoding
  - Forward error correction (FEC) in the baseband
  - Intermediate frequency (IF) processing
  - Multi-channel signal processing
- Price – Multiple DSP devices vs. FPGAs
- Power – Multiple DSP devices vs. FPGAs
- Scalability – to move to larger or smaller devices with the same footprint
- Other reasons that can include
  - FPGA familiarity
  - Consolidation of the DSP device + FPGAs → FPGAs
  - High-end DSP device → Low-cost DSP device + low-cost FPGAs

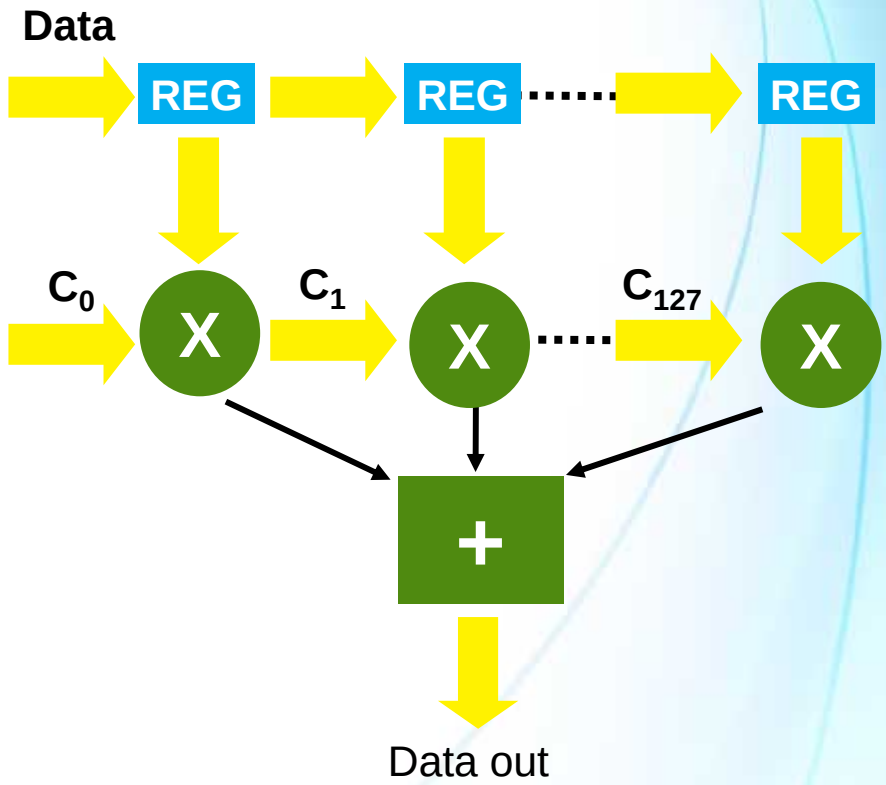
Conventional DSP Performance

- Fundamental unit of computation in a DSP device; multiplier-accumulator (MAC)
- For a typical 128-tap finite impulse response (FIR) filter
  - Conventional DSP processor with a single MAC unit would need 128 loops to process the data



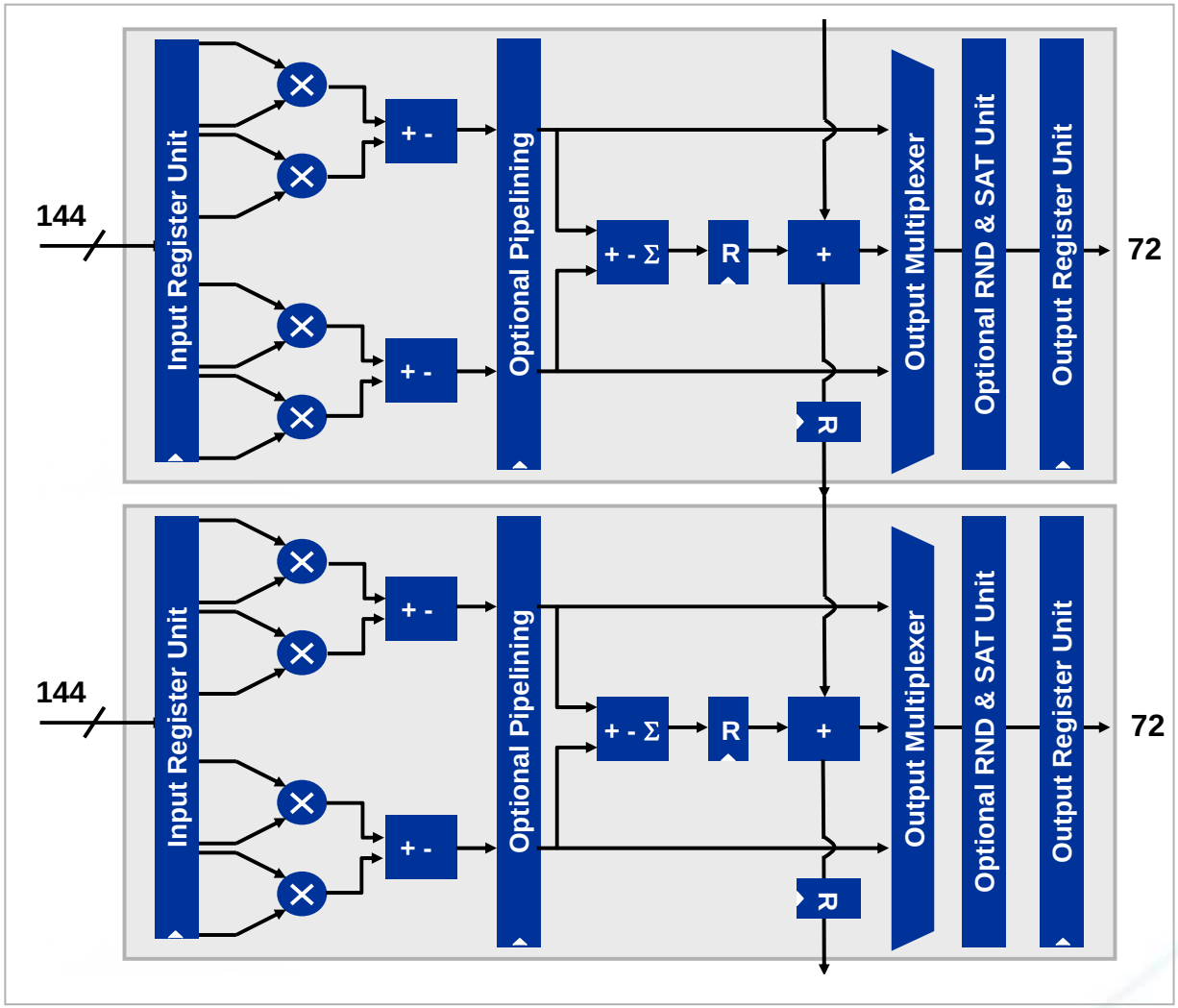
FPGA DSP Performance

- FPGAs have significant logic, memory, and multiplier resources
- These can be used in a parallel manner to implement very high-performance DSP capabilities
- In this example, the 128-tap FIR filter can be implemented in a single loop by using
  - 128 multipliers
  - 128 registers
  - And a single adder



For a 128-tap FIR Filter, Fully Parallel FPGA Implementation

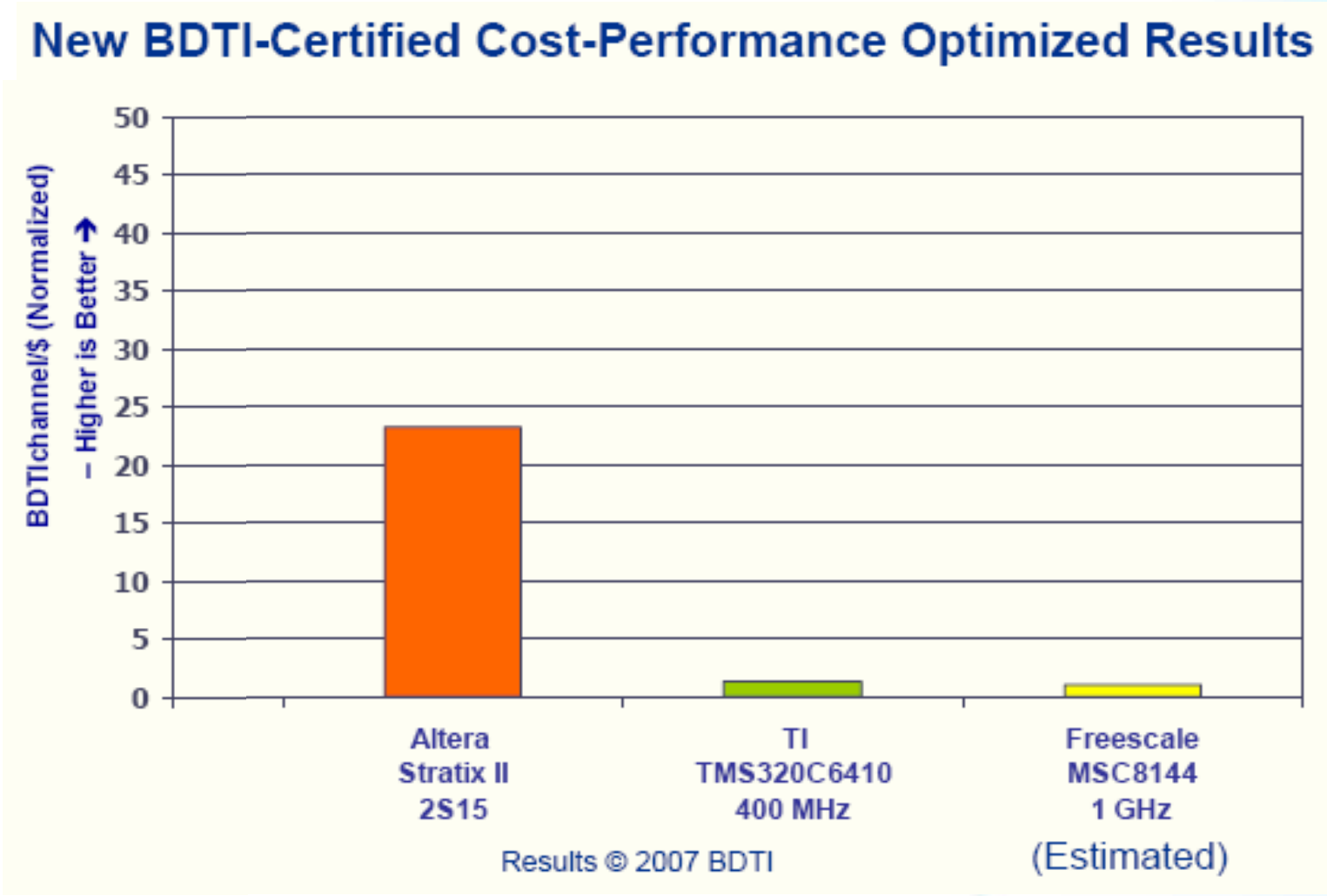
High-Performance DSP Blocks



- Basic multiplier modes
  - 8 x (9x9)
  - 6 x (12x12)
  - 4 x (18x18)
  - 2 x (36x36)
  - 2 x complex (18x18)
- Sum modes
  - 4 x sum of two (18x18)
  - 2 x sum of four (18x18)
- Accumulation
  - 2 x Acc

CY3 CY2

Cost Benchmarks – 2006 BDTI



Slide 9

CY2 Can we remove "optimized" from the graphic title? What does it mean here?
Christine Young, 6/1/2007

CY3 I can't edit this graphic, but trademarks need to be added:

Add a registered trademark at Altera and also at Stratix

Also, the Stratix device part number needs to be fully spelled out, ie: EP2S15
Christine Young, 6/1/2007

Performance → Price and Power Advantage

EP2S180
~172 GMACS
(*Counting ONLY the embedded mults*)

Multiple C6455 DSP devices
(8 GMACS each)

Commentary on Power Consumption

- FPGAs have long been viewed as too power-hungry for most DSP applications – this is an obsolete perspective
- What matters is not the absolute power consumed, but the power consumed per function/channel
- Since FPGAs can process multiple channels (using time division multiplexing)
  - The real comparison is between one FPGA and a bank of DSP devices or
  - Between power/channel

CY4

Commentary on Power Consumption

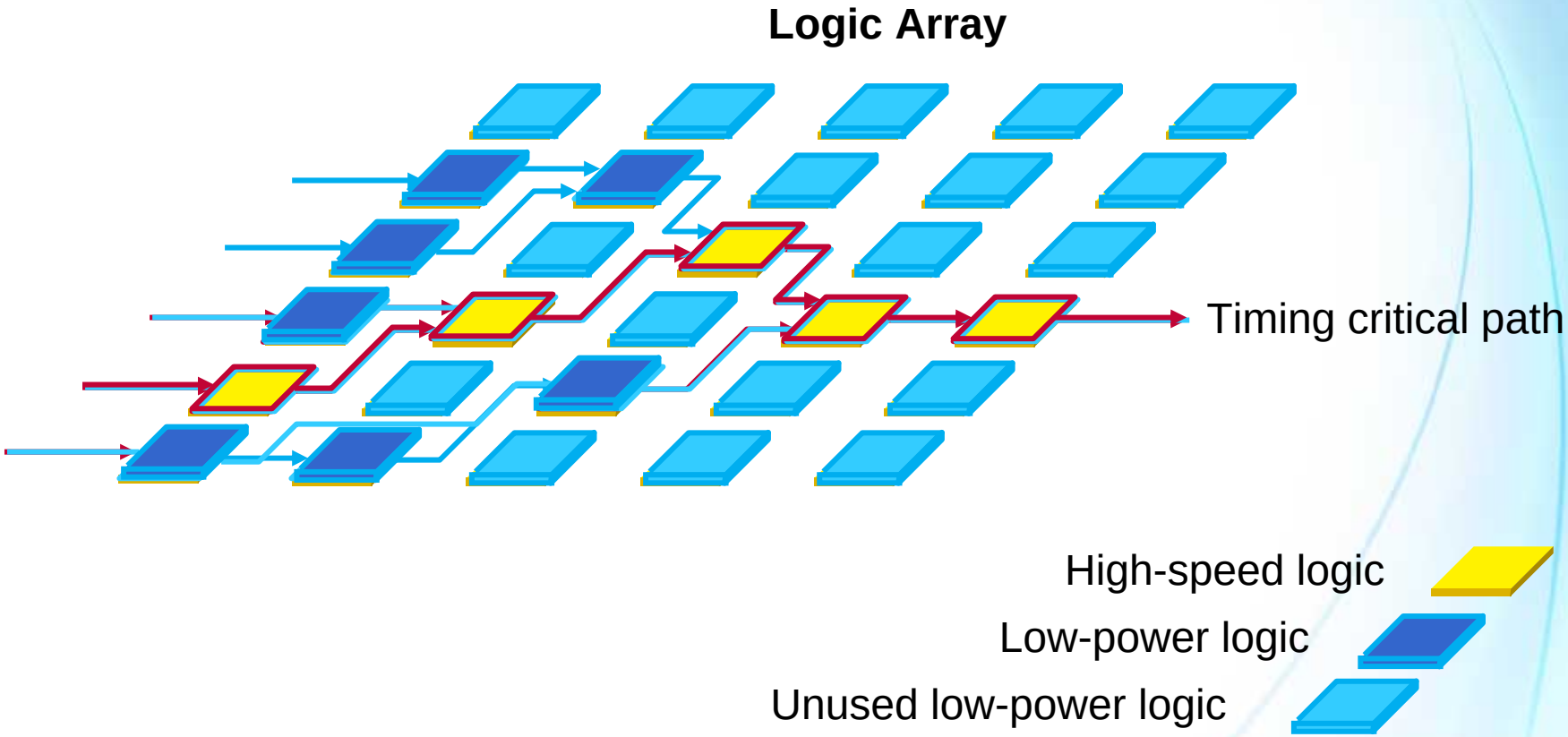
- BDTI did its own "back of the envelope" comparisons of the energy efficiency of FPGAs and DSPs
- BDTI estimated that high-end FPGAs implementing demanding DSP applications, such as that embodied in the BDTI Communications Benchmark (OFDM), consume on the order of 10 watts
- High-end DSP devices consume roughly 2-3 watts
- However, benchmark results show that high-end FPGAs can support roughly 10 to 100 times more channels on this benchmark than high-end DSP devices
- Power consumed/channel
  - FPGA 1 to 0.1 W/channel
  - DSP 2-3 W/channel

Slide 12

CY4 Very text-heavy slide. Suggest discussing some of these points during the presentation (include in speakers notes instead of on the slide)...for example, the 1st bullet can be moved to speakers notes. Other bullets can be condensed

Christine Young, 6/1/2007

Stratix III Programmable Power Technology



Performance Where You Need It, Lowest Power Everywhere Else, Automated by Quartus® II Software

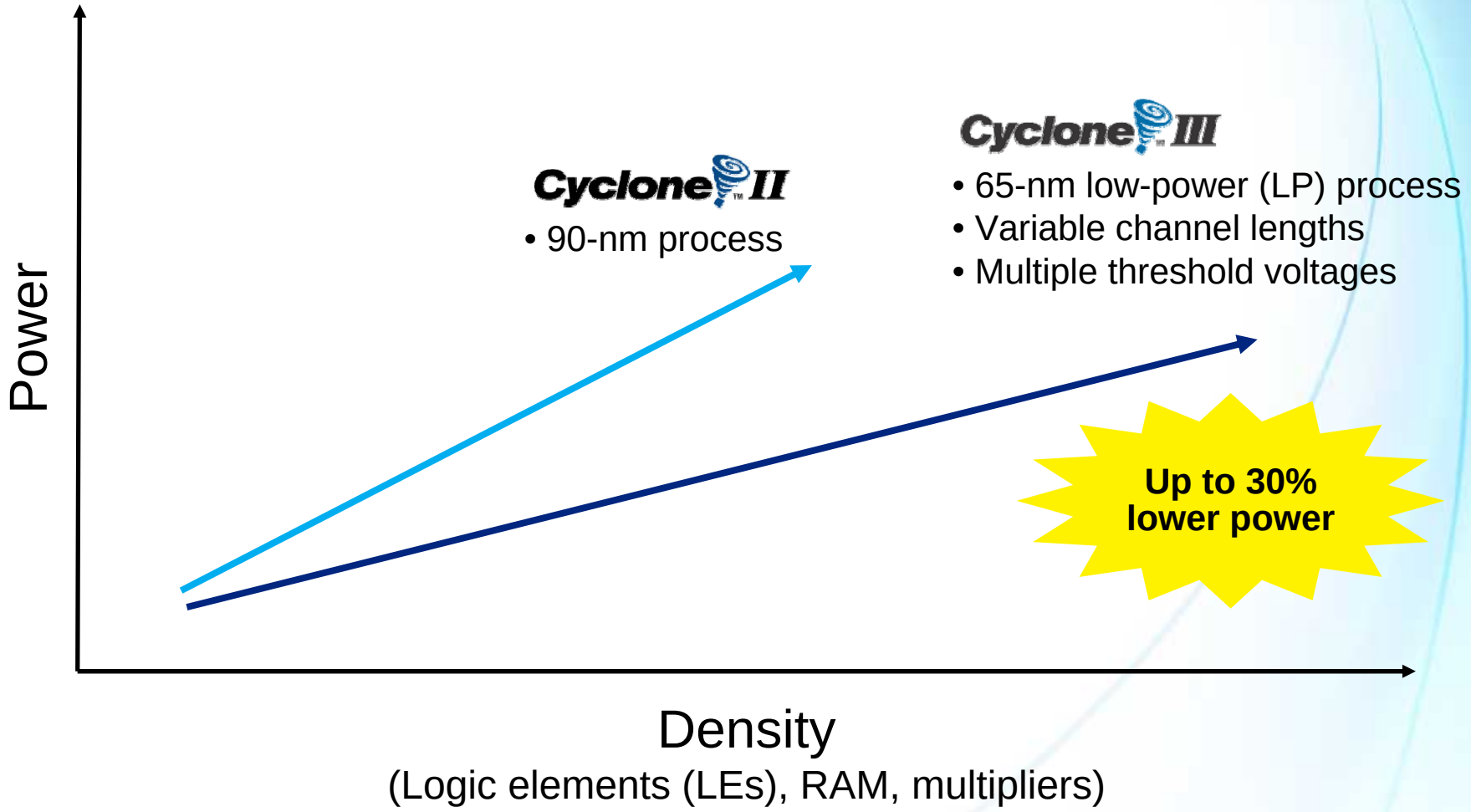
Selectable Core Voltage in Stratix III FPGAs

- Customer selects FPGA core voltage
  - 1.1 V for maximum performance
  - 0.9 V for minimum power
  - Programmable Power Technology is available to both voltages
- Quartus II software v7.1 includes timing models for both 1.1 V and 0.9 V

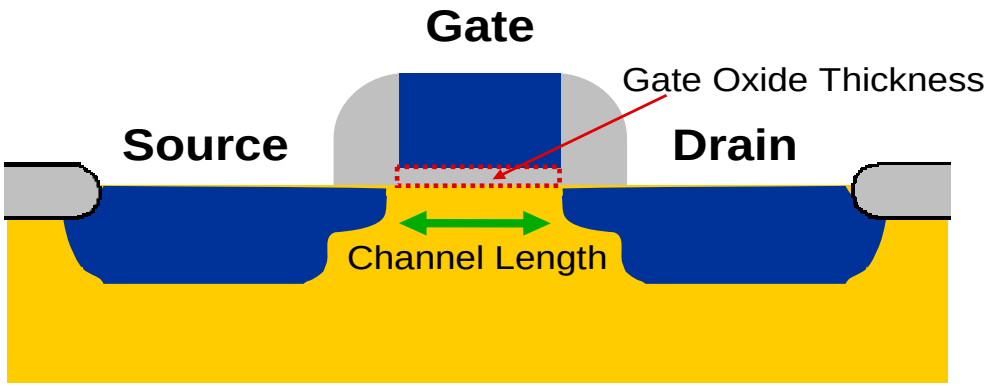
Core voltage	Dynamic power reduction from Stratix II FPGAs	Static power reduction from Stratix II FPGAs
1.1 V	33%	52%
0.9 V	55%	64%

Total power reduction reflects reduced capacitance, Programmable Power Technology, and other Stratix III architectural optimizations

Cyclone III Low Power Process Technology Power Optimization

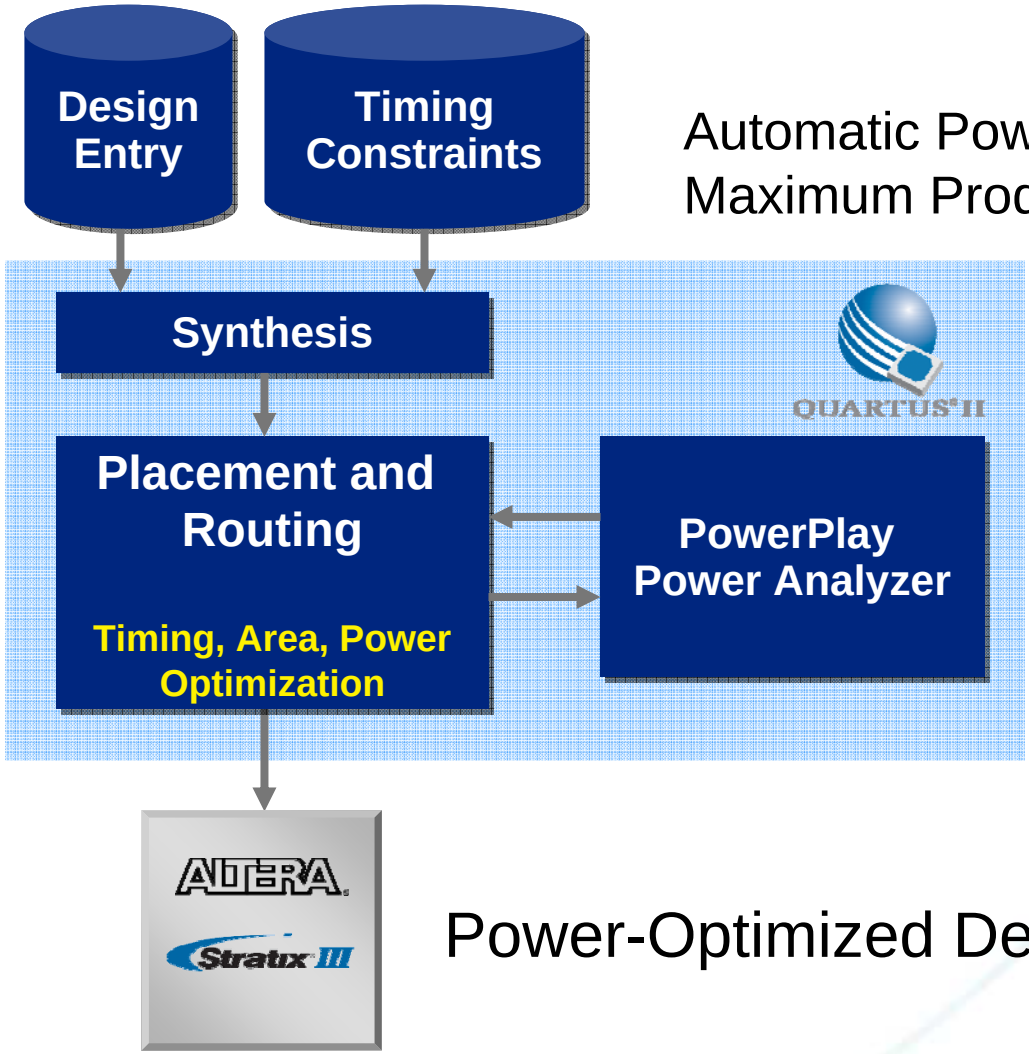


Applying the TSMC Low-Power Process



- Use low V_T transistors where performance is critical
  - Datapath signals in LEs
  - Extend the channel length of low V_T transistors to lower leakage current while maintaining needed performance
- Use slower high V_T transistors to reduce leakage in non-performance-critical circuits
  - Configuration RAM bits and other non-datapath circuits

Quartus II Software Design Flow



Automatic Power Reduction for Maximum Productivity

Timing is always met, then power optimizations are implemented

Power-Optimized Design ☑

ALTERA.

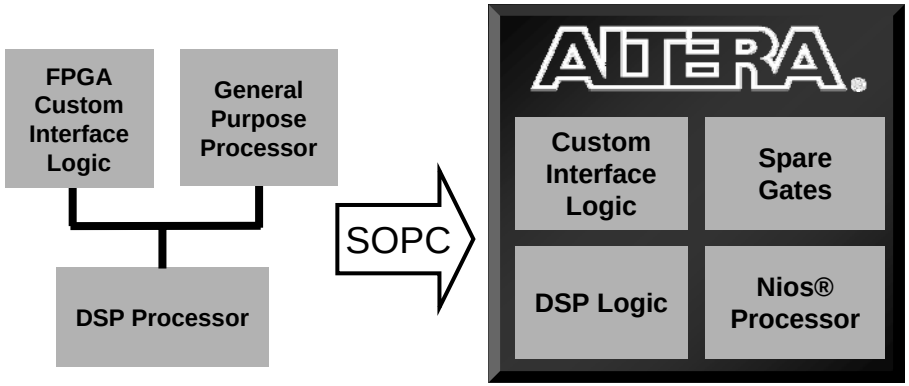
Scalability within a Footprint: Vertical Migration

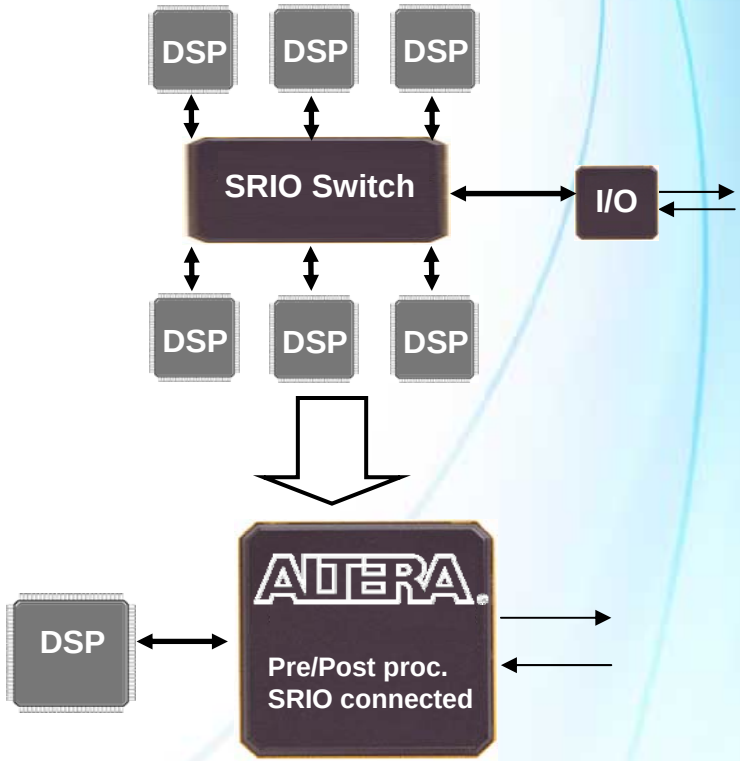
FPGA variant	Device	484-pin FPGA	780-pin FPGA	1152-pin FPGA	1517-pin FPGA	1760-pin FPGA
		1.0 mm 23 x 23	1.0 mm 29 x 29	1.0 mm 35 x 35	1.0 mm 40 x 40	1.0 mm 43 x 43
Stratix III L FPGAs	EP3SL50	288	480			
	EP3SL70	288	480			
	EP3SL110		480	736		
	EP3SL150		480	736		
	EP3SL200			736	864	
	EP3SE260			736	960	
	EP3SL340				960	1,104
Stratix III E FPGAs	EP3SE50	288	480			
	EP3SE80		480	736		
	EP3SE110		480	736		
	EP3SE260			736	960	

Denotes vertical migration support

Integration

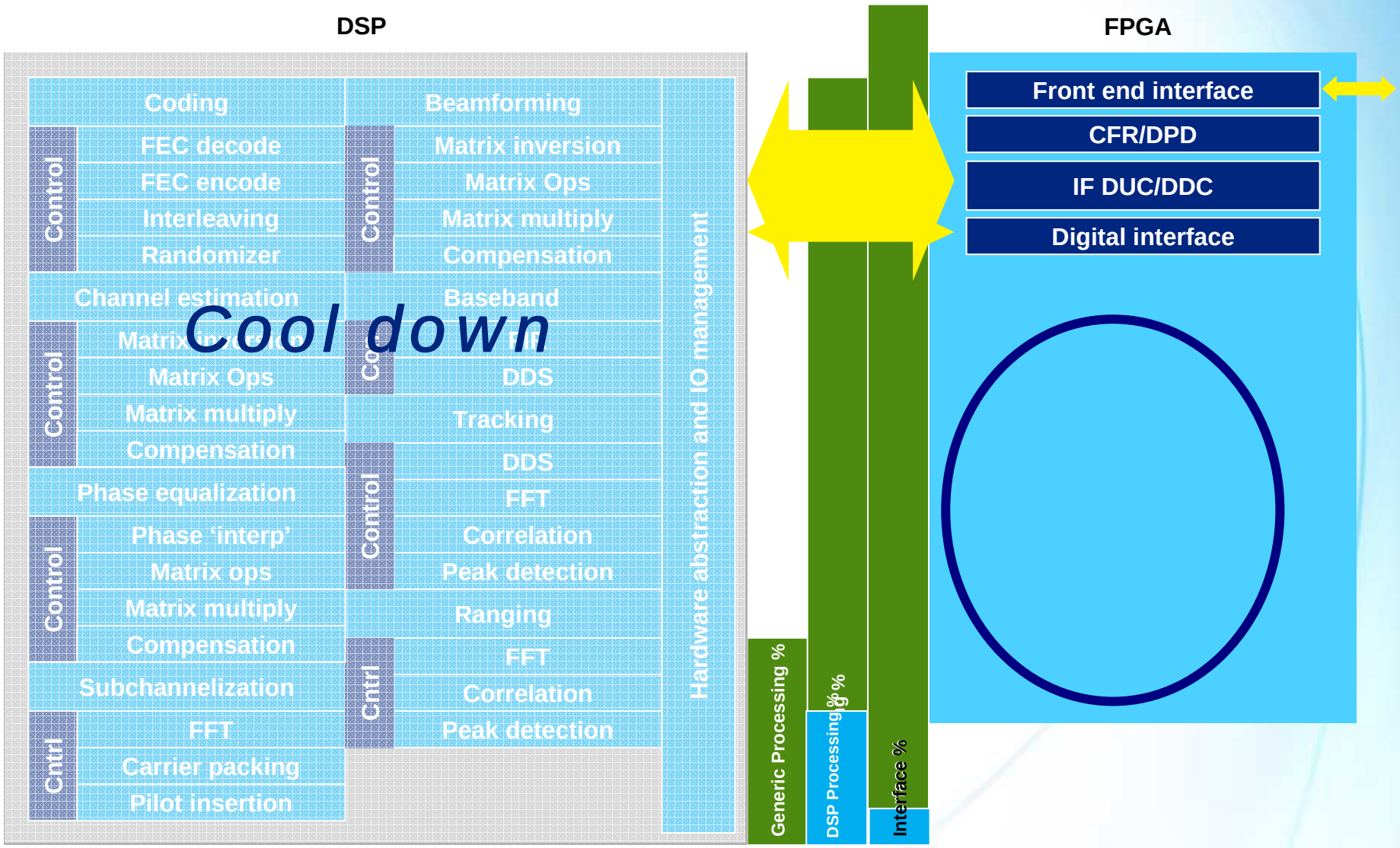
- Replace multiple DSP processors
  - Co-processor
  - Pre/post processor
  - Single chip solutions
- Integrate other system blocks
  - Specific interfaces
  - Control processor(s)
  - Custom logic





Implementation Example

Wireless Systems Example: Leverage FPGA Performance



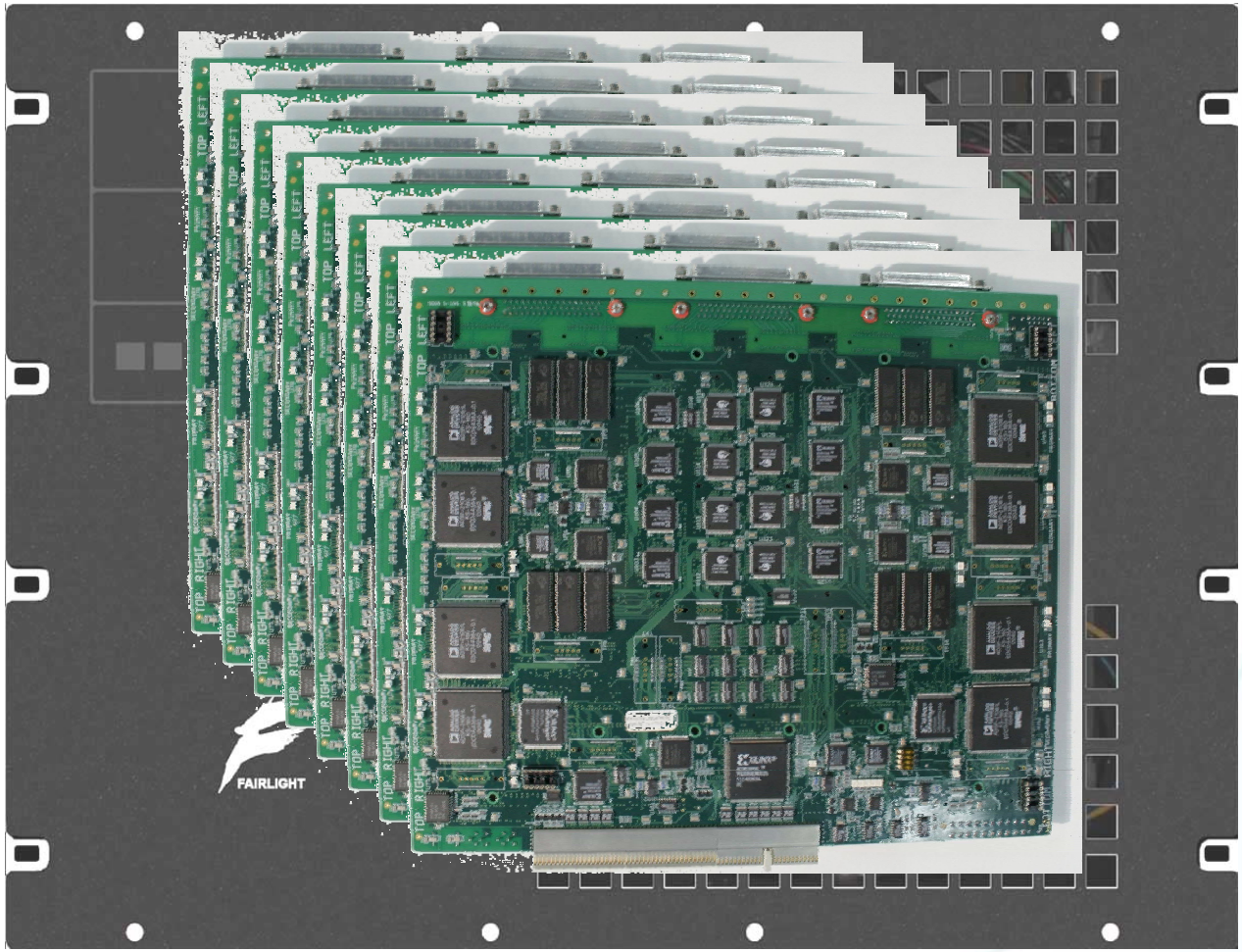
Fairlight

- Formed in 1975, invented first digital music sampling keyboard
- Today develops media processing platforms for film, television, and music
  - Stevie Wonder, Peter Gabriel, Moulin Rouge, Super Bowl XLI
- Two Academy Awards for audio technology
- Audio Technology Hall of Famer

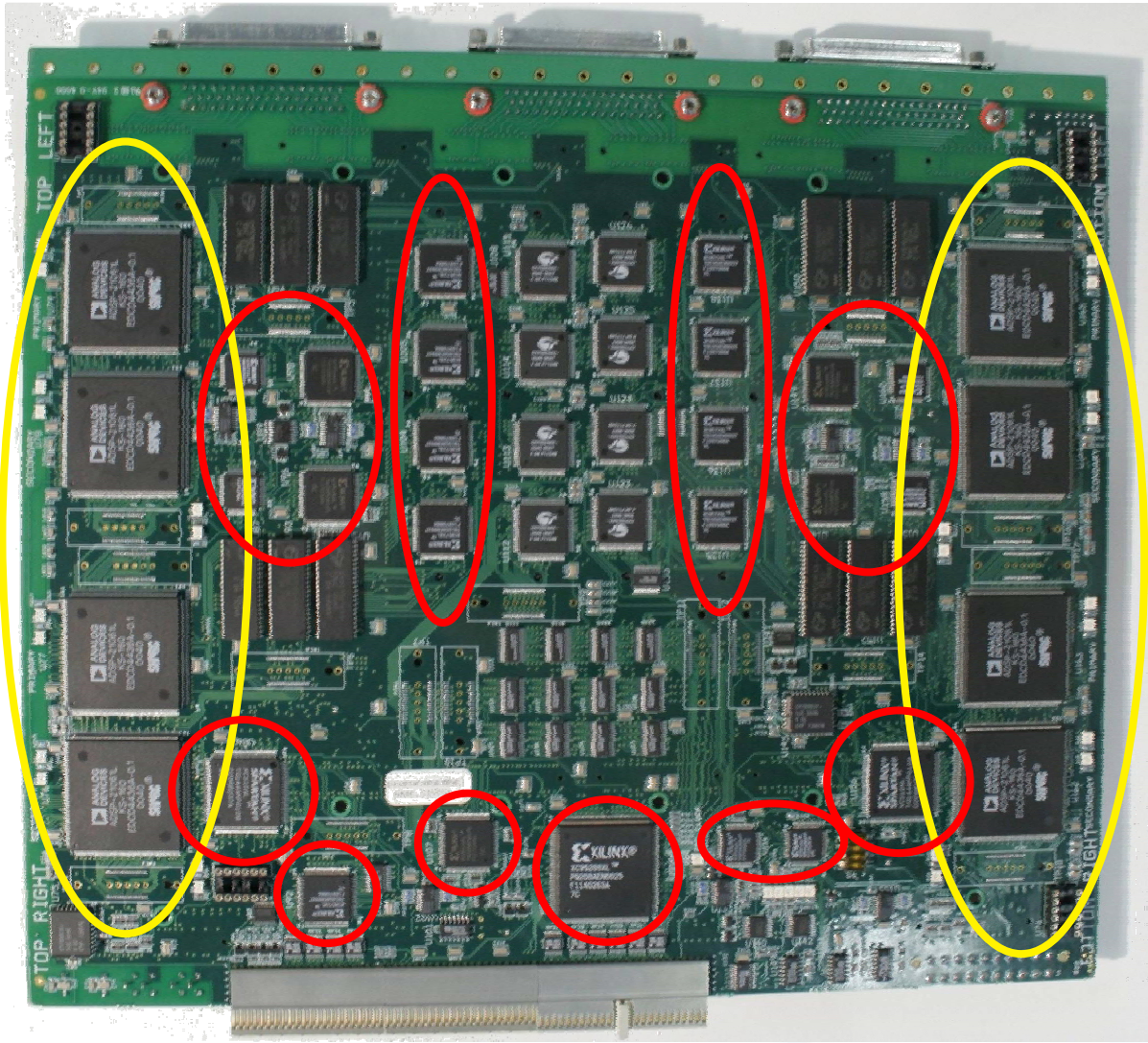
Fairlight Development History

- In 2003, Fairlight's state-of-the art media processing platform:
  - Based on DSP processors
  - Took 5 years to create
  - Cost $20M to develop
- In 2004, began development on next-generation platform for:
  - Guaranteed best-in-class performance
  - Best possible processing algorithms
  - Support for multiple applications
  - Price/performance advantage over other platforms

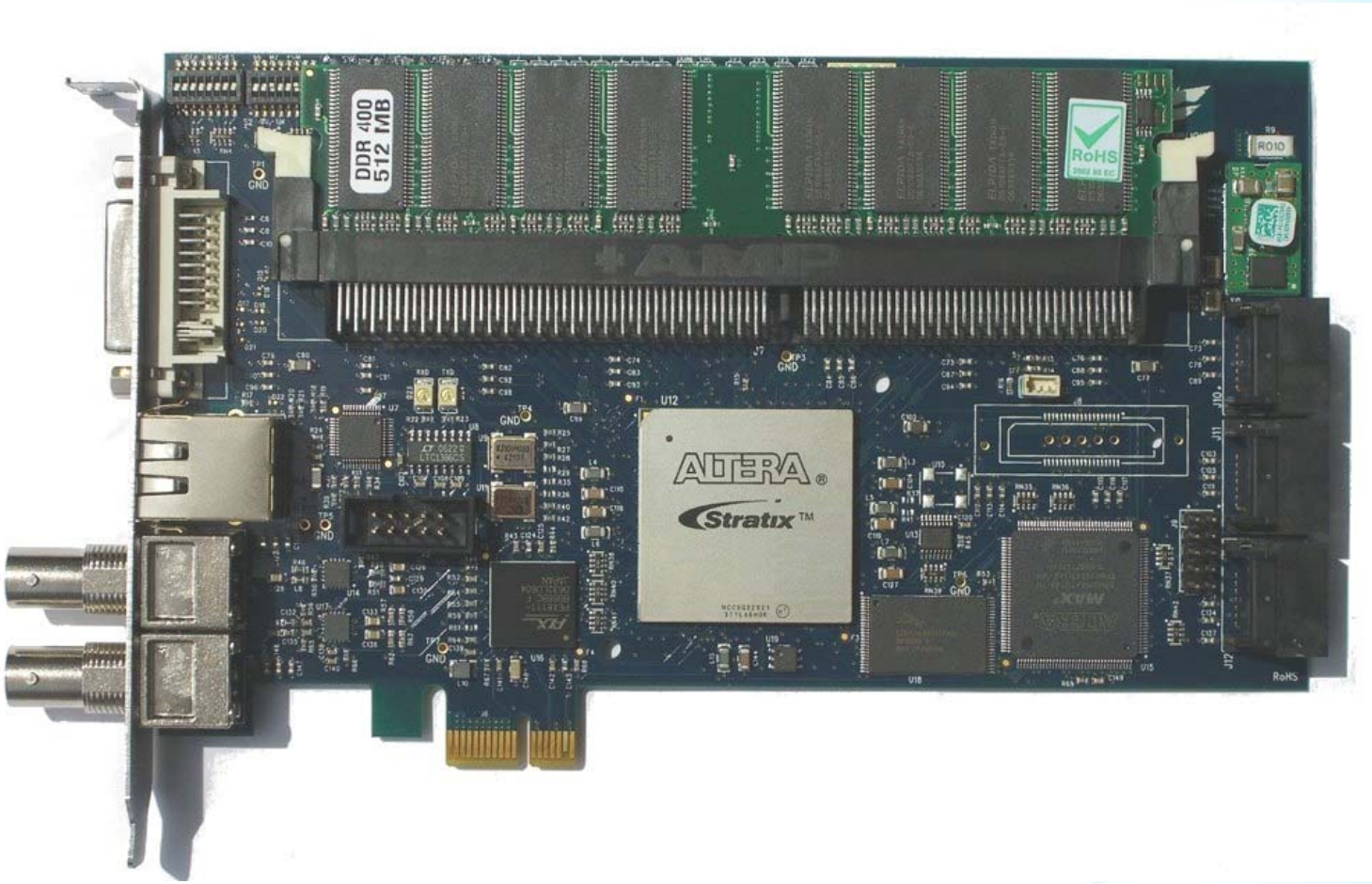
Fairlight's Original System



Fairlight's QDC Board



Fairlight's New System



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FPGA Value Proposition to Fairlight

- Performance
  - 8.6 GFLOPs per card
- Price
  - One Stratix device replaced 64 Analog Devices DSP processors
- Power
  - 600 watts reduced to 8 watts = 98% reduction in power and heat
- Integration
  - CC-1 replaces 8 boards of 64x40-bit floating point DSP devices at ~2% of cost
  - 8 RU of electronics replaced by pocket-sized processing module

Slide 27

CY5 What does the RU stand for? Should be spelled out

Christine Young, 6/1/2007

CY6

Conclusion

Slide 28

CY6 Probably don't need this slide, since there is only one summary slide after this one

Christine Young, 6/1/2007

Summary

- Performance
  - Parallelism offering 100s of GMACS
- Price
  - >10x the performance/price ratio of a DSP processor
  - Huge DSP performance from $4 (Cyclone® III)
- Power
  - Power/channel or per function is an order of magnitude better than DSP devices
- Scalability
  - Scalability/vertical migration within a footprint lowers risks
- Integration