

Agenda

- Gigabit Ethernet overview
- Emerging trends in communications
- Altera[®] Gigabit Ethernet solution
- Altera triple-speed Ethernet (TSE) intellectual property (IP) and demo





Ethernet Evolution

- Invented in 1973 at Xerox PARC to interconnect Altos workstations
- Ease of use led to wide adoption and lower costs
- Nearly 97% of computers use Ethernet to connect to Internet
- Consistently delivered higher performance at lower unit costs



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10 GbE: Extending the Reach and Applications of Ethernet

Fast Ethernet and Gigabit Ethernet

- 10/100 Mbps (Fast Ethernet) is universally used to connect computers to Internet
- 1 GbE becoming pervasive LAN technology

10 Gigabit Ethernet

- Extend reach of Ethernet to data centers, campus backbones, and metropolitan area networks



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Enterprise Campus Backbone (10 GbE-Based)



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Benefits of 10 GbE

Cost-effective solution

- \$10,000 per 10 GbE port
- Competitive SONET OC192 solutions range from \$64K to \$144K per port
- Based on widely deployed 10/100 Mbps and 1 GbE
 - Wide user acceptance
 - Well-trained workforce
- Can be deployed in all parts of the network
 - LAN: local area networks
 - SAN: storage area networks
 - MAN: metropolitan area networks
 - WAN: wide area networks







The Emerging Broadband Supermarket



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9 Source : Ericsson



IPTV Bandwidth Requirements



- Service mix may vary (eg. voice over IP) or service subsets may be offered
- 2nd HD channel initially to support concurrent home personal video recorder (PVR) recording
- Assumes quality of picture competitive with digital satellite/cable

HD=High Definition TV SD=Standard Definition TV HSI =High Speed Internet

Video Services Driving Bandwidth Requirements to the Home

Source: Alcatel

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Multicast Requirements for Video Driving Ethernet Aggregation Market

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DSL Trends: Distributed IP-DSLAM

- Distributed intelligence on line card: 1-Gbps network processing unit (NPU)
 - Local multicast replication ensures quick video response times
 - Internet Group Management Protocol (IGMP) snooping, IPv4 forwarding, L2TP tunneling
 - Flexibility critical
- Increased bandwidth requirements driving:
 - High-speed backplane
 - Bonded DSL links
- Momentum of NPUs targeting DSL line cards threatens FPGA business in DSLAM space



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Networking Trends

Ethernet everywhere

- Reduction of time division multiplexed (TDM) interfaces on routers/switches
- High number of GE/10GE ports: up to 200 GE + 20 10GE per node
- High-density line card (24xGE, 48xGE, 4x10GE over-subscribed to 10G packet processing)

Emergence of Ethernet aggregation

- Driven by IPTV and business Ethernet services
- Ethernet aggregation switches lower cost of edge router
 - Simpler header processing causing NPUs to shift focus from router to metro switch, e.g. Xelerated, EZchip, Greenfield Networks
 - Carrier class failure recovery scheme (< 50 ms) requires proprietary implementation (FPGA)
 - FPGA opportunities for bridge and CoS-aware scheduler
- Migration of legacy TDM onto Ethernet networks
 - Driven by high-margin business services
 - FPGA for interworking function (ATM, FR, POS, RPR, pseudowire)

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CY1



Stratix II GX Advantages for GbE



• 1, 2, 3, ... 20 ports

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Stratix II GX Gigabit Ethernet Media Access Control (MAC) Solution from Altera and MorethanIP

- Full-duplex Gigabit Ethernet MAC
- Integrated 1000 Base-X PCS and PMA
- Full implementation of IEEE 802.3 specification and compliance
- Supports all Stratix[®] II GX FPGAs
- Altera Atlantic[™] interface to application logic
- Developed by MorethanIP
 - Over 10 years experience with Ethernet technologies
- Distributed, licensed, and supported by Altera
 - FREE with Quartus[®] II software subscription



TSE MegaCore Feature Overview

Flexible and integrated MAC/PHY Ethernet solution

- Standalone 10/100/1000Mbps MAC
- Standalone PCS
- PCS + PMA
- 10/100/1000Mbps MAC + PCS + PMA
- MegaWizard[®] II GUI
- SOPC Builder-ready
- Software driver and protocol stack support
- IEEE 802.3 compliance
- UNH validated

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TSE MegaCore Function

- Single to multiple port 10/100-Mbps or 1-Gbps Ethernet applications
- LAN and WAN data plane or control plane (embedded system) applications
- Chip-to-chip, board-to-board, and inter-system network connectivity



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TSE v6.1 MegaWizard

MegaWizard II GUI

- Parameterize
 - Capture user options
 - Provide resource usage estimation
 - Derive HDL parameter and port information
- Generate
 - Top-level register transfer level (RTL) variation file
 - IP functional simulation model
 - Quartus II software constraint files
 - HDL testbenches and ModelSim simulation scripts

🕄 MegaWizard2		
	About Documentation	
10/100/1000 MAC 1000Base-X PCs		
Configuration	·	
Version:		
PHY Identifier (32 bit):	🔊 MegaWizard2	_ 0
	↓	
Use er	hbedded SERDES	Documentation
Management/Control	10/100/1000 MAC 1000Base-X PCS	
Reset signal level: 11	Core Module Options	
1.	Tinclude Asynchronous FIFOs	
	Include Host Interface with Registers instead of Configuration	Pins
	Set Version Number: Host Clock:	MHz
	☐ Include MDIO Module (MDC/MIO) Host Clock Divisor:	x.xx MHz
	Enable MAC 10/100 Half Duplex Support	
	Timplement MII/GMII loopback	
	Enable supplemental MAC unicast addresses	
	Implement Statistics Counters	
	Implement Multicast Hashtable	
	FIFO Configuration	
	Ingress (RX) depth	Width
	Memory Type: Gen (Embed Memory)	Csbit
	Depth:	C 32 bit
	Egress (RX) depth	
	Memory Type: Gen (Embed Memory)	
	Depth:	
	23000	
	RAM Blocks used: 4	
	Management/Control Clock settings (Simul	ation)
	Reset signal level: '1' VLocal: 125.0	MHz
	Can get Back Finish	
	Cancel < Back	Next > Einish



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Availability – IP Cores



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Summary

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- Gigabit Ethernet technology pervasive in communications due to aggregation of services
- Altera provides best-in class FPGAs for Gigabit Ethernet applications
 - Stratix II GX FPGAs for high-performance systems
 - Arria[™] GX FPGAs for mainstream Gigabit Ethernet applications
- Complete solution validated in hardware
 - IP cores, characterization reports, development boards
 - Interoperability

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