White Paper

Broadcast Video Infrastructure Implementation Using FPGAs

Introduction

The proliferation of high-definition television (HDTV) video content creation and the method of delivering these contents in a bandwidth-limited broadcast channel environment have driven new video compression standards and associated video image processing applications. Traditionally, only cable and satellite operators provided video delivery. Now telecommunication companies (telcos) are getting into this arena by using the latest video coder/decoders (CODECs) and video-processing technology to transmit digital video to the consumer via Internet protocol television (IPTV).

Video and Image Processing Trends

Many new and exciting innovations, such as HDTV and digital cinema, revolve around video and image processing, and the evolution of this technology is rapid. Leaps forward in image capture and display resolutions, advanced compression techniques, and video intelligence are the driving forces behind this innovation. Resolutions in broadcast equipment have increased significantly over the last few years, as shown in Table 1.

Table 1. Resolution by Broadcast End Equipment

End Equipment	Resolution
HDTV	1920 x 1080 pixels
Digital Cinema	4096 x 1714 pixels

Advanced compression techniques are replacing previous-generation technology, offering enhancements like better streaming capability, higher compression for a given quality, and lower latency. JPEG2000 is also gaining momentum in storage and digital cinema. Even as these new compression solutions are deployed, standards committees continue to enhance H.264 and JPEG2000 standards.

In the last 10 years, the digital television broadcast industry has been well served by the MPEG-2 standard for standard-definition television (SDTV). H.264-AVC (MPEG4-Part 10) and the Microsoft version, VC1, will eventually replace MPEG-2 as a video-encoding method for both SDTV and HDTV. Broadcast equipment manufacturers must provide various encoding standards in order to satisfy current and future needs. In addition to the various core video CODEC standards, there are also different types of video pre- and postprocessing algorithms used to enhance the overall picture quality for the consumer.

With expanding resolutions and evolving compression, there is a need for high performance while keeping architectures flexible to allow for quick upgradeability. In addition, as a technology matures and its volumes increase, there will be a desire to reduce costs. By providing solutions for these needs, programmable logic devices (PLDs) play an important role for the emerging digital video broadcast infrastructure.

Video Content Creation

The first stage of the video broadcast chain is the professional digital video camera that captures the video and audio contents. The video can either be SD or HD. This digital camera will typically have a Society of Motion Picture and Television Engineers (SMPTE)-defined serial data interface (SDI) output. SDI is an uncompressed video stream running at 270 Mbps (SD), 1.485 Gbps (HD), or 2.97 Gbps (1080p HD). Altera's Stratix® II GX FPGAs, with their integrated serializer/deserializer (SERDES) and clock/data recovery (CDR), process the video stream onto the SDI output of the camera.

Video Pre- and Postprocessing

The NTSC standard for television transmission, used by broadcasters in North America, has a fixed 6-MHz bandwidth per channel. (The 8-MHz PAL standard is used in Europe and other parts of the world.) This bandwidth

limitation was set long before digital television emerged. This analog bandwidth limitation dictated the current digital television (DTV) transmission specification. Digital video quality is superior to the classical analog video. The higher the digital resolution, the higher the bandwidth that is required to convey or transmit the video data. Delivering good quality video almost invariably requires preprocessing the source video.

Limiting the available bandwidth in the digital domain with various video compressions will manifest in different ways when displaying the decoded stream. Pushing the video compressor hard will produce block noise or blocking artifacts, due to the DCT of the block-based CODEC. Video pre- and postprocessing makes it easier for the encoder to compress the video, as well as further enabling it to improve picture quality and reduce delivery bandwidth requirements. This capability is of critical importance for cable, satellite, telcos, and IPTV broadcast business models where meeting high quality demands must be achieved within narrow bandwidth constraints. The preprocessing may involve using 2D filtering to smooth out some of the high-frequency content before it enters the encoder to reduce the amount of block noise. Altera's Video and Image Processing Suite includes 2D finite impulse response (FIR) and median filter functions. They provide a flexible and efficient means to perform 2D FIR filtering operations using matrices of 3x3, 5x5, or 7x7 constant coefficients. Therefore, pre- and postprocessing are key differentiators for any type of video compression to have the best performance in a bandwidth-limited environment.

Video Compression

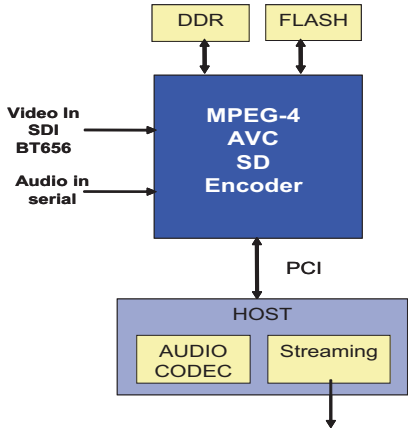
The next stage sets the course for compressing the preprocessed raw video data before transmitting to the end user. There are various generations of compression standards ranging from MPEG1 to MPEG4, with four methods for compression: discrete cosine transform (DCT), vector quantization (VQ), fractal compression, and discrete wavelet transform (DWT). Table 2 summarizes the various MPEG standards

Table 2. Compression Standards

Standard	Data Rate	Applications
MPEG-1	<1.5 Mbps	VCD for CD-ROM, Level 3 is the most popular for MP3 audio
MPEG-2	1.5 Mbps to 15 Mbps	DTV for cable satellite and terrestrial broadcast
MPEG-4	0.5 Mbps to 40 Mbps	Video conferencing, surveillance, and broadcasting with Part 10 for H.264

MPEG-2 is the dominant standard for DTV across the world, with digital cable, satellite, and terrestrial broadcasters still using this standard. As the broadcast industry trends toward more HD content, the given transmission bandwidth is under ever more pressure to make it fit in the predefined analog bandwidth spectrum. As IPTV starts to roll out on the traditional telco wiring systems, MPEG-2 definitely will not be economical or feasible for carrying video programs to consumers. The ITU-T Video Coding Experts Group (VCEG), together with the ISO/IEC Moving Picture Experts Group (MPEG), introduced the MPEG4-Part 10 (also called H.264) standard. Capable of providing good video quality at bit rates substantially lower than previous standards, H.264 does so without so much of an increase in complexity as to make the design impractical (excessively expensive) to implement. An additional goal was to allow the standard to be flexible enough to be applied to a very wide variety of applications (both low and high bitrates, as well as low- and high-resolution video) and to work well on a very wide variety of networks and systems. By using the Stratix II FPGA, Altera's intellectual property partner ATEME has introduced the industry’s first single-chip SD H.264 main profile encoder for the broadcast industry (Figure 1).

Figure 1. Stratix II Single-Chip H.264 Encoder Block Diagram



There are also other compression standards such as JPEG2000, which use state techniques based on wavelet technology. The architecture should lend itself from portable digital cameras, video storage, and advanced medical imaging.

Video Distribution

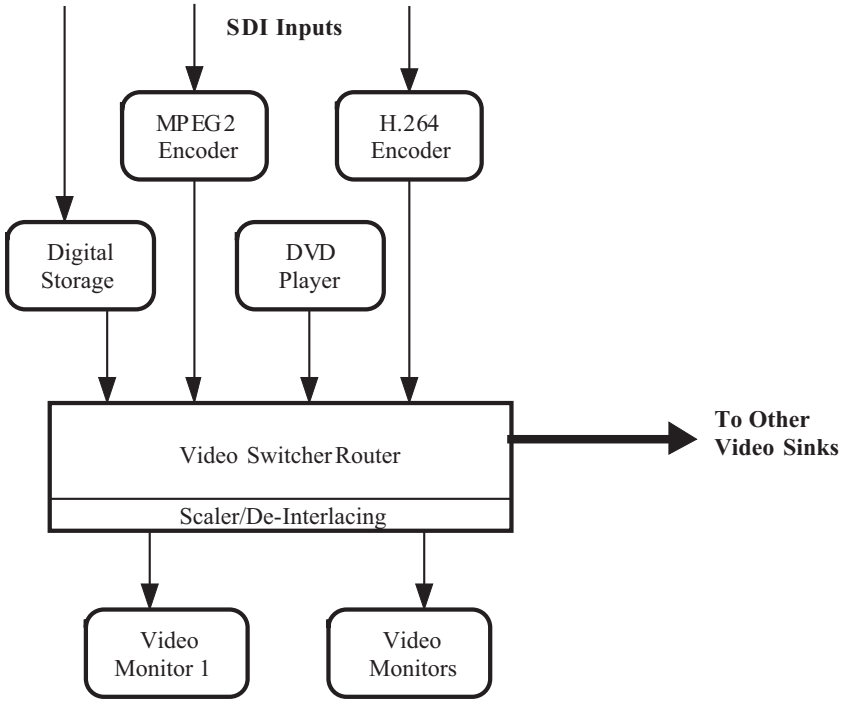
The compressed video can be routed and distributed within the broadcast studio facility by using the ASI standard for short distance routing. The industry trend is to use a video over IP network to distribute video data over long distances. Altera offers a video over IP reference design that demonstrates the transmission of MPEG-2 transport stream (TS) data over IP-based networks. The reference design bridges one or more compressed video streams and IP packets with 100 Mbps or 1 Gbps Ethernet. The ASI encode and decode reference design is also available. A digital video broadcast asynchronous serial interface (DVB-ASI) is a serial data transmission protocol that transports MPEG-2 packets over copper-based cables or optical networks.

Video Scaling and De-Interlacing

Production studio and head-end equipment can usually perform video scaling and de-interlacing for applications such as SD to HD conversion or vice versa. Other applications include filters for edge detection processing, vertical motion filter, and interfield motion filter.

One of the common requirements for many professional studios is the ability to use single or multiple display devices to show a variety of normal SDTV or HDTV signals. The ability to easily control the switching between these various sources via a remote control is essential in creating an professional, easy-to-use system. Therefore video scaling and de-interlacing is essential for the video switcher/router that is capable of handling the different type of video resolution for video switching, routing, and local displays, such as the one shown in Figure 2.

Figure 2. Studio Monitors



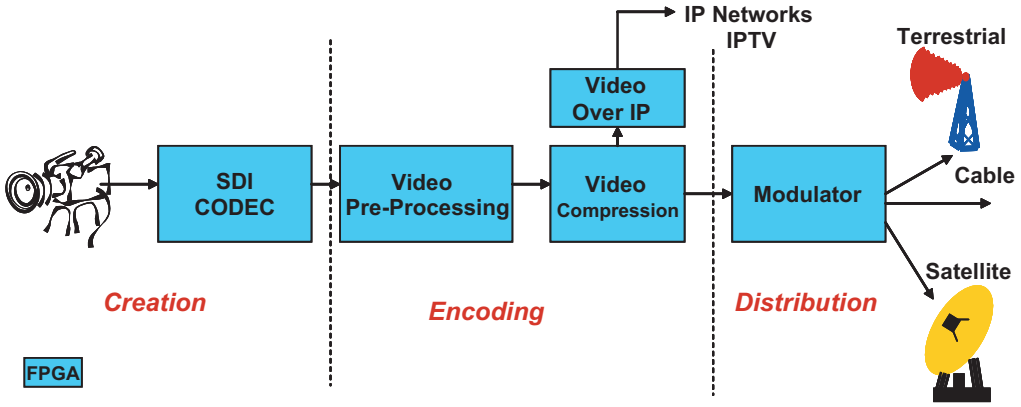
Color Space Conversion and Video Formats

Since there are many video formats that broadcasters must work with, depending on where the final end users are located, the broadcast studio must be able to convert between different color spaces and video formats. Color is described using different color space domains, with each space domain associated to various applications based on system requirements. Color information is determined by two separate chrominance signals, Cb and Cr, which are a function of a third signal, Y, the brightness or luminance signal. The RGB color space is also defined by three components, red, green, and blue. Color space conversion is often necessary when transferring data between devices that use different color space models. For example, to transfer a television image to a computer monitor, you may need to convert the image from the YCbCr color space to the RGB color space. Conversely, transferring an image from a computer display to a television set may require a transformation from the RGB color space to the YCbCr color space. The Altera® color space converter MegaCore® function can be used to perform these types of color transformations for a variety of applications.

Overall Broadcast System Infrastructure

The overall digital broadcast infrastructure originates with the video content creation from either the television studio or the motion picture production studio. The creation process interface uses SDI for transporting the raw video to a storage device or to some type of nonlinear editor (NLE) for video editing and feature enhancement. The final edited video is compressed using MPEG-2, JPEG2000, or H.264 during the encoding process before being distributed to the consumers via cable, satellite, terrestrial, or the latest IPTV technology network. Figure 3 shows a high-level building block of a broadcast infrastructure.

Figure 3. Broadcast Infrastructure



Video and Image Processing System Architectures

System architecture choices include standard cell ASICs, ASSPs, and programmable solutions such as digital signal processing (DSP) or media processors and FPGAs. Each of the approaches has advantages and disadvantages, with the ultimate choice depending on end equipment requirements and solution availability. Given the trends discussed above, the ideal architecture would have the following characteristics: high performance, flexibility, easy upgradability, low development cost, and a migration path to lower cost as the application matures and volume ramps.

High Performance

Performance not only applies to compression, but also pre- and postprocessing functions. In fact, in many cases these functions consume more performance than the compression algorithm itself. Examples of these functions include scaling, de-interlacing, filtering, and color space conversion.

The broadcast market's need for high performance rules out processor-only architectures. They simply cannot meet the performance requirements with a single device. A state-of-the-art DSP running at 1 GHz cannot perform H.264 HD decoding or H.264 HD encoding, which is about ten times more complex than decoding. FPGAs are the only programmable solutions able to tackle this problem. In some cases, the best solution is a combination of an FPGA plus an external DSP processor.

Flexibility Provides Fast Time to Market and Easy Upgradability

When technology rapidly evolves, architectures must be flexible and easy to upgrade. Since standard cell ASICs and ASSPs are neither, they cannot be used for those applications. Typically designed for very high-volume consumer markets, ASSPs often are quickly obsolete, making them an extremely risky choice for most applications.

Low Development Cost

When adding up costs for masks and wafer, software, design verification, and layout, development of a typical 90-nm standard-cell ASIC can cost as much as US$30 million. Only the highest volume consumer markets can justify such pricey development costs.

Migration Path to Lower Unit Costs

As standards stabilize and volumes increase, it is important to have a solution with a low-cost migration path. Often this means either market-focused ASSPs or standard-cell custom ASIC devices. However, the rising cost of custom silicon makes those solutions economically feasible in only the highest volume consumer applications. Most silicon companies with a focus on video and imaging target applications such as video camcorders, set-top boxes, digital still cameras, cell phones and other portable products, or LCD TVs and monitors. Therefore, when designing a

lower-volume type of application, it is best to consider an FPGA, as it is unlikely an ASSP with the exact feature set required exists, and even the best off-the-shelf solution is a risky choice due to the high potential for obsolescence.

Altera's Video and Image Processing Solution

For the reasons described above, FPGAs are particularly well suited to meet the requirements of many video and image processing applications. Altera FPGAs have the following characteristics that make them very appealing for video and image processing architectures:

- *High performance:* HD processing can be implemented in a single Altera FPGA.
- *Flexibility:* Altera FPGAs provide the ability to upgrade architectures quickly to meet evolving requirements and standards, while scalability allows use of FPGAs in low-cost and high-performance systems.
- *Low development cost:* Video development kits from Altera start as low as US$1,095 and include the software tools required to develop a video system using Altera FPGAs.
- *Obsolescence proof:* Altera FPGAs have a very large customer base that ships products for many years after introduction. In addition, FPGA designs are easily migrated from one process node to the next.
- *Structured ASIC migration path to lower costs:* Altera structured ASICs start at US$15 at 100ku for 1 million ASIC gates.
- *Altera's Video and Image Processing Solution:* This includes optimized DSP Design Flows, Altera's Video and Image Processing Suite, interface and third-party video compression intellectual property, and video reference designs.

ASSP-Like Functionality on FPGAs/Structured ASICs

With a growing number of solutions, Altera and its partners provide ASSP functionality in the form of an FPGA or structured ASIC. An example of this is ATEME's H.264 Main Profile Standard Definition Encoder product. With this product, customers use FPGAs just as they do an ASSP. The benefit over the traditional ASSP approach is that the FPGA solution evolves quickly, with no risk of obsolescence.

DSP Design Flow

For custom development, Altera provides an optimized DSP design flow that allows several different ways to represent the design. These include VHDL/Verilog, model-based design, and C-based design. Altera's Video and Image Processing Suite of functions can be used in conjunction with any of these design flow options.

Altera and The MathWorks have joined forces to create a comprehensive DSP development flow that allows designers to enjoy the price/performance benefits of Altera FPGAs while leveraging Simulink, The MathWorks's model-based design tool. Altera's DSP Builder is a DSP development tool that connects Simulink with Altera's industry-leading Quartus® II development software. DSP Builder provides a seamless design flow in which designers perform algorithmic development in the MATLAB software and system-level design in the Simulink software, then port the design to hardware description language (HDL) files for use in the Quartus II software. The DSP Builder tool is tightly integrated with the SOPC Builder tool, allowing the user to build systems that incorporate Simulink designs and Altera embedded processor and intellectual property cores. This development flow is easy and intuitive for designers who do not have extensive experience using programmable logic design software.

Video and Image Processing Suite

The Video and Image Processing Suite consists of nine functions with parameters that can be statically, or in some cases, dynamically changed. Table 3 summarizes these functions.

Table 3. Functions Available With the Video and Image Processing Suite

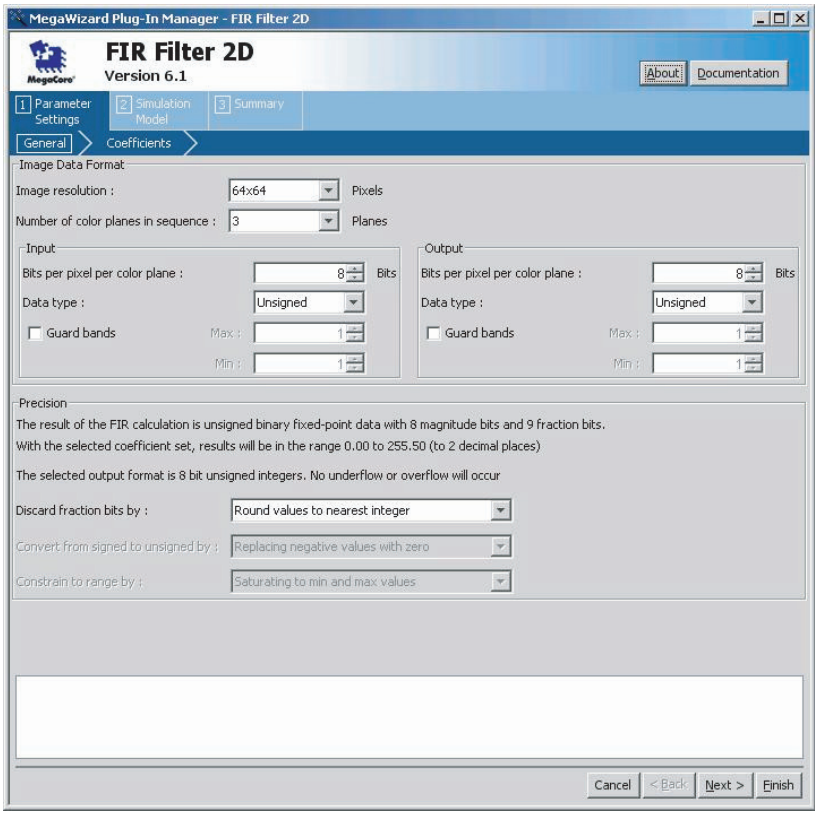
Function	Description
De-Interlacer	Converts interlaced video formats to progressive video format
Color Space Converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames

Table 3. Functions Available With the Video and Image Processing Suite

Function	Description
Alpha Blending Mixer	Mixes and blends multiple image streams
Gamma Corrector	Performs gamma correction on a color plane/space
Chroma Resampler	Changes the sampling rate of the chroma data for image frames
2D Filter	Implements 3x3, 5x5, or 7x7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images
2D Median Filter	Implements 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line Buffer Compiler	Efficiently maps image line buffers to Altera on-chip memories

The 2D Filter GUI shown in Figure 4 is an example of the type of user configuration available with the cores provided in the Video and Image Processing Suite. Resolutions, bits per sample, FIR filter size, edge behavior, overflow behavior, and accumulator length are all static parameters supported in the 2D filter core

Figure 4. 2D Filter GUI



Video Compression

Several third parties have video compression solutions targeting Altera FPGAs and structured ASICs. Table 4 lists some of the common video compression standards and associated third parties.

Table 4. Third-Party Video Compression Solutions

Function	Company
H.264 Main and High Profile	ATEME
H.264 Baseline Profile	CAST, W&W
JPEG/JPEG2000	Barco, Broadmotion, CAST

Table 4. Third-Party Video Compression Solutions

Function	Company
MPEG4 SP/ASP	Barco, CAST

Video Interfaces and System Intellectual Property

Altera and its partners also provide interface cores that are often required in a video system. These include ASI, SDI, 10/100/1000 Ethernet, and DDR/DDR2 Memory Controllers. Table 5 is a partial listing of these types of cores and reference designs.

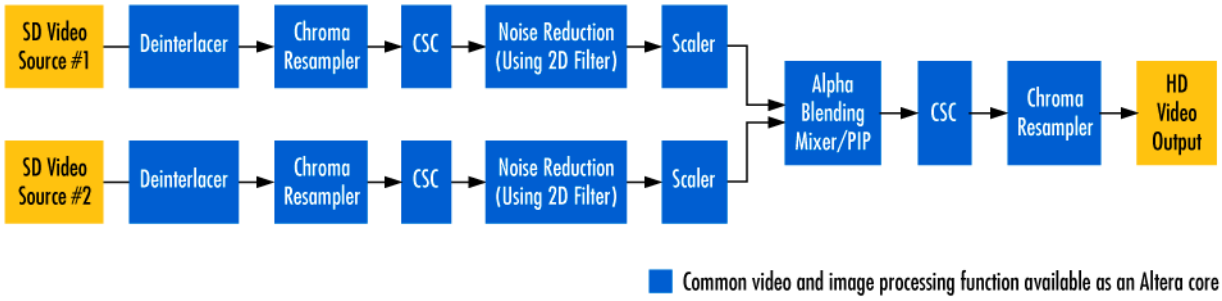
Table 5. Video Interfaces and System Intellectual Property

Function	Company
10/100/1000 Ethernet	Altera, MoreThanIP
DDR/DDR2 Memory Controllers	Altera
32-bit RISC Processor	Altera (Nios® II)
Serial RapidIO™ Interface to External Processors	Altera
TI EMIF Interface	Altera Reference Design
ATA Hard Disk Drive Interface	Nuvation
NOR Flash	Altera
Compact Flash and SD Interfaces	Altera
Video Over IP	Altera Reference Design
ASI	Altera
SDI	Altera

Example Video Design

A typical video system using the Video and Image Processing Suite is shown in Figure 5.

Figure 5. Example Design Block Diagram



Video Development Kits

Altera currently offers two video development kits. The Audio Video Development Kit, Stratix II GX Edition has a 2-channel composite video input, VGA output port, 96-KHz audio I/O, 256-Mbyte DDR2 DRAM, and Cyclone II device. The Video Development Kit, Stratix II GX Edition provides support for 4-channel HD SDI, ASI, DVI, HDMI, USB, Gigabit Ethernet, 1394, and DDR2 SDRAM. A video reference design using the Video and Image Processing Suite and DSP Builder and SOPC Builder development tools is included with the kits. In addition to these kits, there are several Altera third-party development kits targeted at video solutions.

Benchmarks

Table 6 and Table 7 show example functions and the corresponding FPGAs required for implementation.

Altera's Cyclone III low-cost FPGAs incorporate up to 4 Mbits of embedded memory, 488 embedded 9x9 multipliers at 260 MHz, and 120,000 logic elements (LEs). The Cyclone III EP3C40 device is a midrange FPGA in the family and is priced at under US$20 for 250,000 units.

Stratix II high-performance, high-density devices incorporate up to 9 Mbits of embedded memory, 768 9x9 embedded multipliers at 450 MHz, and 179,000 LEs. These functions also can be implemented in Altera's HardCopy® II structured ASIC devices.

Table 6. Encoding Standard Benchmarks

Encoding Standard	FPGA Implementation
H.264 Baseline Profile SD Encoding	Cyclone III EP3C40 *(1)*
H.264 Baseline Profile 1280x1024 Encoding	Stratix II EP2S30 *(1)*
H.264 Main Profile SD Encoding	Stratix II EP2S130
H.264 High Profile 720p Encoding	Multiple Stratix II FPGAs
JPEG2000 Digital Cinema Encoding (2k)	Stratix II EP2S130

Note:
(1) Significant logic, memory, and DSP resources left for pre- and postprocessing functions

Table 7. Pre- and Postprocessing Benchmarks

Pre- and Postprocessing	FPGA Implementation
5x5 2D Filter for 720p	Cyclone III EP3C10
5x5 2D Median Filter for 720p	Cyclone III EP3C10
Linear Interpolation Scaler for SD to 720p	Cyclone III EP3C5

Summary

PLDs will play an increasingly important role in the digital buildup of the broadcast industry infrastructure. The key value proposition of PLDs give equipment manufacturers the flexibility and upgradeability to be competitive in this industry. Altera's portfolio of products not only provides the silicon hardware, but also the intellectual property needed to implement an entire system solution from content creation, through encoding, to the distribution chain.

Further Information

- Altera's Video and Image Processing Solutions website:
  www.altera.com\video_imaging
- Altera's Video Processing Reference Design:
  www.altera.com/end-markets/refdesigns/sys-sol/broadcast/ref-post-processing.html

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