White Paper

Video and Image Processing Design Using FPGAs

Introduction

In this paper, we will look at the trends in video and image processing that are forcing developers to re-examine the architectures they have used in the past. This paper will discuss the tradeoffs of different architectures and conclude with details and benchmarks for Altera's new solutions in this area. With low-cost FPGAs and structured ASICs, high-definition solutions can now be implemented for less than US$1.00 per 1,000 logic elements (LEs).

Video and Image Processing Trends

Many new and exciting innovations, such as HDTV and digital cinema, revolve around video and image processing and this technology's rapid evolution. Leaps forward in image capture and display resolutions, advanced compression techniques, and video intelligence are the driving forces behind the technological innovation.

Resolutions in particular have increased significantly over the last few years. Table 1 shows current state-of-the-art resolutions in different end equipment types.

Table 1. Resolutions by End Equipment Types

End Equipment	Resolution
HDTV	1920 x 1080 pixels
Digital Cinema	4096 x 1714 pixels
Videoconferencing	1280 x 720 pixels
Medical Imaging	3000 x 3000 pixels
Industrial Surveillance	1280 x 720 pixels
Military Surveillance	4000 x 4000 pixels
Machine Vision	4000 x 4000 pixels

The move from standard definition (SD) to high definition (HD) represents a 6X increase in data that needs to be processed. Video surveillance is also moving from Common Intermediate Format (CIF) (352 x 288) to D1 format (704 x 576) as a standard requirement, with some industrial cameras even moving to HD at 1280 x 720. Military surveillance, medical imaging, and machine vision applications are also moving to very high resolution images.

Advanced compression techniques are replacing previous generation technology, offering enhancements like better streaming capability, higher compression for a given quality, and lower latency. As the standard for digital cinema, JPEG 2000 is gaining momentum in military, medical imaging, and surveillance. H.264 is expected to replace MPEG2 in broadcast TV applications, MPEG4 Part 2 in video surveillance systems, and H.263 in videoconferencing. Even as these new compression solutions are deployed, ongoing standards activity continues to enhance H.264 and JPEG 2000 standards.

The DICOM medical imaging standard has finalized Supplement 105, including multicomponent transformations in Part 2 of JPEG 2000 for the compression of 3D medical imagery. Supplement 106 will include JPIP as a protocol for remote browsing of medical images compressed using JPEG 2000.

The next extension to MPEG 4 Part 10 (H.264 AVC) is Scaleable Video Coding (SVC). SVC addresses coding schemes for reliable delivery of video to diverse clients over heterogeneous networks using available system resources, particularly in scenarios where the downstream client capabilities, system resources, and network conditions are not known in advance. For example, clients may have different display resolutions, systems may have different caching or intermediate storage resources, and networks may have varying bandwidths, loss rates, and best-effort or quality-of-service (QoS) capabilities. An extension of AVC/H.264 is being developed by the Joint Video Team (JVT) to provide scalability at the bitstream level, with good compression efficiency, and allowing free

combinations of scalable modes (such as spatial, temporal, and SNR/fidelity scalability). Application areas include video surveillance systems, mobile streaming video, wireless multichannel video production and distribution, and multiparty video telephony/conferencing.

Another rapidly evolving area is video intelligence. Cameras have had the ability to pan, tilt, zoom, and panorama, but these will be driven increasingly by system intelligence rather than manual intervention. Motion detection allows more efficient hard disk storage by only archiving video frames where a motion threshold is passed. The promise of video object recognition would allow for automated surveillance monitoring, which is much more effective than manual surveillance monitoring.

With expanding resolutions and evolving compression, there is a need for high performance while keeping architectures flexible to allow for quick upgradeability. As technologies mature and volumes increase, there also will be a desire to reduce costs.

Video and Image Processing System Architectures

System architecture choices include standard cell ASICs, ASSPs, and programmable solutions such as digital signal processing (DSP) or media processors and FPGAs. Each of the approaches has advantages and disadvantages, with the ultimate choice depending on end equipment requirements and solution availability. Given the trends discussed above, the ideal architecture would have the following characteristics: high performance, flexibility, easy upgradability, low development cost, and a migration path to lower cost as the application matures and volume ramps.

High Performance

Performance not only applies to compression, but also pre- and postprocessing functions. In fact, in many cases these functions consume more performance than the compression algorithm itself. Examples of these functions include scaling, de-interlacing, filtering, and color space conversion.

For the markets described above, the need for high performance rules out processor-only architectures. They simply cannot meet the performance requirements with a single device. A state-of-the-art DSP running at 1 GHz cannot perform H.264 HD decoding or H.264 HD encoding, which is about ten times more complex than decoding. FPGAs are the only programmable solutions able to tackle this problem. In some cases, the best solution is a combination of an FPGA plus an external DSP processor.

Flexibility Provides Fast Time to Market and Easy Upgradeability

When technology rapidly evolves, architectures must be flexible and easy to upgrade. This rules out standard cell ASICs and ASSPs for those applications. Typically designed for very high volume consumer markets, ASSPs often are quickly obsolete, making them an extremely risky choice for most applications.

Low Development Cost

When adding up costs for masks and wafer, software, design verification, and layout, development of a typical 90-nm standard-cell ASIC can cost as much as US$30 million. Only the highest volume consumer markets can justify such pricey development costs.

Migration Path to Lower Unit Costs

As standards stabilize and volumes increase, it is important to have a solution with a low-cost migration path. Often this means either market-focused ASSPs or standard-cell custom ASIC devices. However, the rising cost of custom silicon makes those solutions economically feasible in only the highest volume consumer applications. Most silicon companies with a focus on video and imaging target applications such as video camcorders, set-top boxes, digital still cameras, cell phones and other portable products, or LCD TVs and monitors. Therefore, when designing a lower-volume type of application, it is best to consider an FPGA, as it is unlikely an ASSP with the exact feature set required exists and even the best off-the-shelf solution is a risky choice due to the high potential for obsolescence.

Altera's Video and Image Processing Solution

For the reasons described above, FPGAs are particularly well suited to meet the requirements of many video and image processing applications. Altera® FPGAs have the following characteristics that make them very appealing for video and image processing architectures:

- *High performance:* HD processing can be implemented in a single Altera FPGA.
- *Flexibility:* Altera FPGAs provide the ability to upgrade architectures quickly to meet evolving requirements, while scalability allows use of FPGAs in low-cost and high-performance systems.
- *Low development cost:* Video development kits from Altera start as low as US$1,095 and include the software tools required to develop a video system using Altera FPGAs.
- *Obsolescence proof:* Altera FPGAs have a very large customer base who ship products for many years after introduction. Also, FPGA designs are easily migrated from one process node to the next.
- *Structured ASIC migration path to low costs:* Altera structured ASICs start at US$15 at 100ku for 1 million ASIC gates.
- *Altera's Video and Image Processing Solution:* This includes optimized DSP Design Flows, Altera's Video and Image Processing Suite, and interface and third-party video compression IP, and video reference designs.

ASSP-Like Functionality on FPGA/Structured ASICs

With a growing number of solutions, Altera and its partners provide ASSP functionality in the form of an FPGA or structured ASIC. An example of this is ATEME's H.264 Main Profile Standard Definition Encoder product. With this product, customers use FPGAs just as they do an ASSP. The benefit over the traditional ASSP approach is that the FPGA solution evolves quickly, with no risk of obsolescence.

DSP Design Flow

For custom development, Altera provides an optimized DSP design flow that allows several different ways to represent the design. These include VHDL/Verilog, model-based design, and C-based design. Altera's Video and Image Processing Suite of cores can be used in conjunction with any of these design flow options.

Altera and The MathWorks have joined forces to create a comprehensive DSP development flow that allows designers to enjoy the price/performance benefits of Altera FPGAs while leveraging Simulink, The MathWorks's model-based design tool. Altera's DSP Builder is a DSP development tool that connects Simulink with Altera's industry-leading Quartus® II development software. DSP Builder provides a seamless design flow in which designers perform algorithmic development in the MATLAB software and system-level design in the Simulink software, and then port the design to hardware description language (HDL) files for use in the Quartus II software. The DSP Builder tool is tightly integrated with the SOPC Builder tool, allowing the user to build systems that incorporate Simulink designs and Altera embedded processor and intellectual property cores. This development flow is easy and intuitive for designers who do not have extensive experience using programmable logic design software.

Video and Image Processing Suite

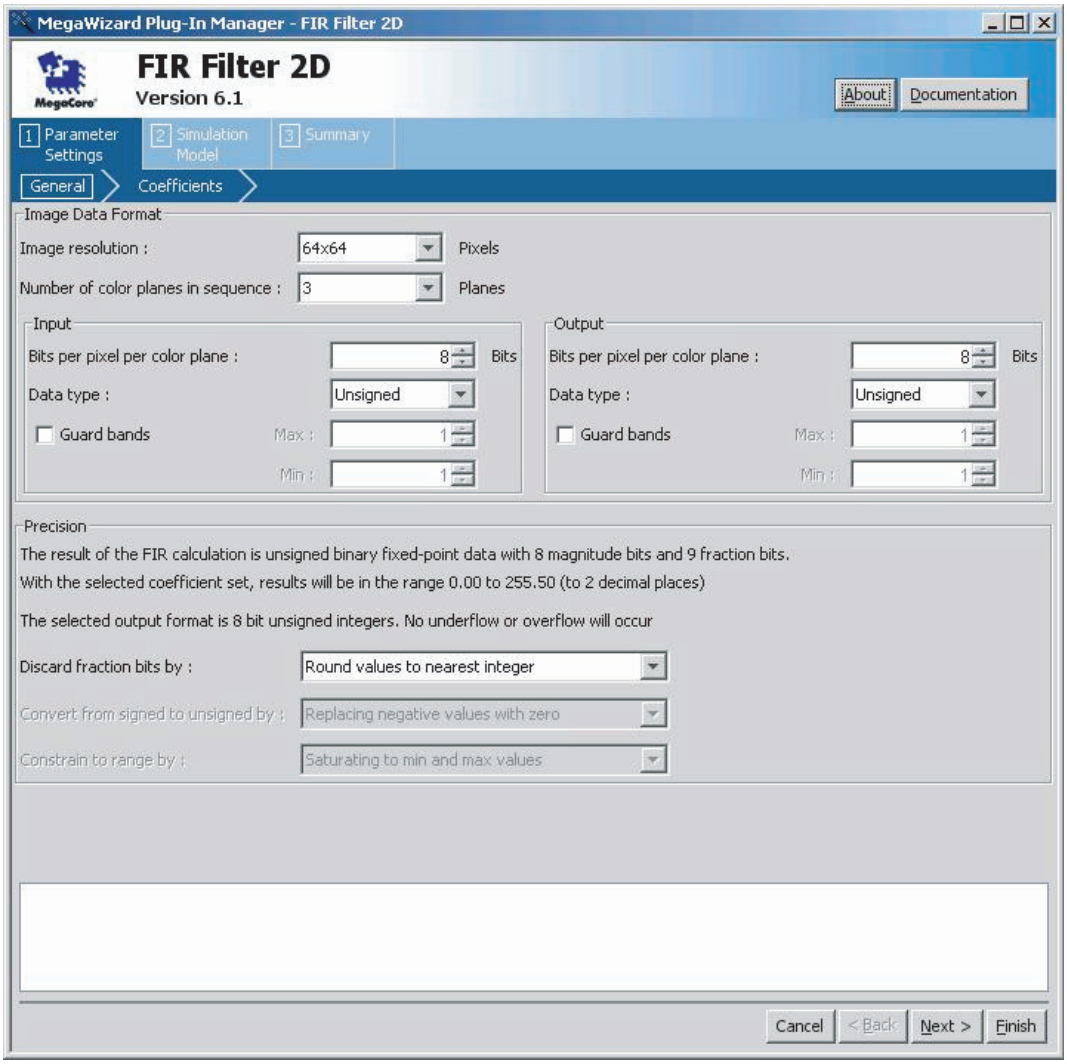
The Video and Image Processing Suite consists of nine functions with parameters that can be statically, or in some cases, dynamically changed. Table 2 summarizes these functions.

Table 2. Functions Available With the Video and Image Processing Suite

Function	Description
De-Interlacer	Converts interlaced video formats to progressive video format
Color Space Converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Alpha Blending Mixer	Mixes and blends multiple image streams
Gamma Corrector	Performs gamma correction on a color plane/space
Chroma Resampler	Changes the sampling rate of the chroma data for image frames
2D Filter	Implements 3x3, 5x5, or 7x7 finite impulse response (FIR) filter operation on an image-data stream to smooth or sharpen images
2D Median Filter	Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line Buffer Compiler	Efficiently maps image line buffers to Altera on-chip memories

The 2D Filter GUI is shown in Figure 1 as an example of the type of user configuration that is available with the cores provided in the video and image processing suite. Resolutions, bits per sample, FIR filter size, edge behavior, overflow behavior, and accumulator length are all static parameters supported in the 2D filter core.

Figure 1. 2D Filter GUI



Video Compression

Several third parties have video compression solutions targeting Altera FPGAs and structured ASICs. Table 3 lists some of the common video compression standards and associated third parties.

Table 3. Third-Party Video Compression Solutions

Function	Company
H.264 Main and High Profile	ATEME
H.264 Baseline Profile	CAST, W&W
JPEG/JPEG2000	Barco, Broadmotion, CAST
MPEG4 SP/ASP	Barco, CAST

Video Interfaces and System IP

Altera and its partners also provide interface cores that are often required in a video system. These include ASI, SDI, 10/100/1000 Ethernet, and DDR/DDR2 Memory Controllers. Table 4 has a partial listing of these types of cores and reference designs.

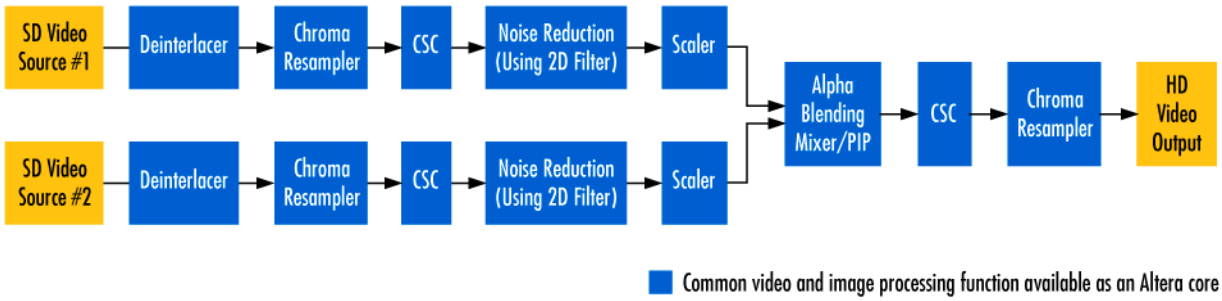
Table 4. Video Interfaces and System IP

Function	Company
10/100/1000 Ethernet	Altera, MorethanIP
DDR/DDR2 Memory Controllers	Altera
32-bit RISC Processor	Altera (Nios® II processor)
SRIO Interface to External Processors	Altera
TI EMIF Interface	Altera Reference Design
ATA Hard Disk Drive Interface	Nuvation
NOR Flash	Altera
Compact Flash and SD Interfaces	Altera
Video Over IP	Altera Reference Design
ASI	Altera
SDI	Altera

Example Video Design

A typical video system using the Video and Image Processing Suite is shown in Figure 2.

Figure 2. Example Design Block Diagram



Benchmarks

Table 5 and Table 6 show example functions and the corresponding FPGAs required for implementation.

Altera's Cyclone III low-cost FPGAs incorporate up to 4 Mbits of embedded memory, 488 embedded 9x9 multipliers at 260 MHz, and 120,000 LEs. The Cyclone III EP3C40 device is a midrange FPGA in the family and is priced at under US$20 for 250,000 units.

Stratix II high-performance, high-density devices incorporate up to 9 Mbits of embedded memory, 768 9x9 embedded multipliers at 450 MHz, and 179,000 LEs. These functions also can be implemented in Altera's HardCopy® II structured ASIC devices.

Table 5. Encoding Standard Benchmarks

Encoding Standard	FPGA Implementation
H.264 Baseline Profile SD Encoding	Cyclone III EP3C40 *(1)*
H.264 Baseline Profile 1280x1024 Encoding	Stratix II EP2S30 *(1)*
H.264 Main Profile SD Encoding	Stratix II EP2S130
H.264 High Profile 720p Encoding	Multiple Stratix II FPGAs
JPGE2000 Digital Cinema Encoding (2k)	Stratix II EP2S130

Note:
(1) Significant logic, memory, and DSP resources left for pre- and postprocessing functions

Table 6. Pre- and Postprocessing Benchmarks

Pre- and Postprocessing	FPGA Implementation
5x5 2D Filter for 720p	Cyclone III EP3C10
5x5 2D Median Filter for 720p	Cyclone III EP3C10
Linear Interpolation Scaler for SD to 720p	Cyclone III EP3C5

Conclusion

FPGAs are great fits for video and image processing applications, such as broadcast infrastructure, medical imaging, HD videoconferencing, video surveillance, and military imaging. Video and image processing solutions for Altera FPGAs include optimized development tools and kits, reference designs, video compression IP, and interface and system IP, as well as Altera's video and image processing IP suite. These solutions can improve cost, performance, and productivity for many video and imaging applications.

Further Information

- Altera's Video and Image Processing Solutions website:
  www.altera.com/video_imaging
- Video Processing Reference Design:
  www.altera.com/end-markets/refdesigns/sys-sol/broadcast/ref-post-processing.html

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