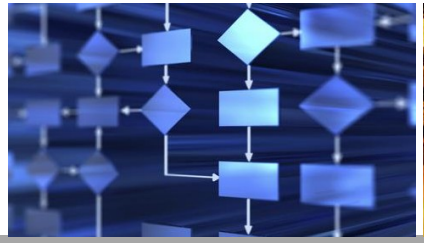
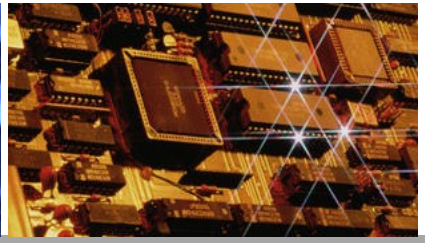
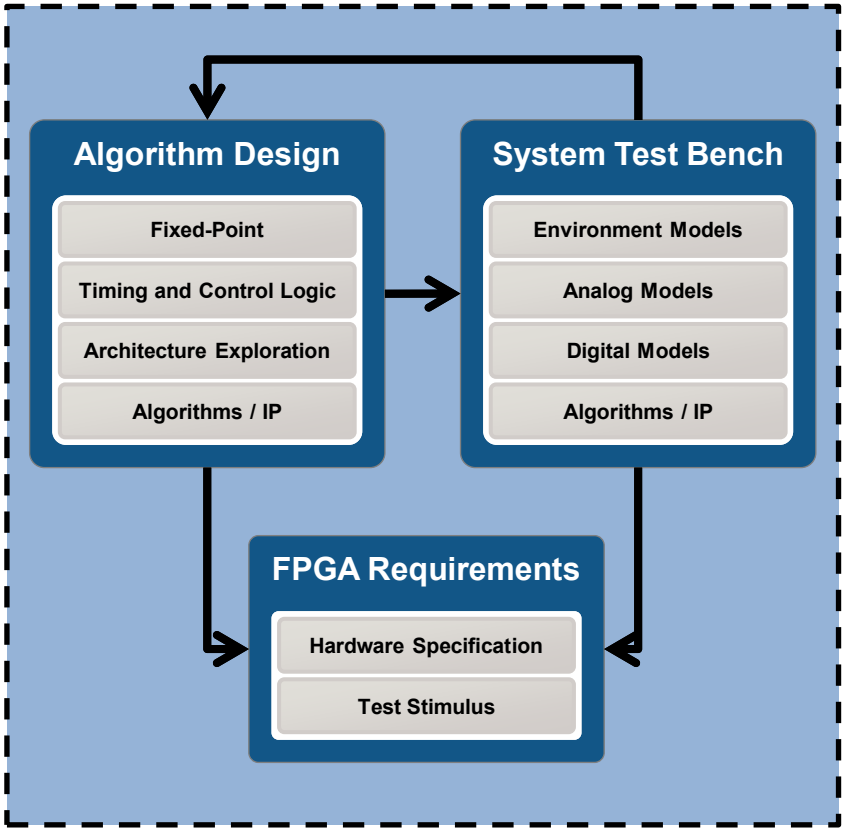
Model-Based Design for Altera FPGAs Using HDL Code Generation

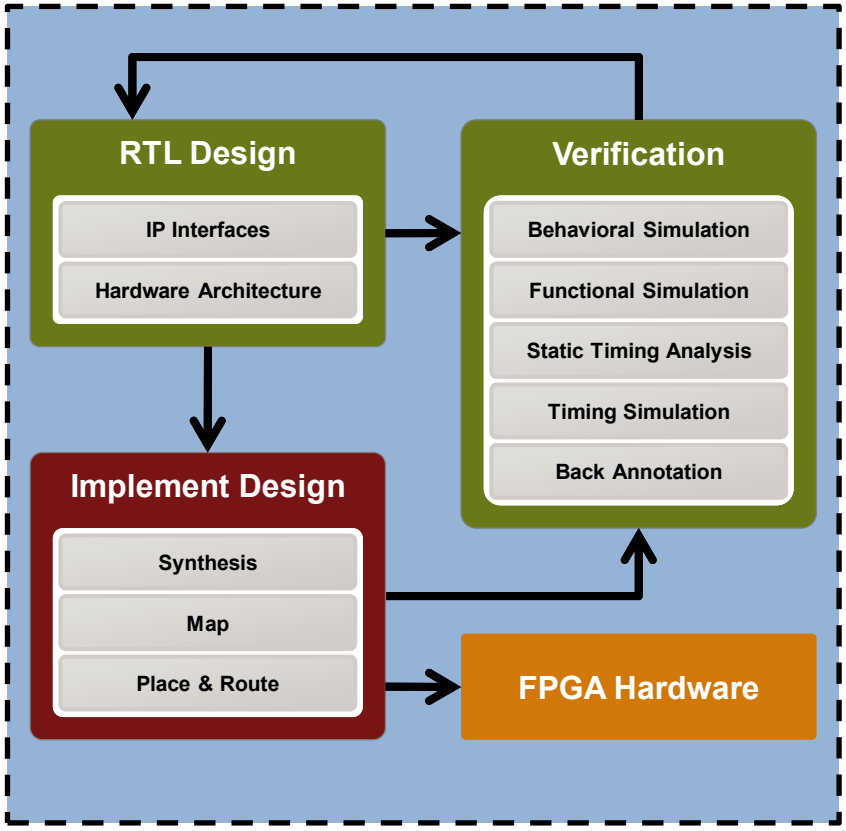

Z

Separate Views of DSP Implementation

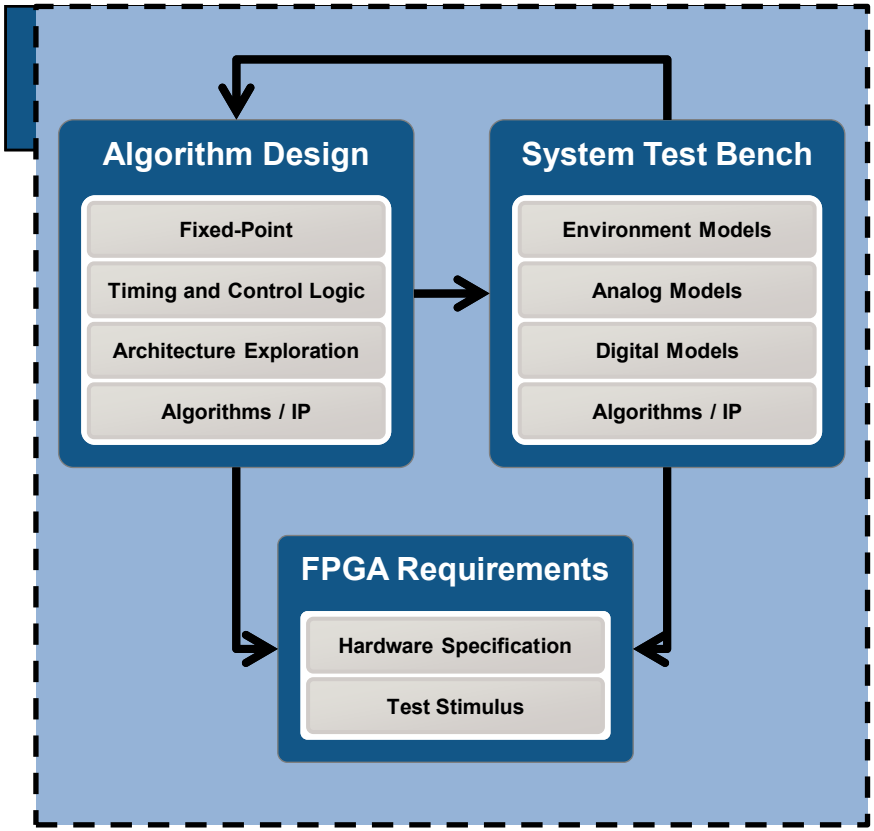
System Designer

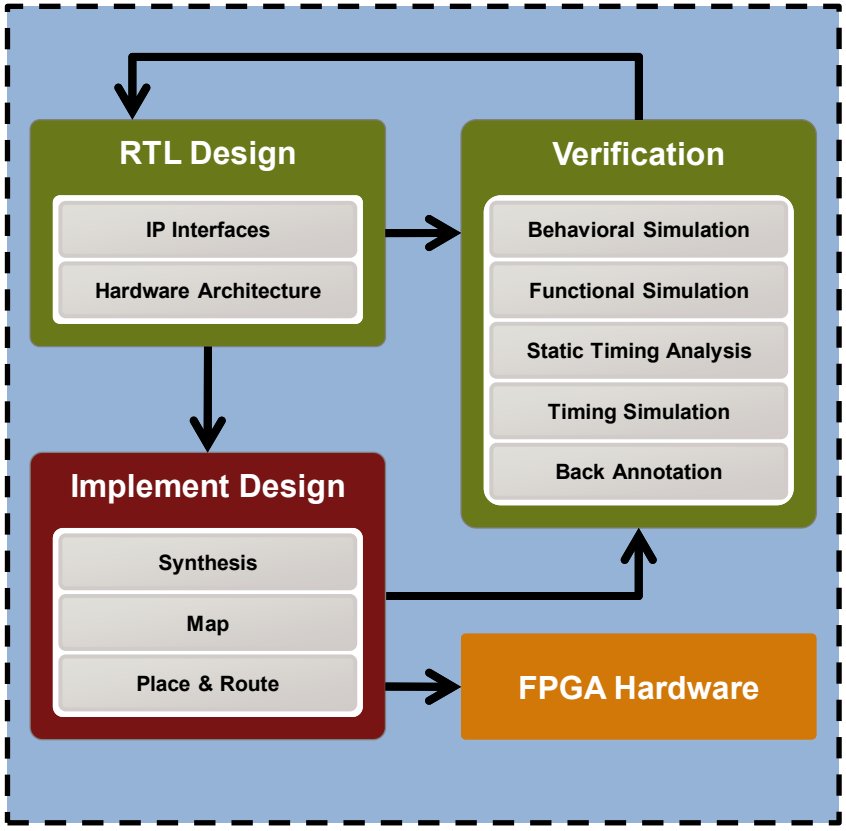


FPGA Designer

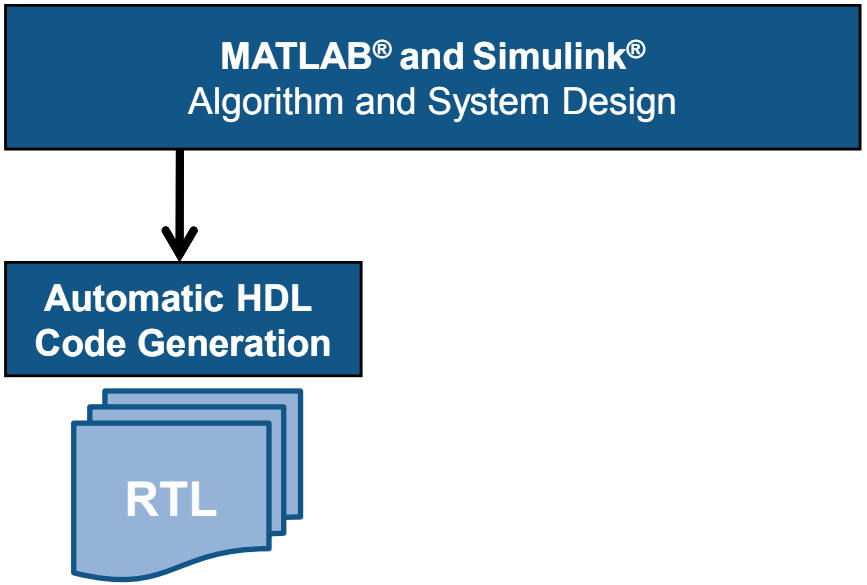


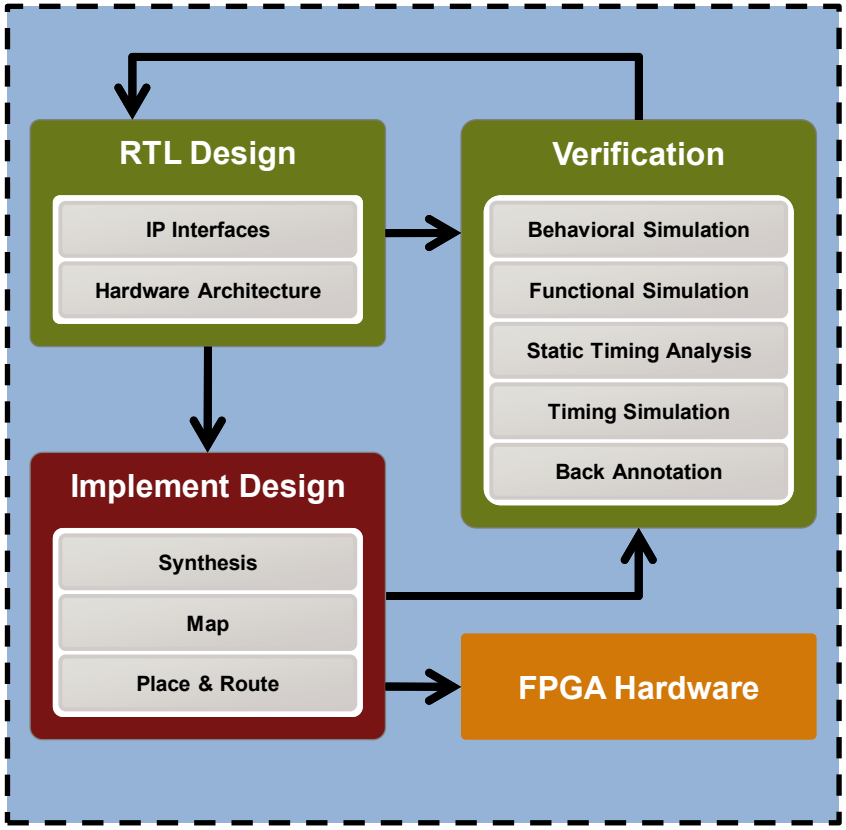
Model Based Design for Implementation



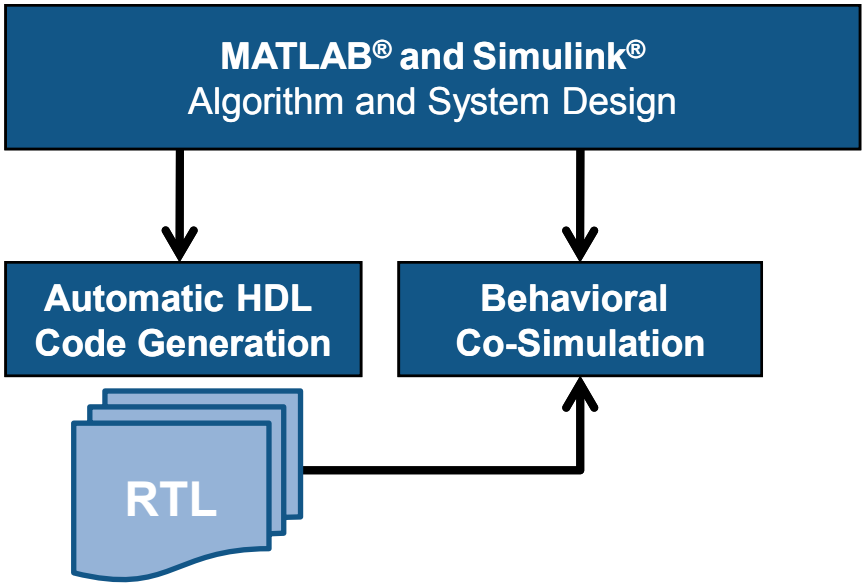


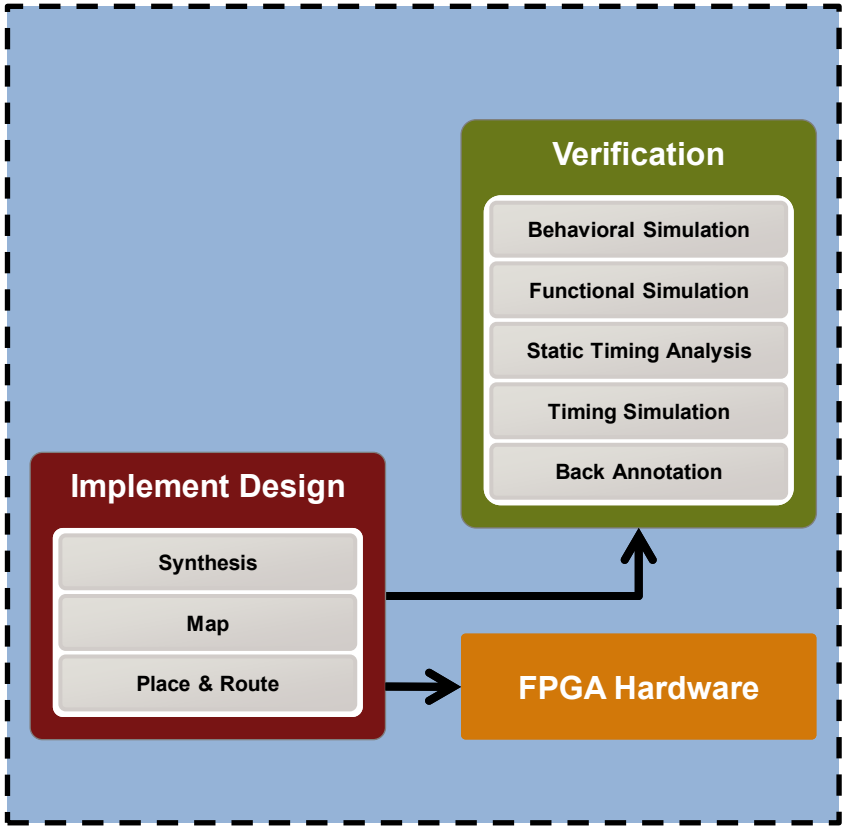
Model Based Design for Implementation



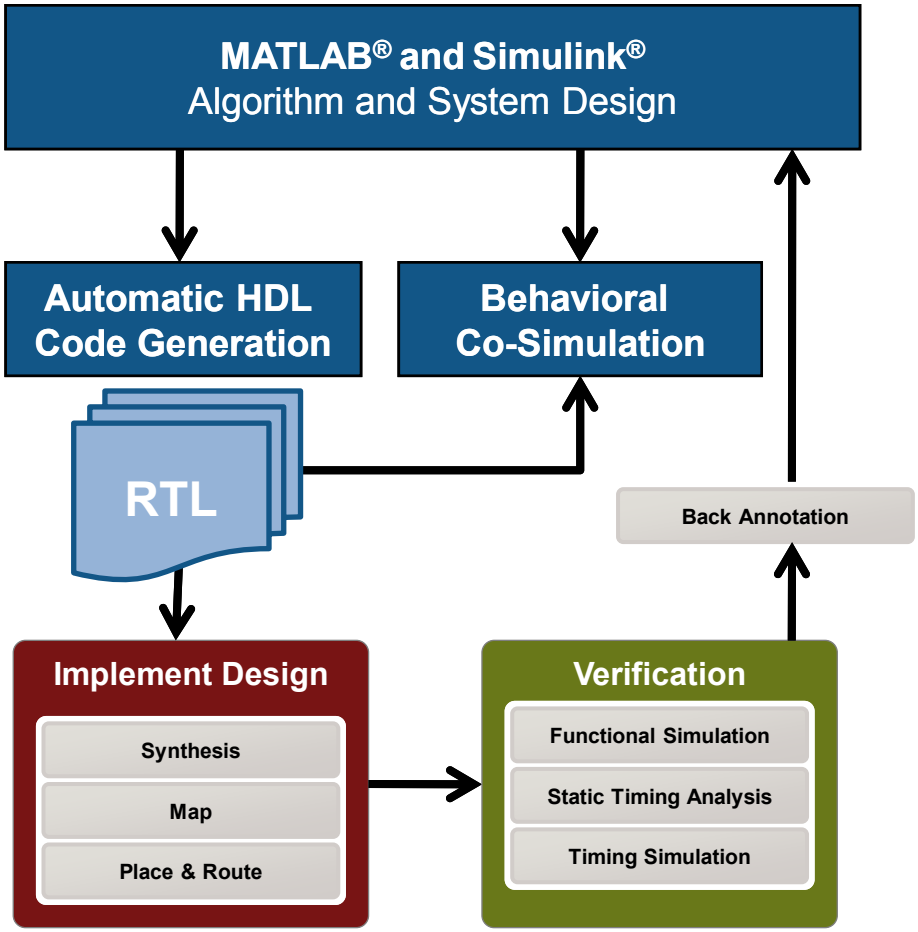


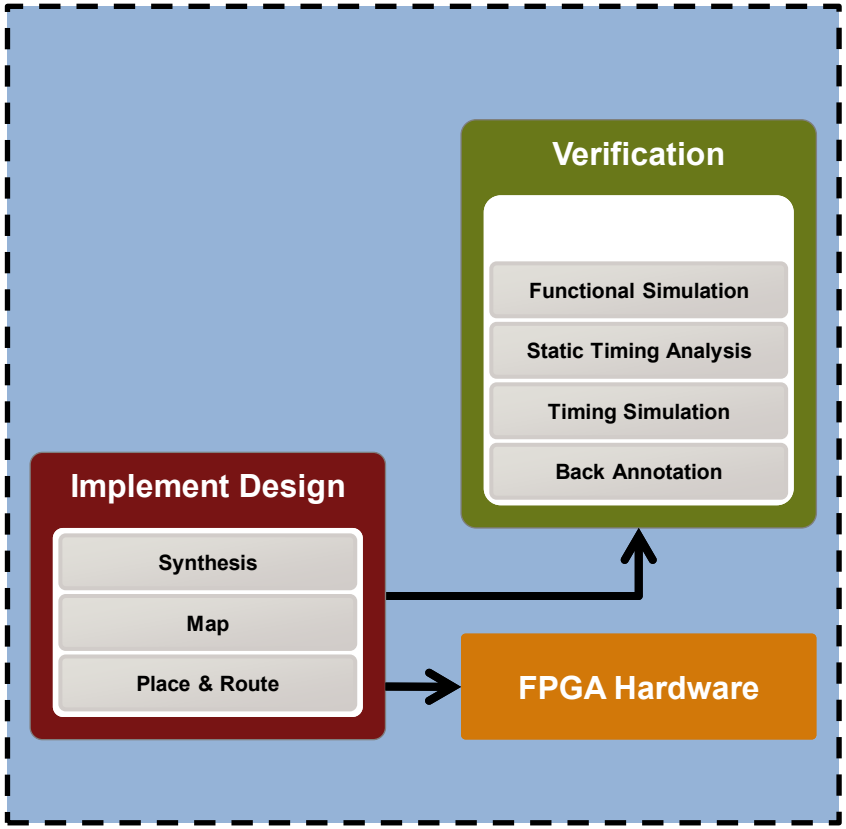
Model Based Design for Implementation



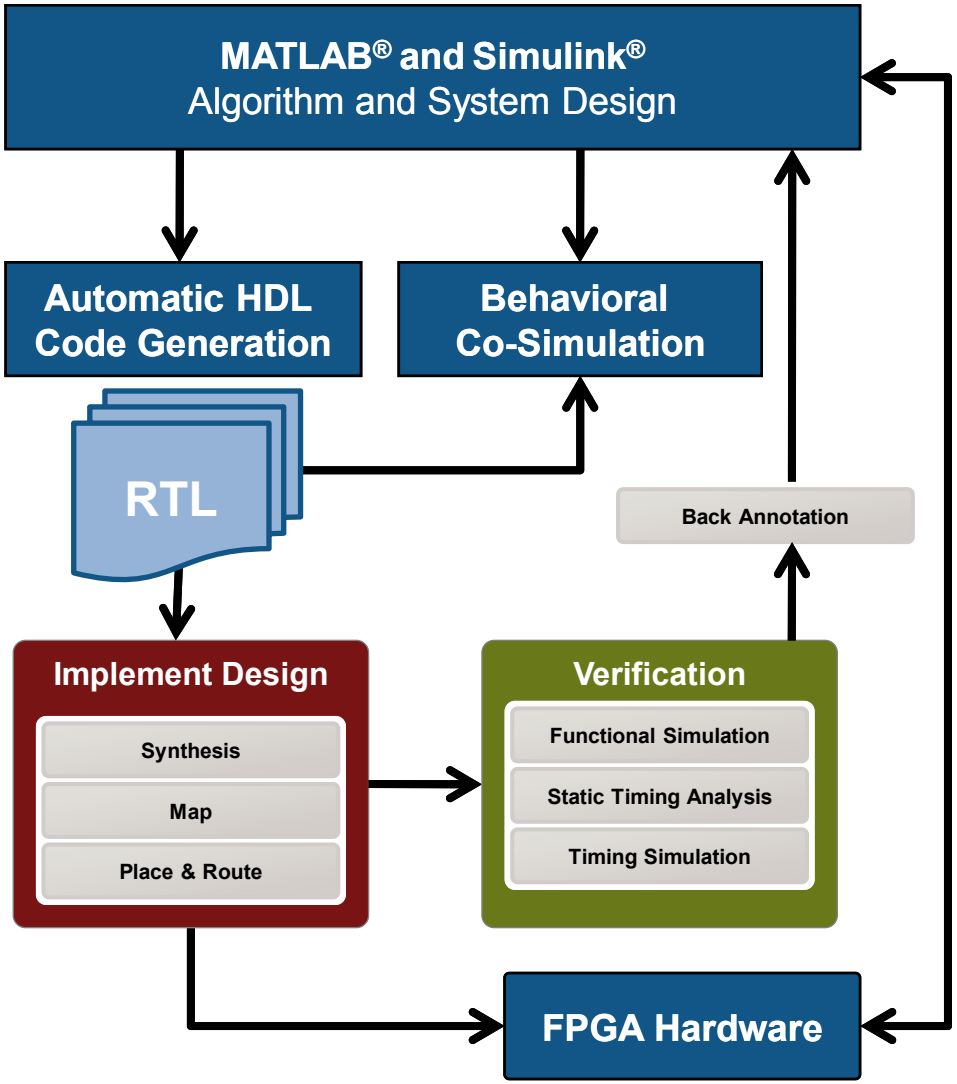


Model Based Design for Implementation



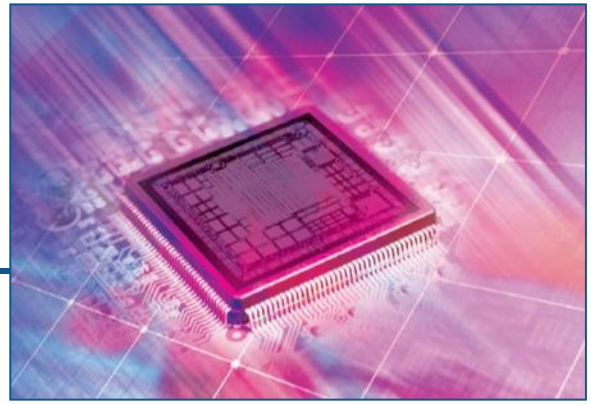


Model Based Design for Implementation



FPGA Hardware

Faraday Accelerates SIP Development and Shrinks NAND Flash Controller ECC Engine Gate Count by 57%



Faraday's silicon IP on an SoC.

Challenge

Accelerate the development of SoCs and ASICs

Solution

Use MathWorks tools for Model-Based Design to speed up system-level simulations, improve system performance, and shorten time-to-market

Results

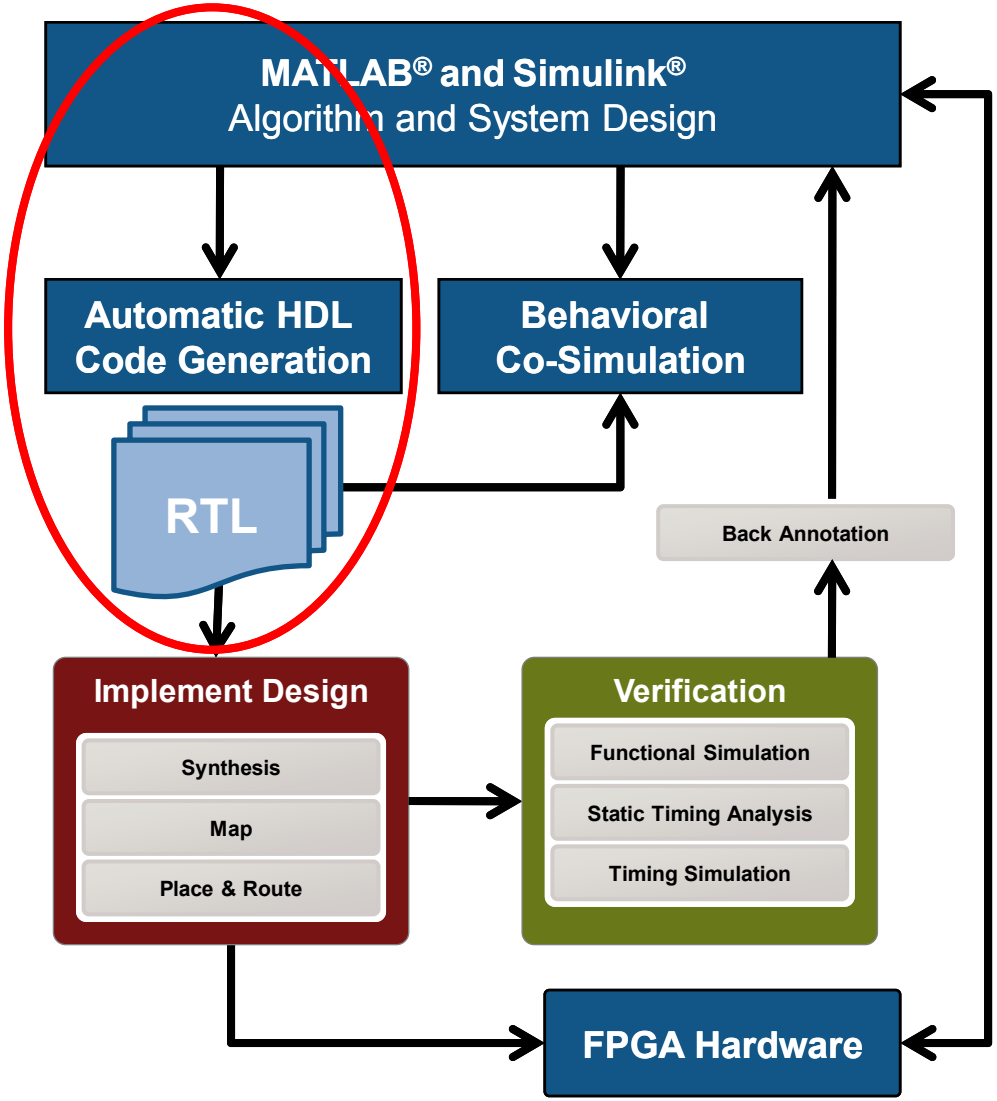
- Simulations 200 times faster
- Throughput performance increased by 15%
- Gate count cut by 57%

"The Simulink environment is ideal for system-level architecture exploration. The simulations are 200 times faster than they were in our previous workflow — and Simulink models can be easily converted to C as well as to HDL code, which enables high scalability and reusability."

Ken Chen
Faraday

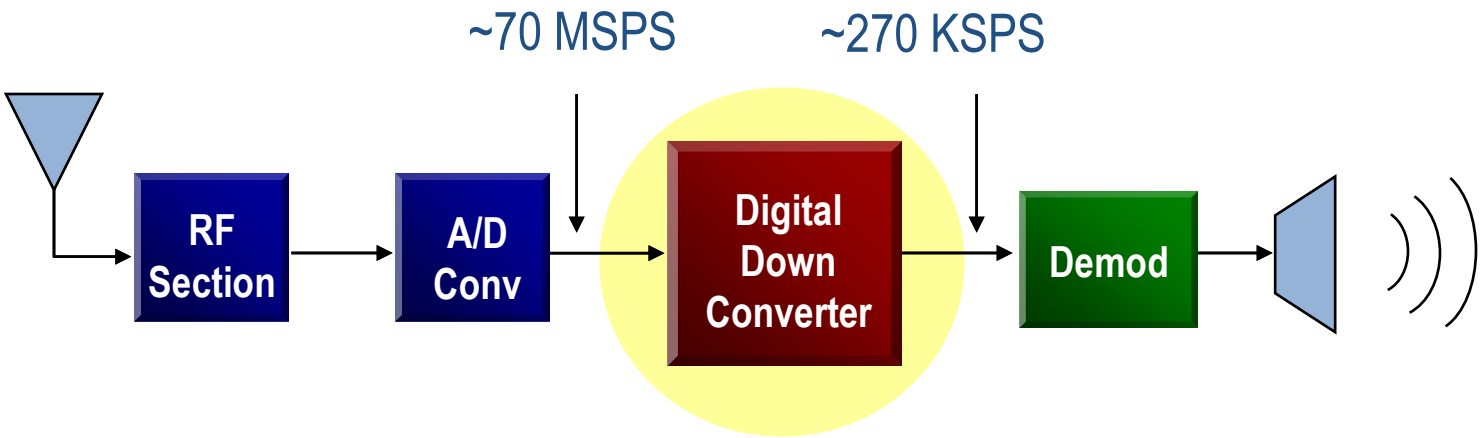
Link to user story

From Algorithm to Synthesizable RTL



Digital Down Converter

- DDC accepts
  - A high sample-rate passband signal (may be 50 to 100 Msps)
- DDC produces
  - A low sample-rate baseband signal ready for demodulation

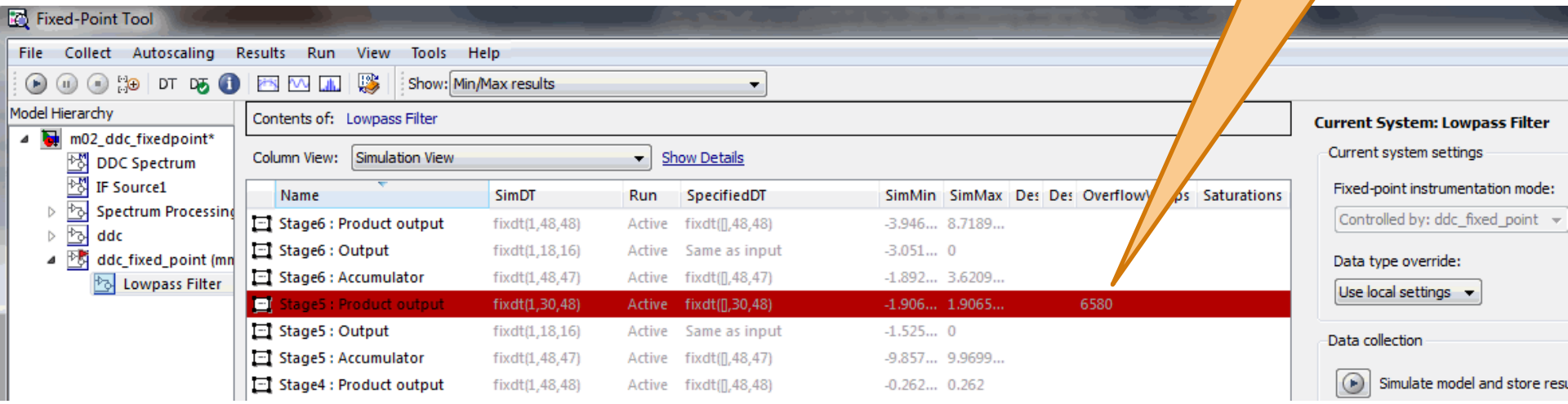


Fixed Point Analysis

Digital Down Converter

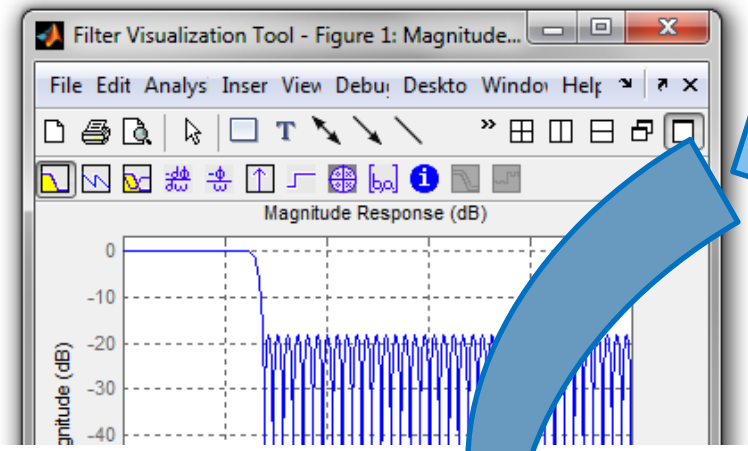
- Convert floating point to fixed point models
  - Automatic tracking of signal range (also intermediate quantities)
  - Fraction lengths recommendation
- Bit-true models in the same environment
  - Quantify the impact of fixed point quantization

Find and fix issues with fixed point easily

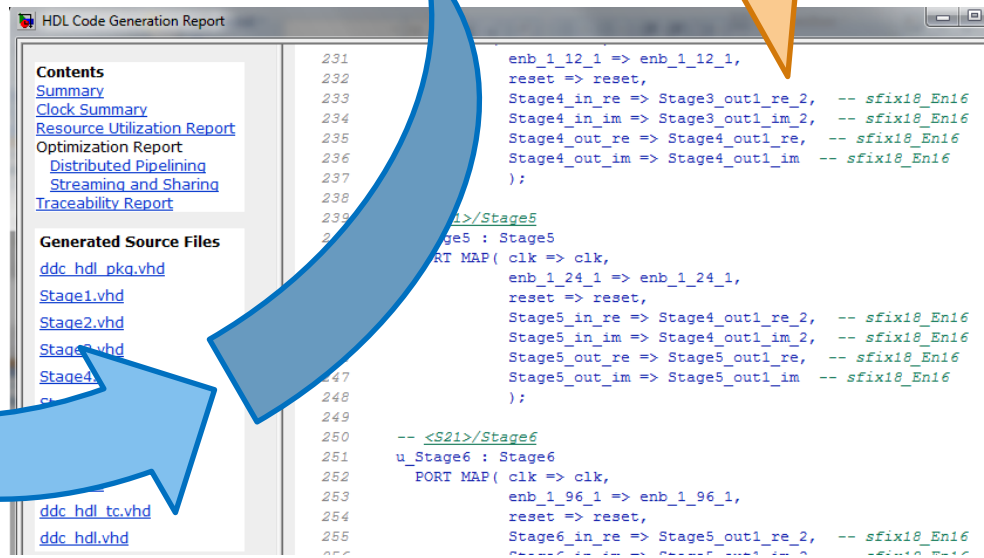


Automatic HDL Code Generation

Digital Down Converter

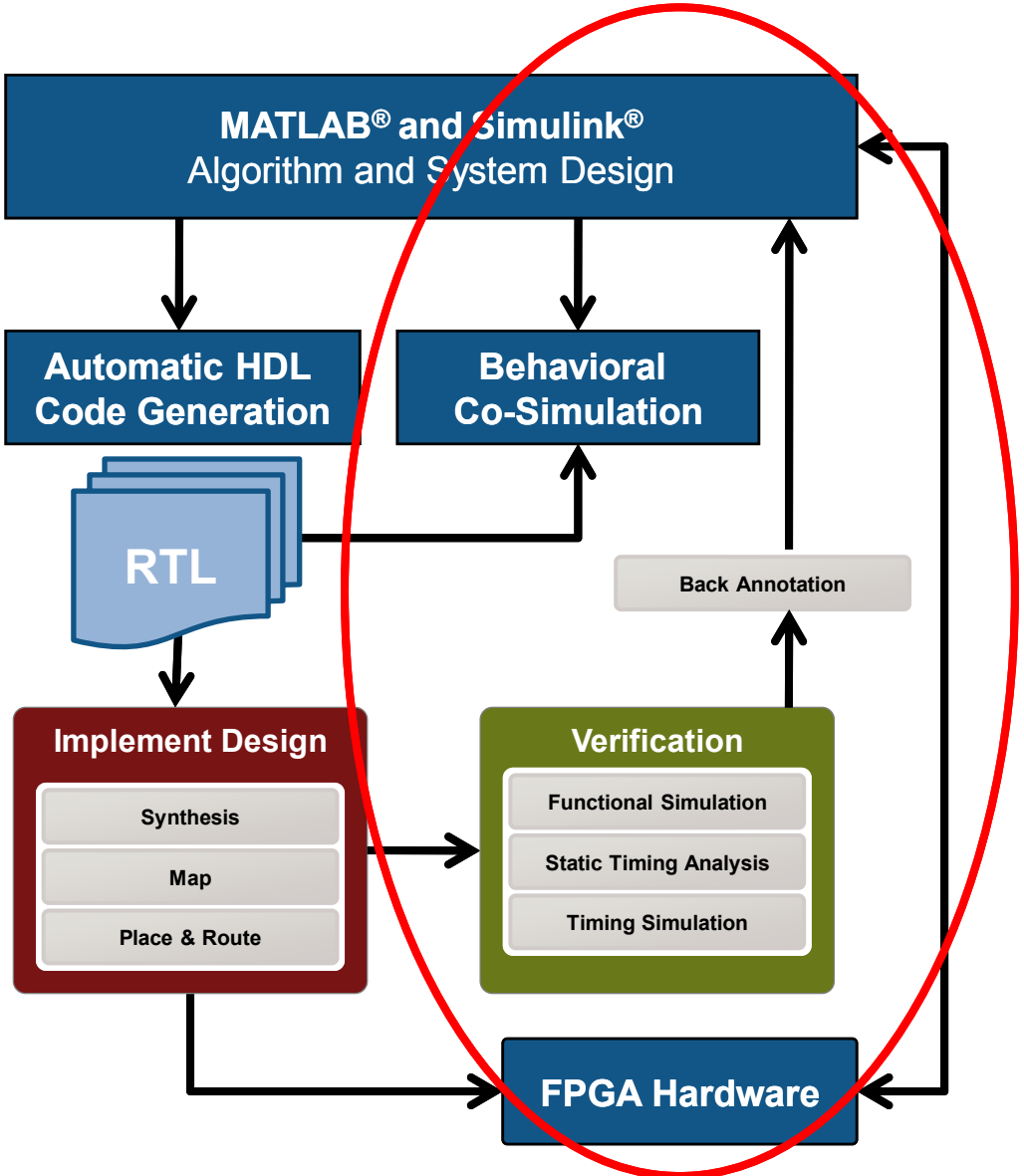


Automatically generate bit true, cycle accurate HDL code from Simulink, MATLAB and Stateflow



Full traceability between model and HDL code

Integrated HDL Verification

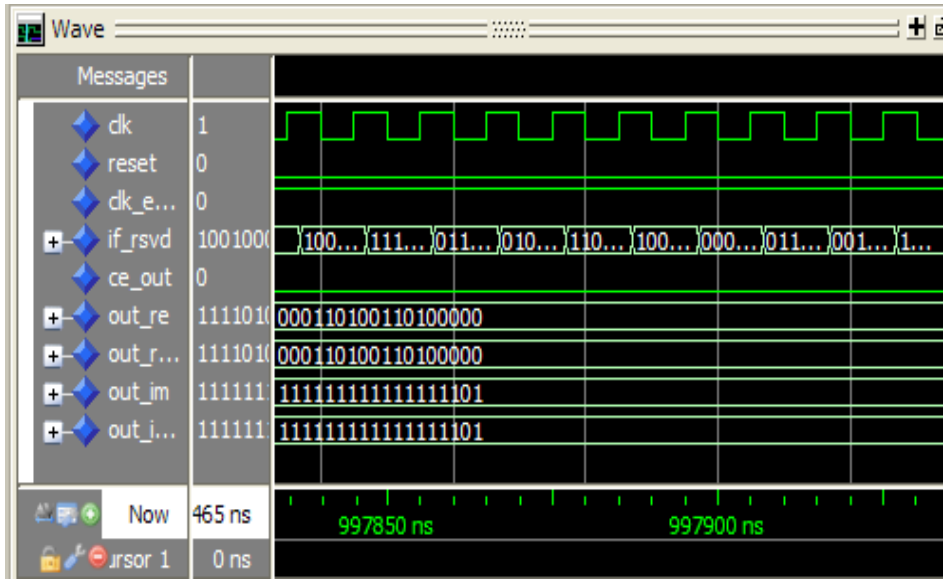


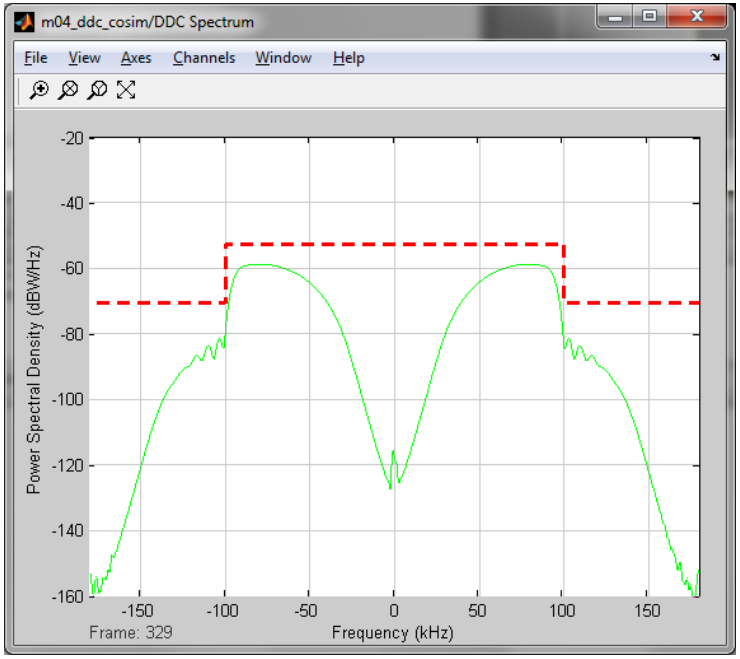
Verification Challenges:
HDL Verification

- Design the Test Bench twice
  - 10 – to – 1 ratio of Test bench LOC – to – Design LOC
- Many stimulus files from MATLAB
- These are ideal references which require pre- and post-processing
- How to analyze results?

Verification Challenges:

HDL Verification





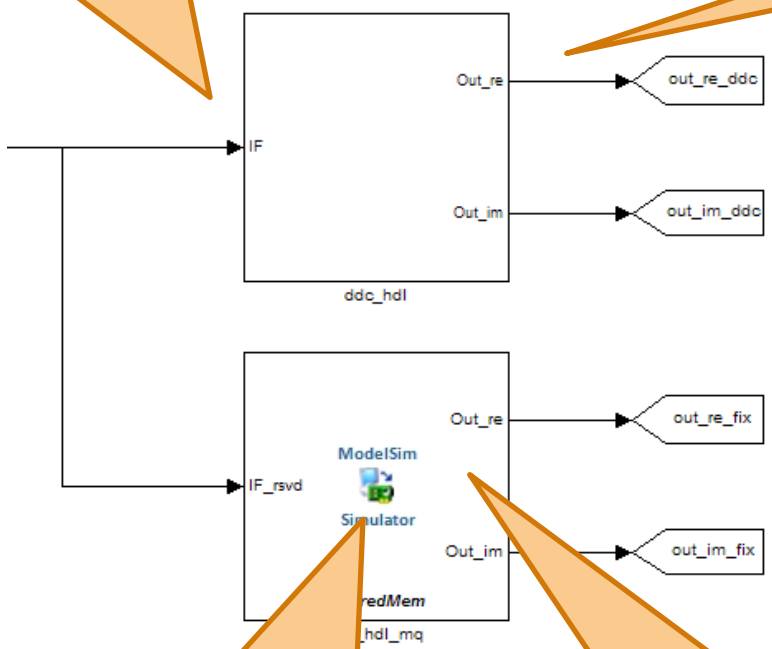
Demo: Re-Use System Level Test Bench

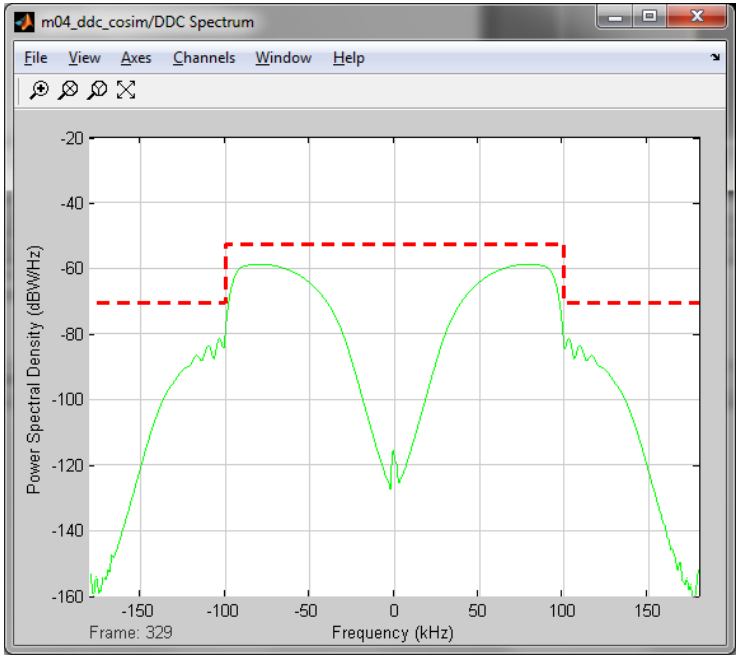
Co-Simulation with HDL simulators

Digital Down Converter

Re-use system level test bench

Flexible test bench creation in Simulink

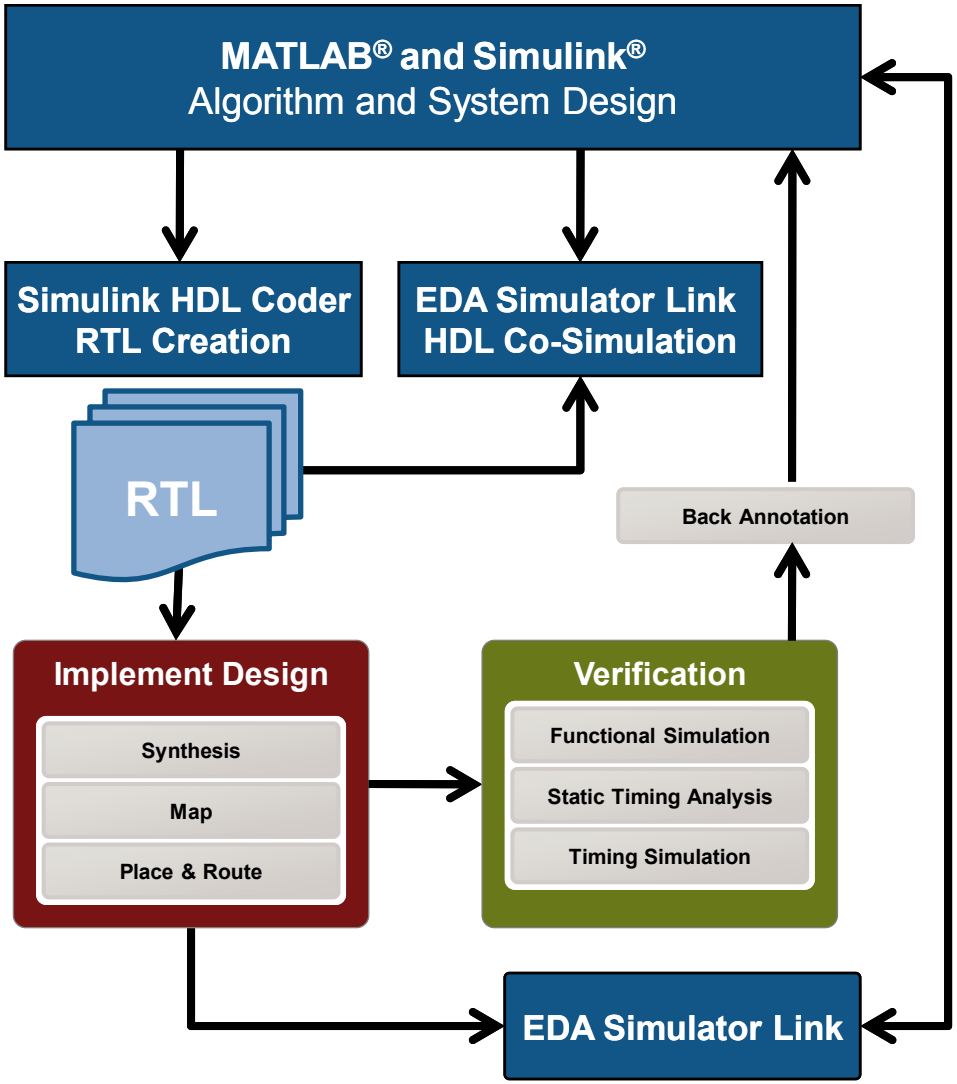




Direct simulation link to HDL Simulators

Automatically generated co-simulation models and Wizards for legacy HDL code

From Algorithm to FPGA Prototyping and Verification

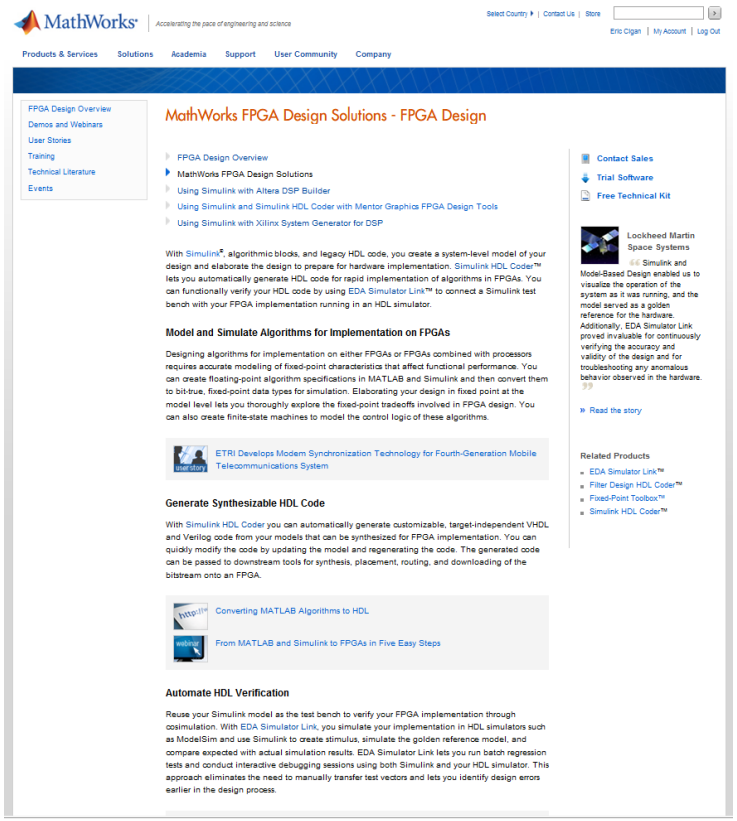


Next Steps …

1. Visit www.mathworks.com/fpga for more information

2. Watch our FPGA webinars: mathworks.com/company/events/webinars

3. Contact your local sales reps for a **trial** of MathWorks HDL code generation and verification products



Questions?