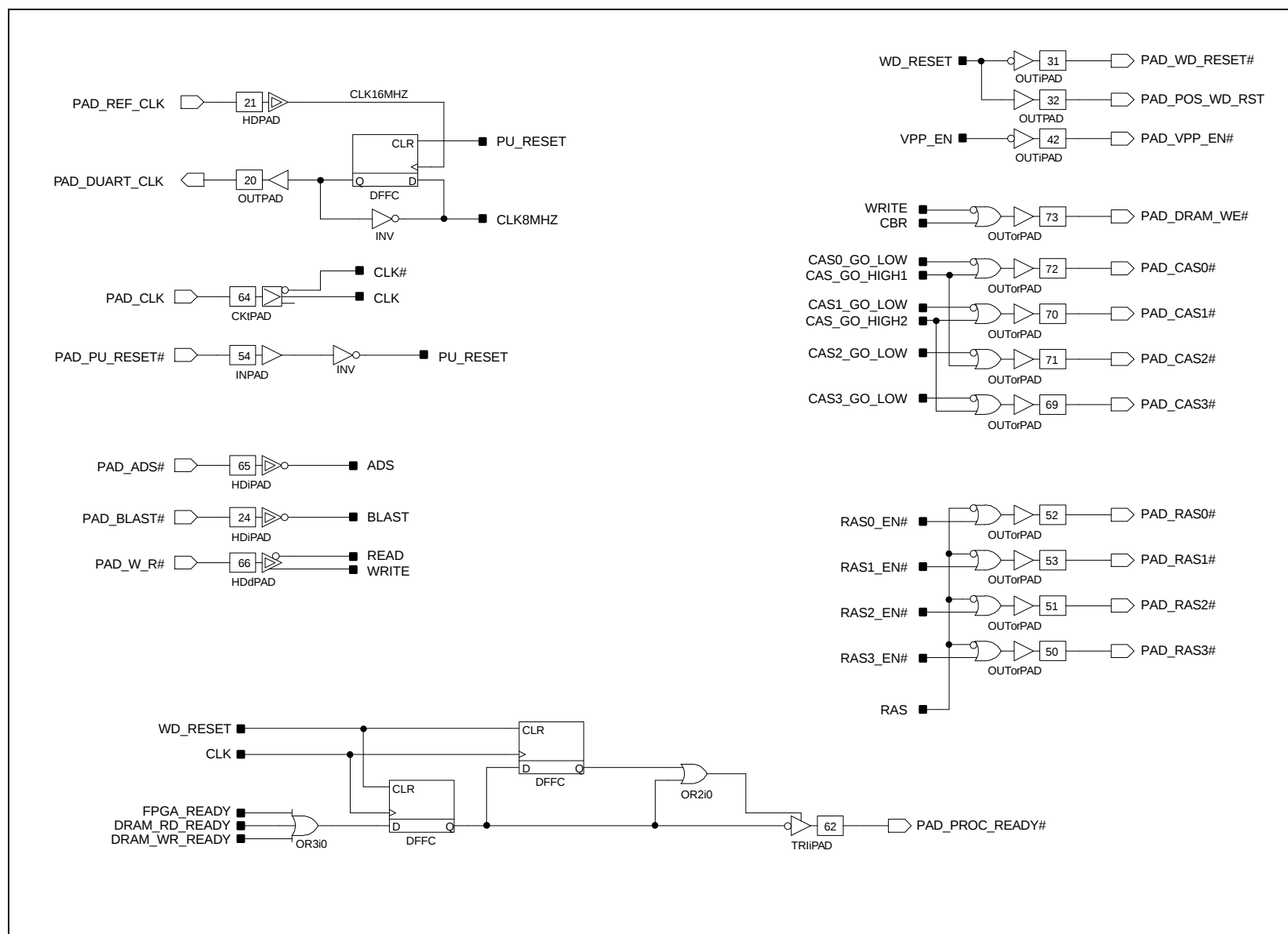
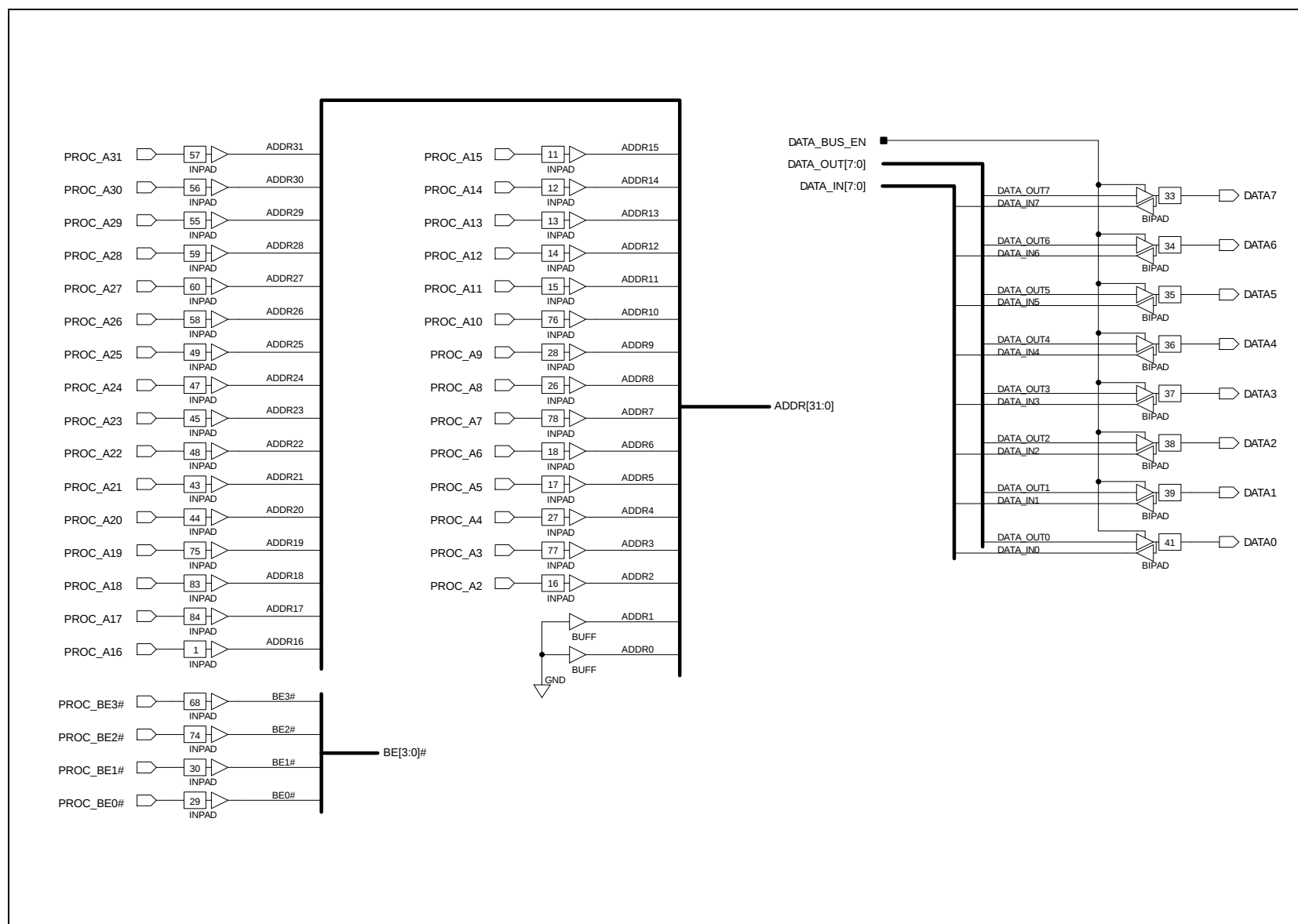


DRAM CONTROLLER FPGA SCHEMATICS



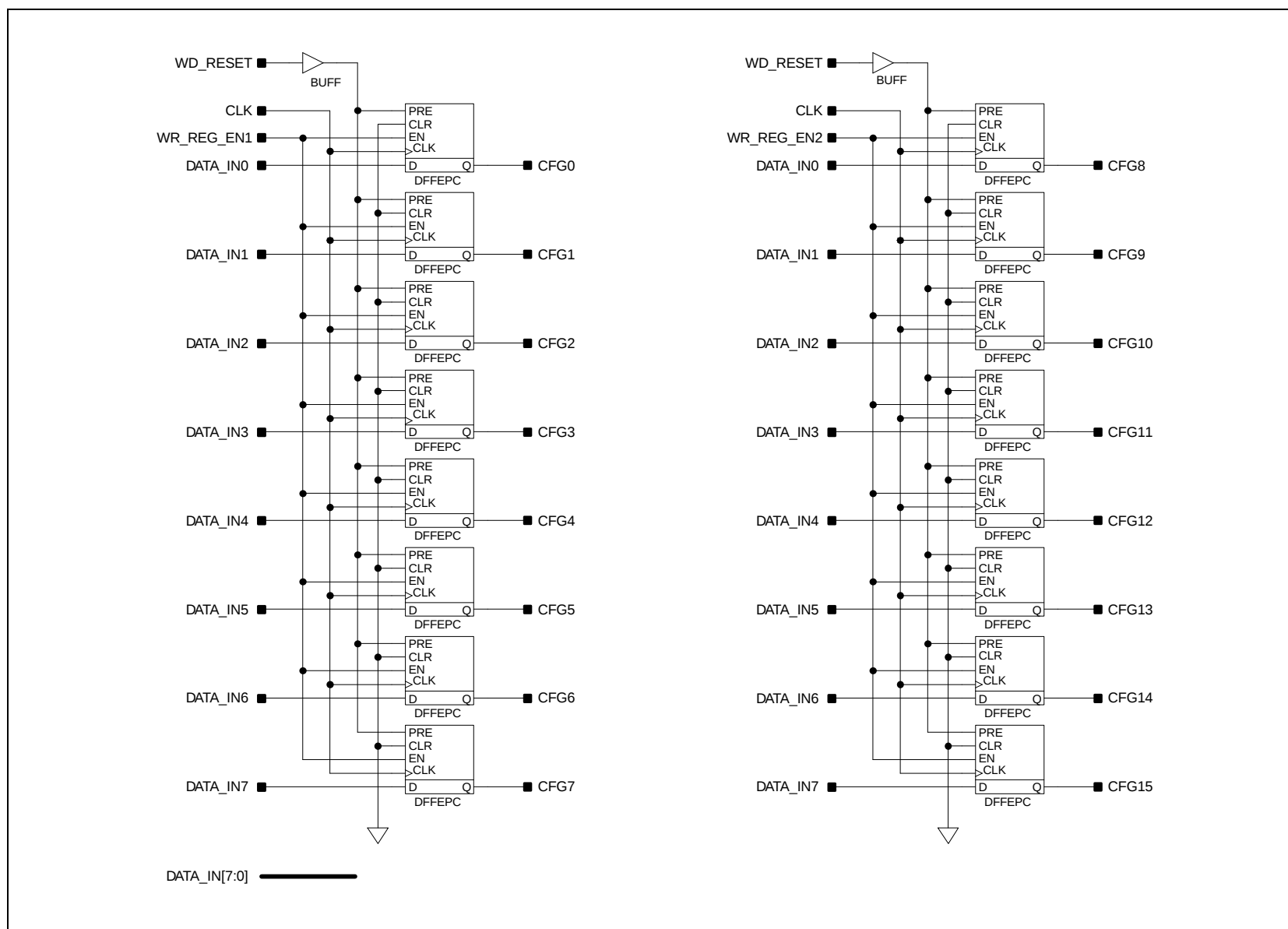


DRAM Controller FPGA Schematics—Sheet 1

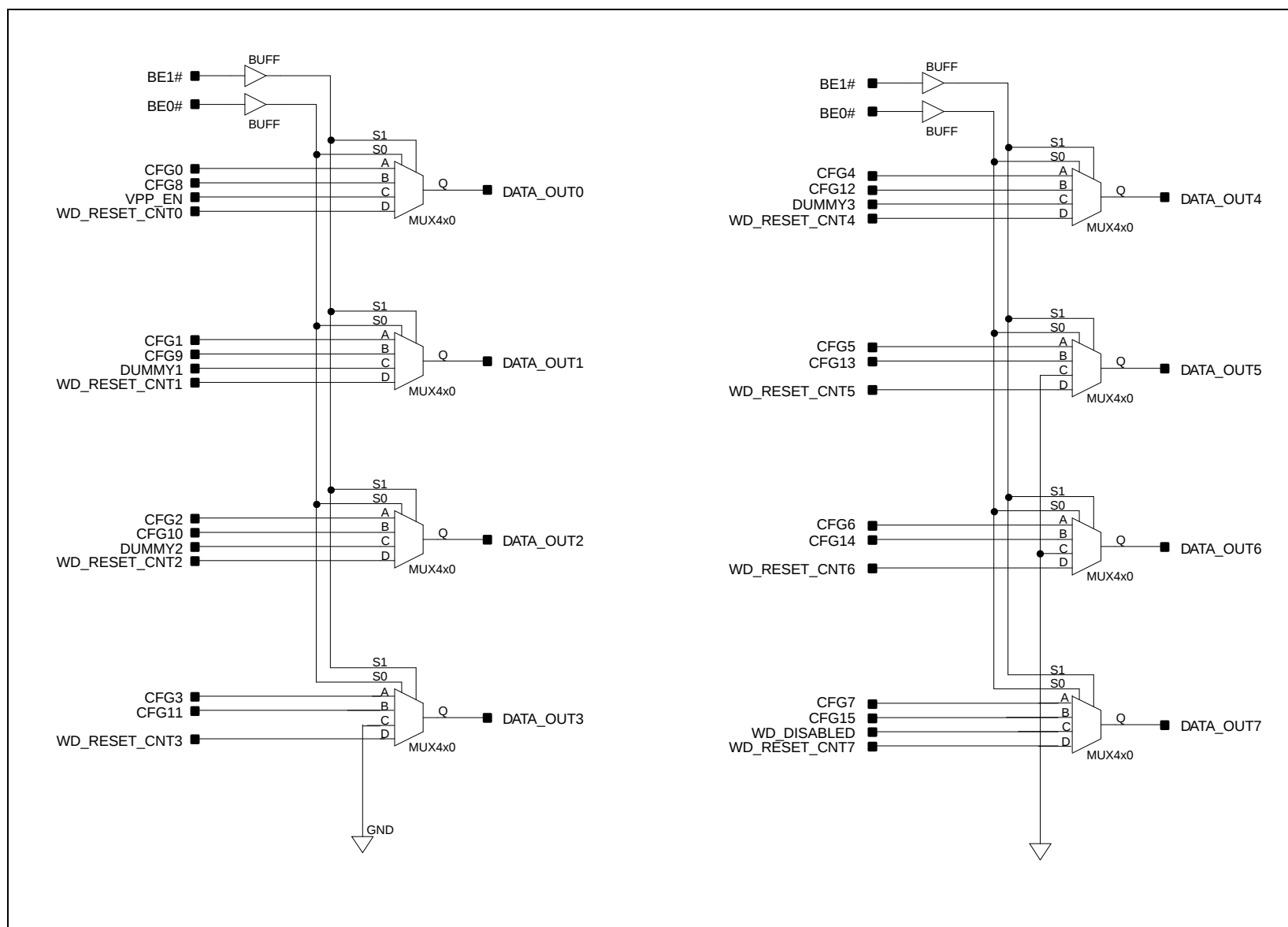


DRAM Controller FPGA Schematics—Sheet 2

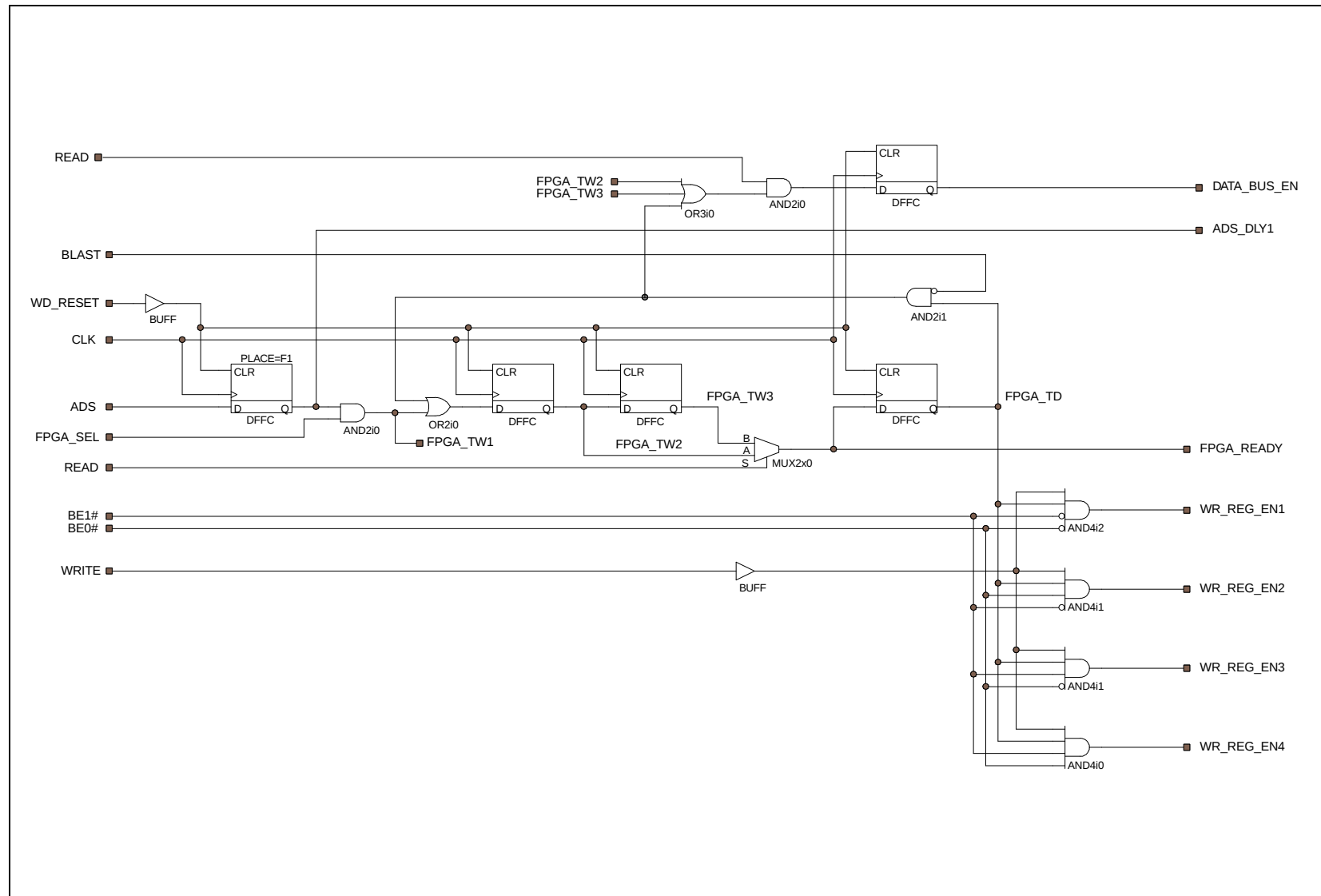




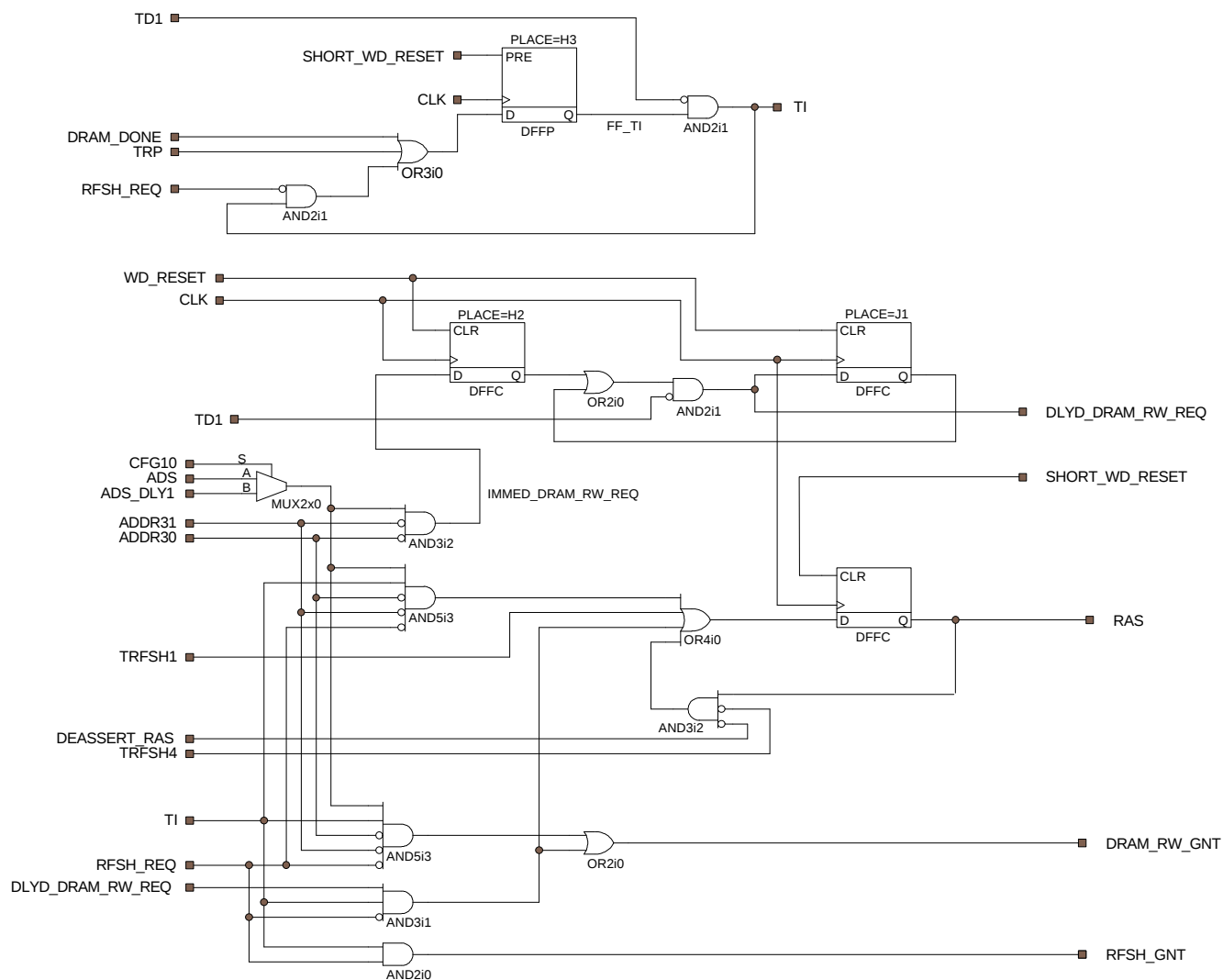
DRAM Controller FPGA Schematics—Sheet 4



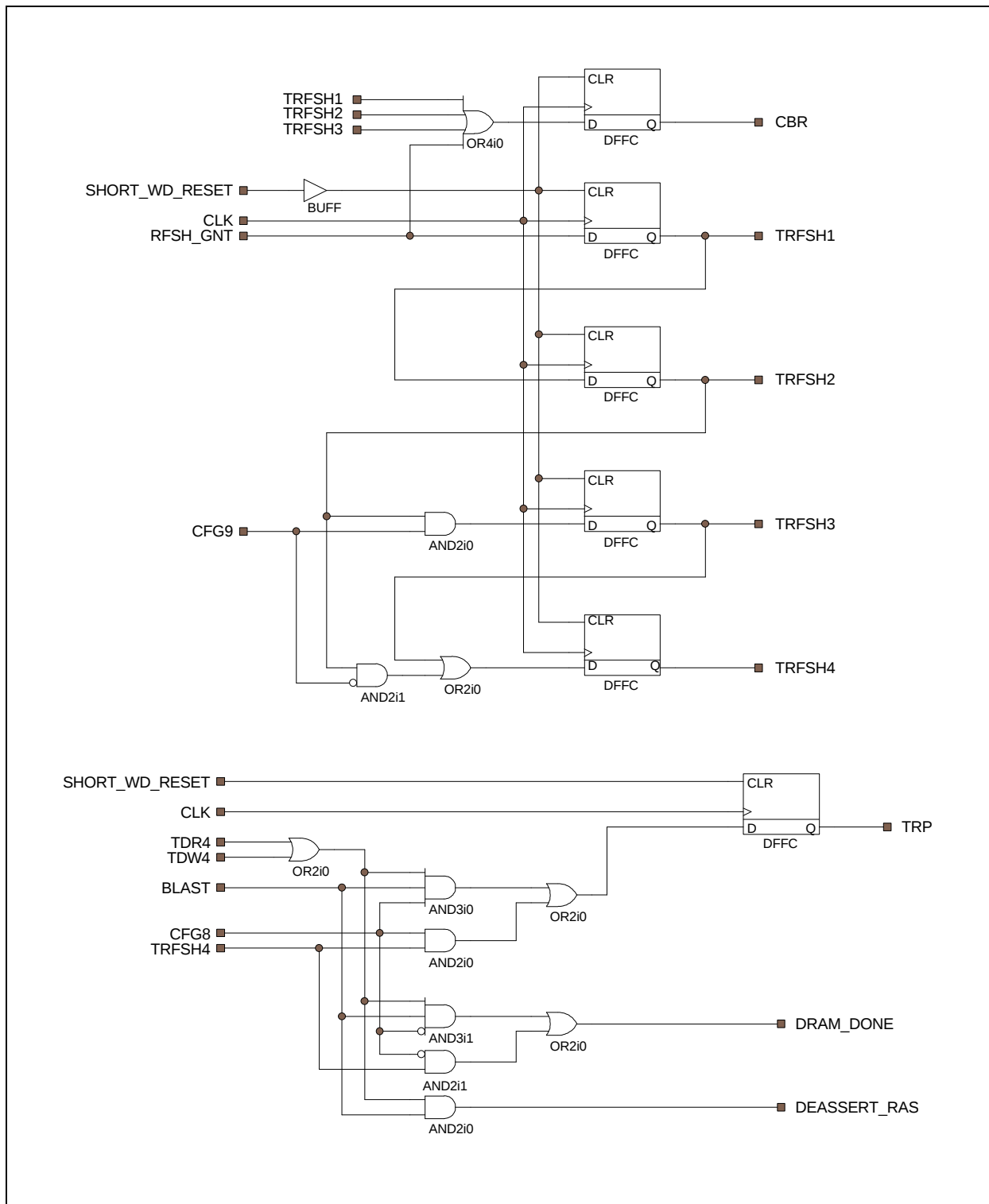
DRAM Controller FPGA Schematics—Sheet 5



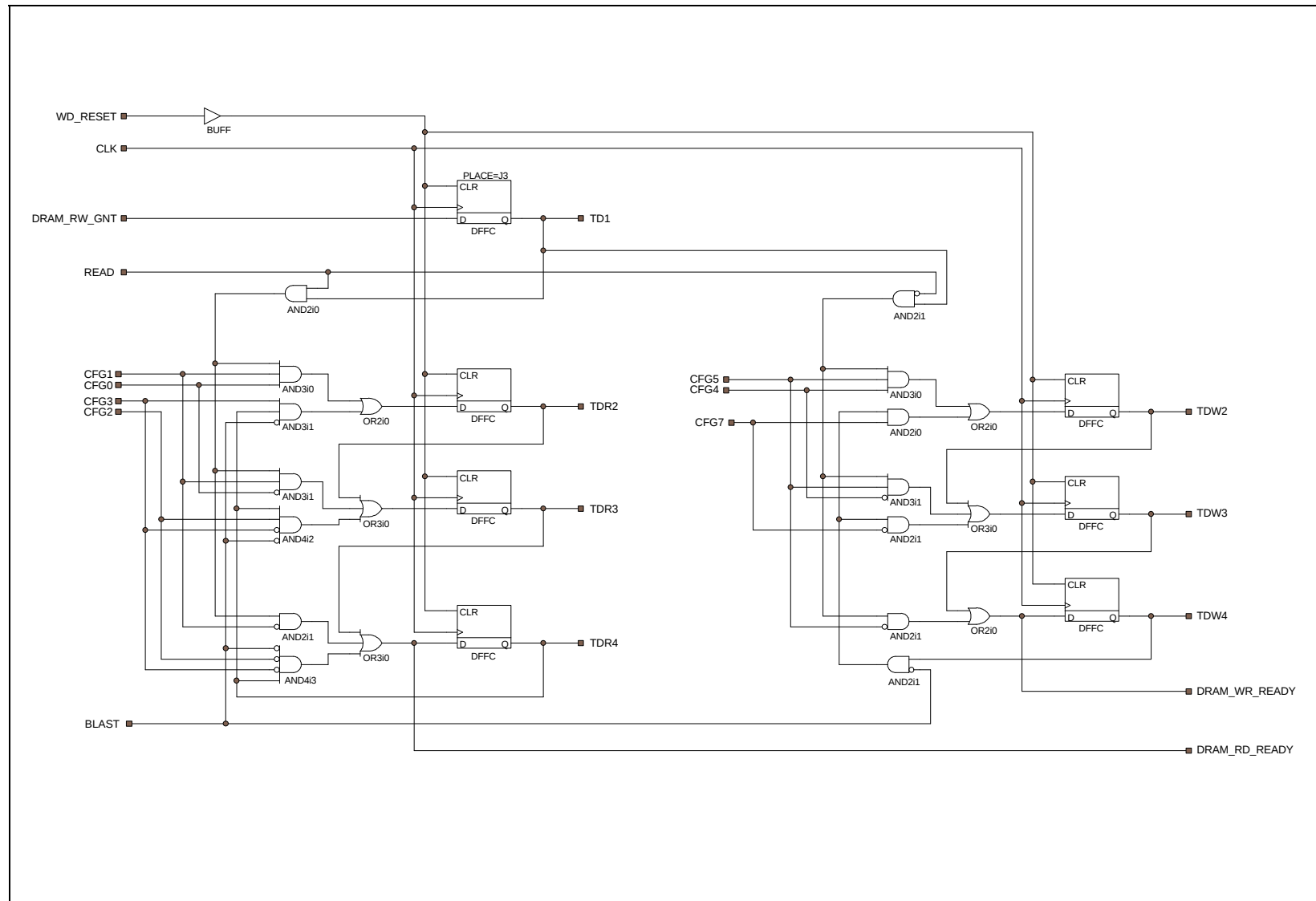
DRAM Controller FPGA Schematics—Sheet 6



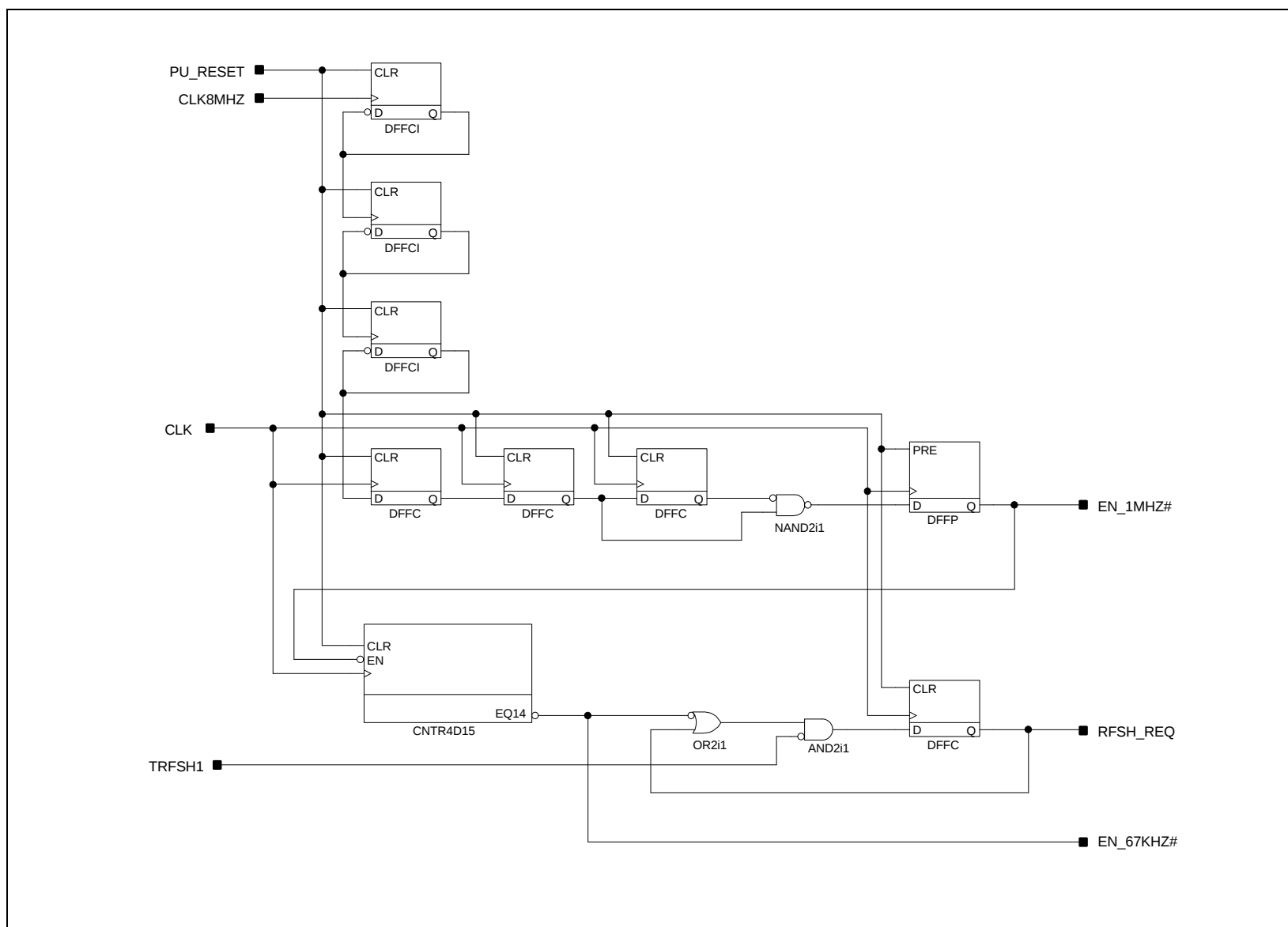
DRAM Controller FPGA Schematics—Sheet 7



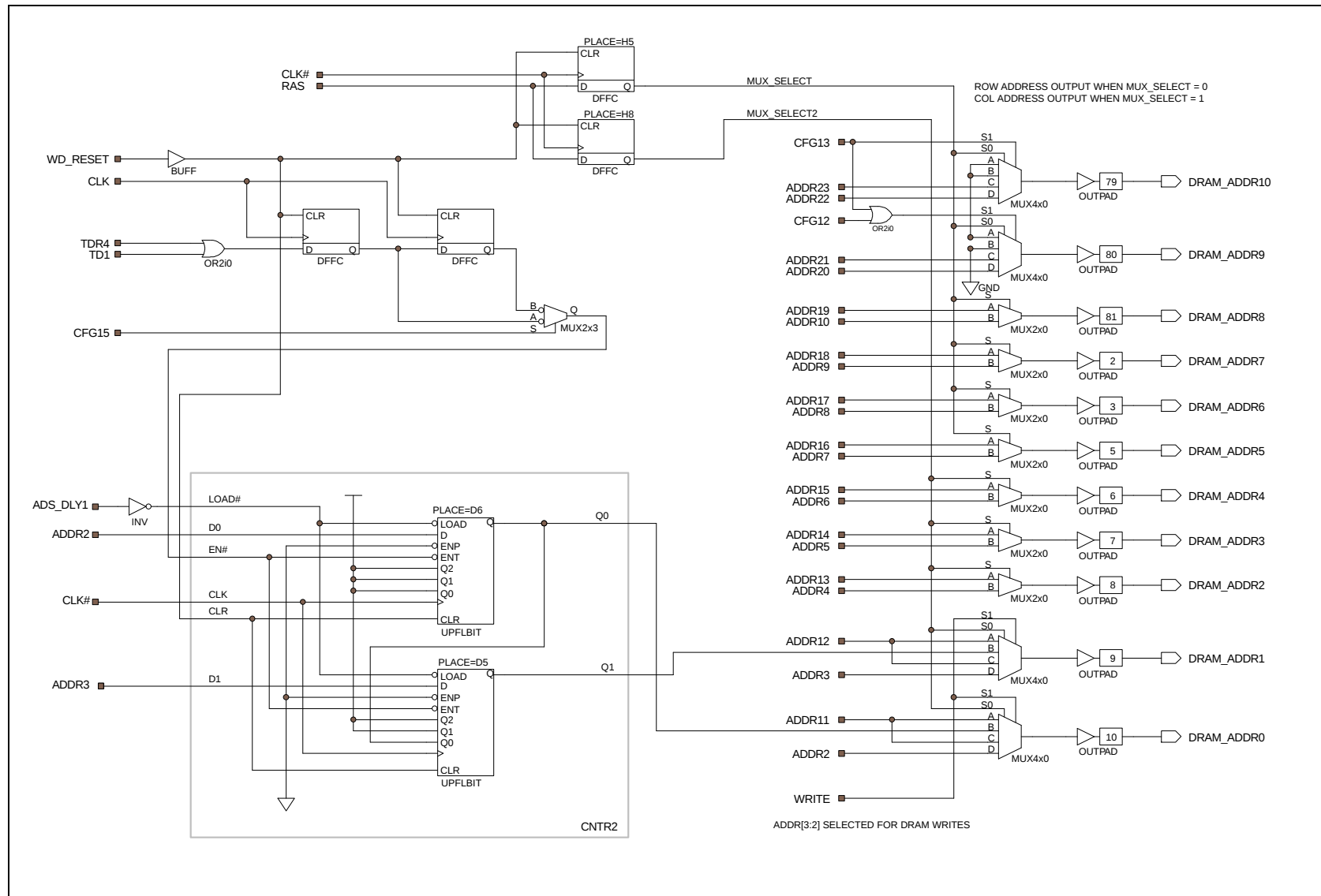
DRAM Controller FPGA Schematics—Sheet 8



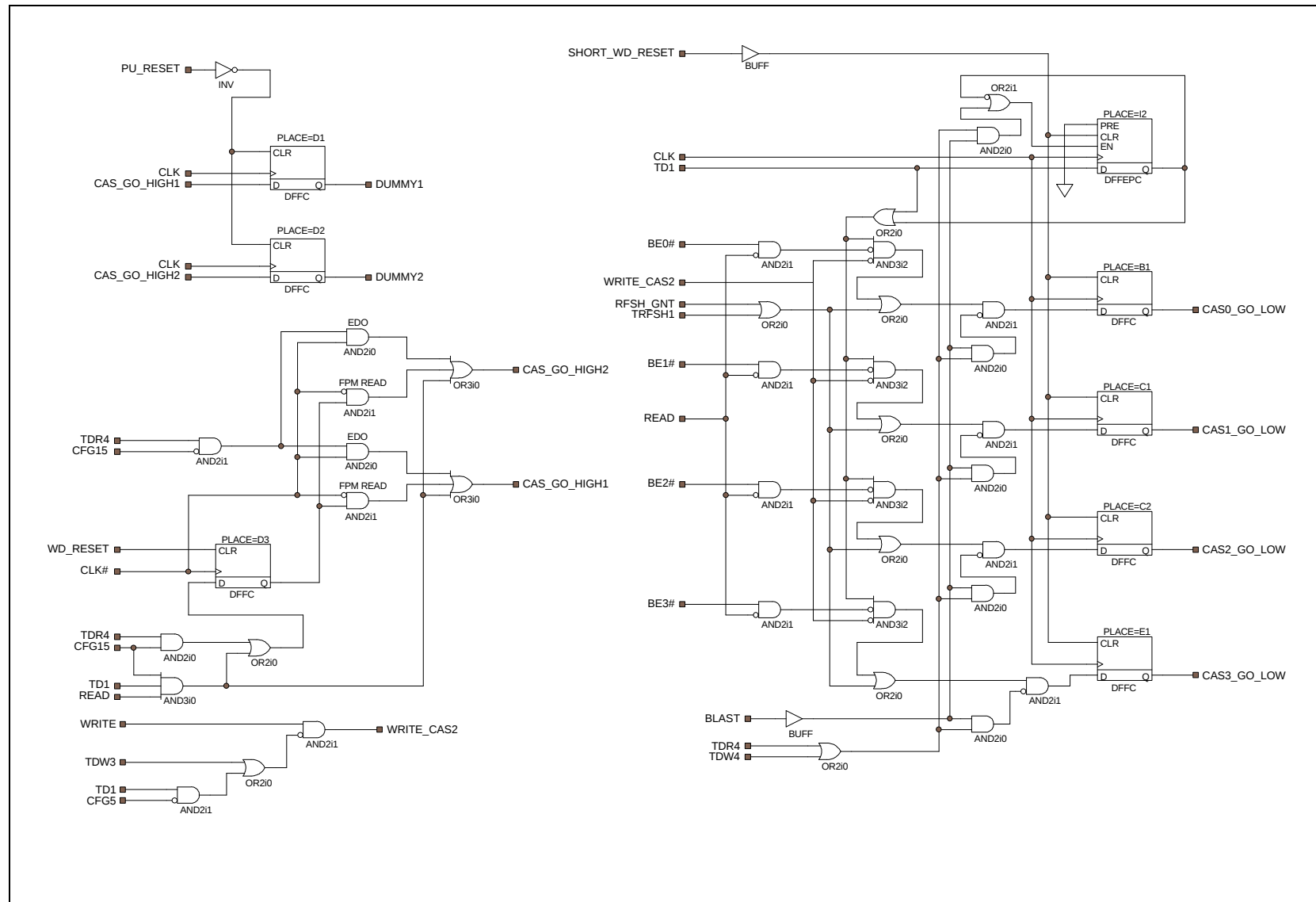
DRAM Controller FPGA Schematics—Sheet 9



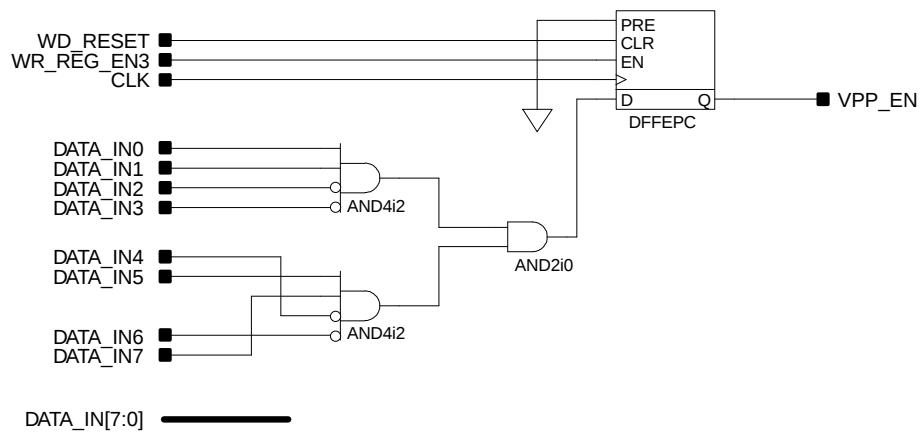
DRAM Controller FPGA Schematics—Sheet 10



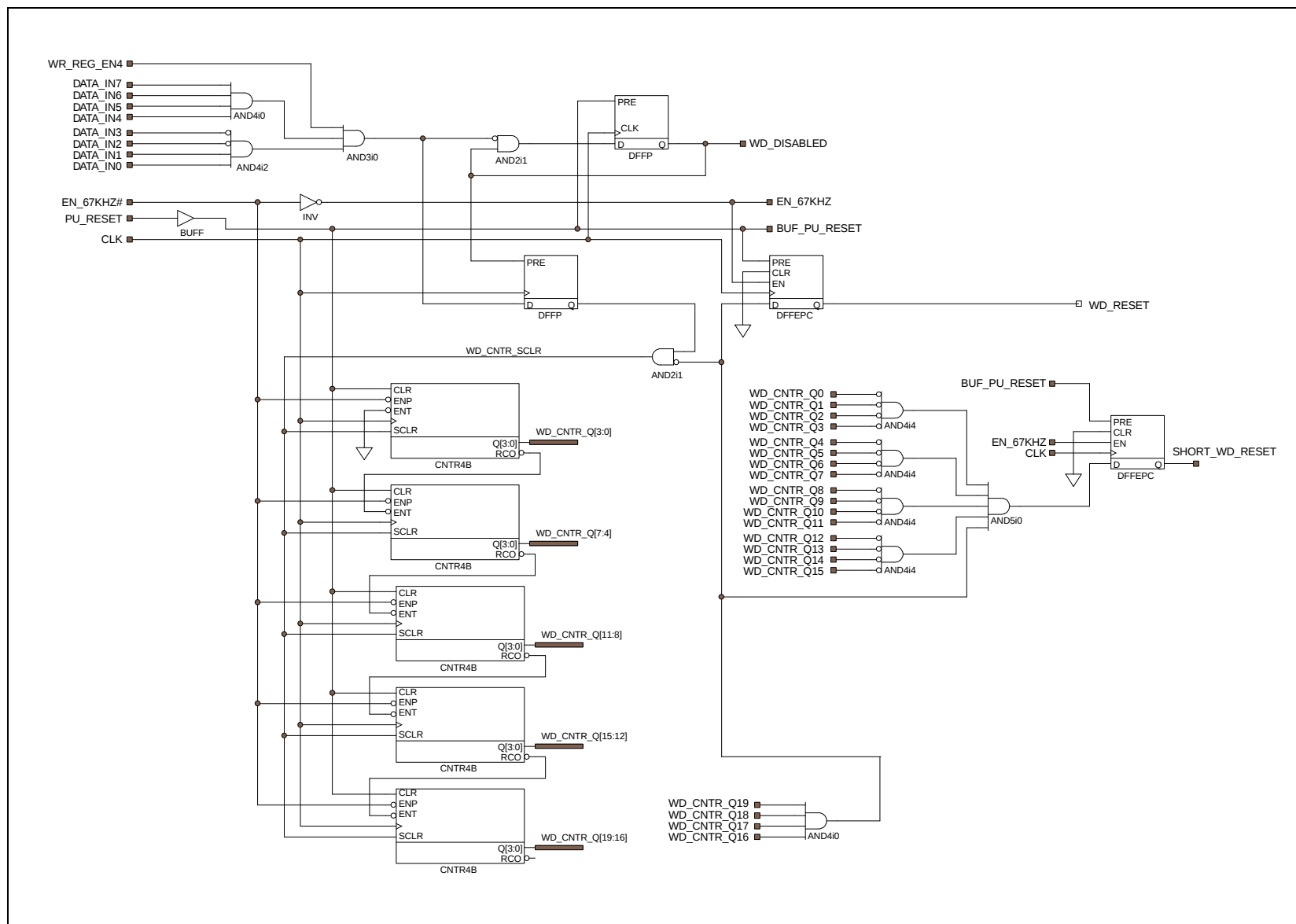
DRAM Controller FPGA Schematics—Sheet 11



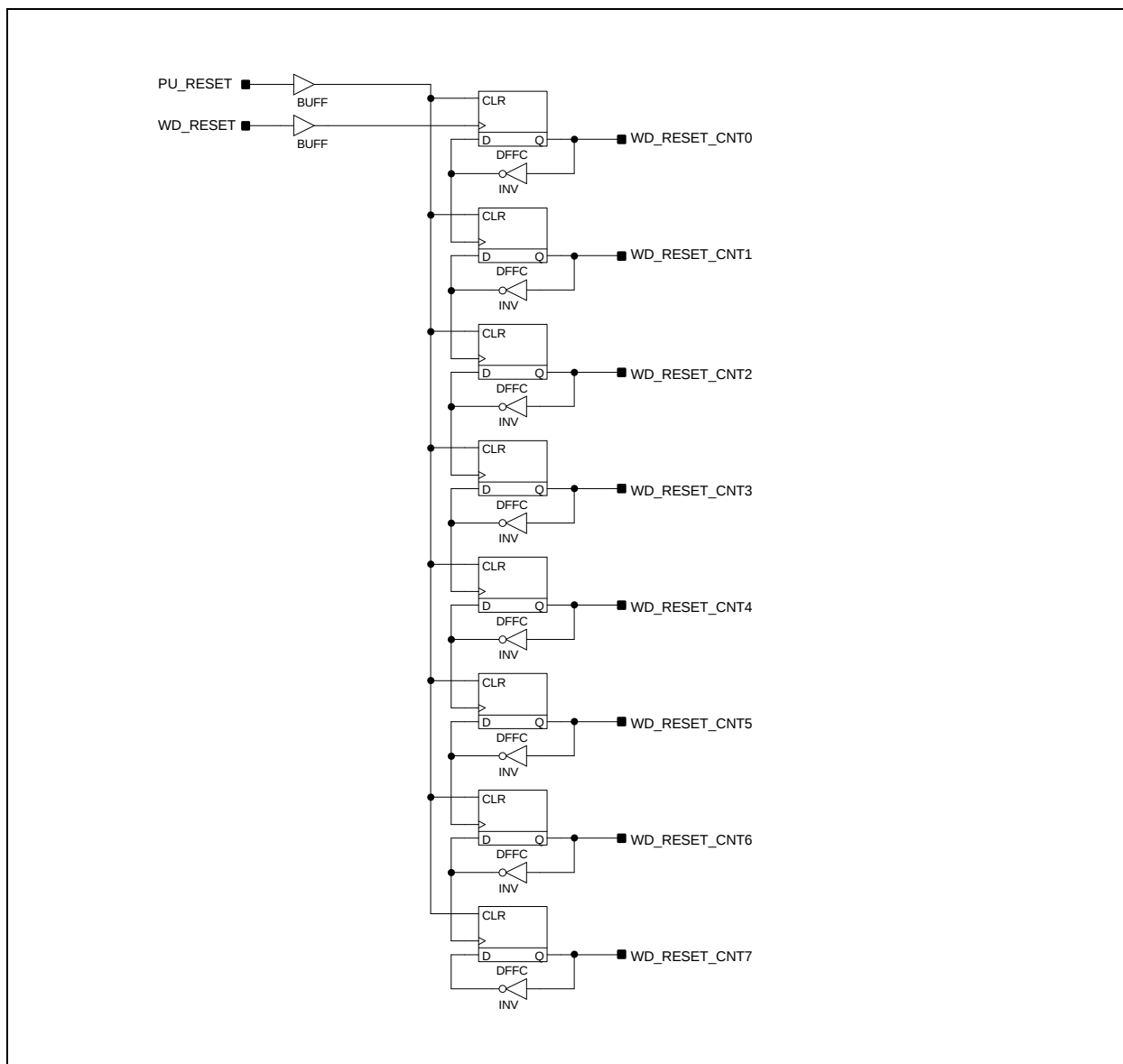
DRAM Controller FPGA Schematics—Sheet 12



DRAM Controller FPGA Schematics—Sheet 13



DRAM Controller FPGA Schematics—Sheet 14



DRAM Controller FPGA Schematics—Sheet 15

