ANTIC

C012296 (NTSC)

REV. D

CONFIDENTIAL

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ATARI

ATARI INCORPORATED
1265 BORREGAS AVE.
SUNNYVALE, CA. 94086

TITLE ANTIC (NTSC)

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SCALE

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1.0) GENERAL:

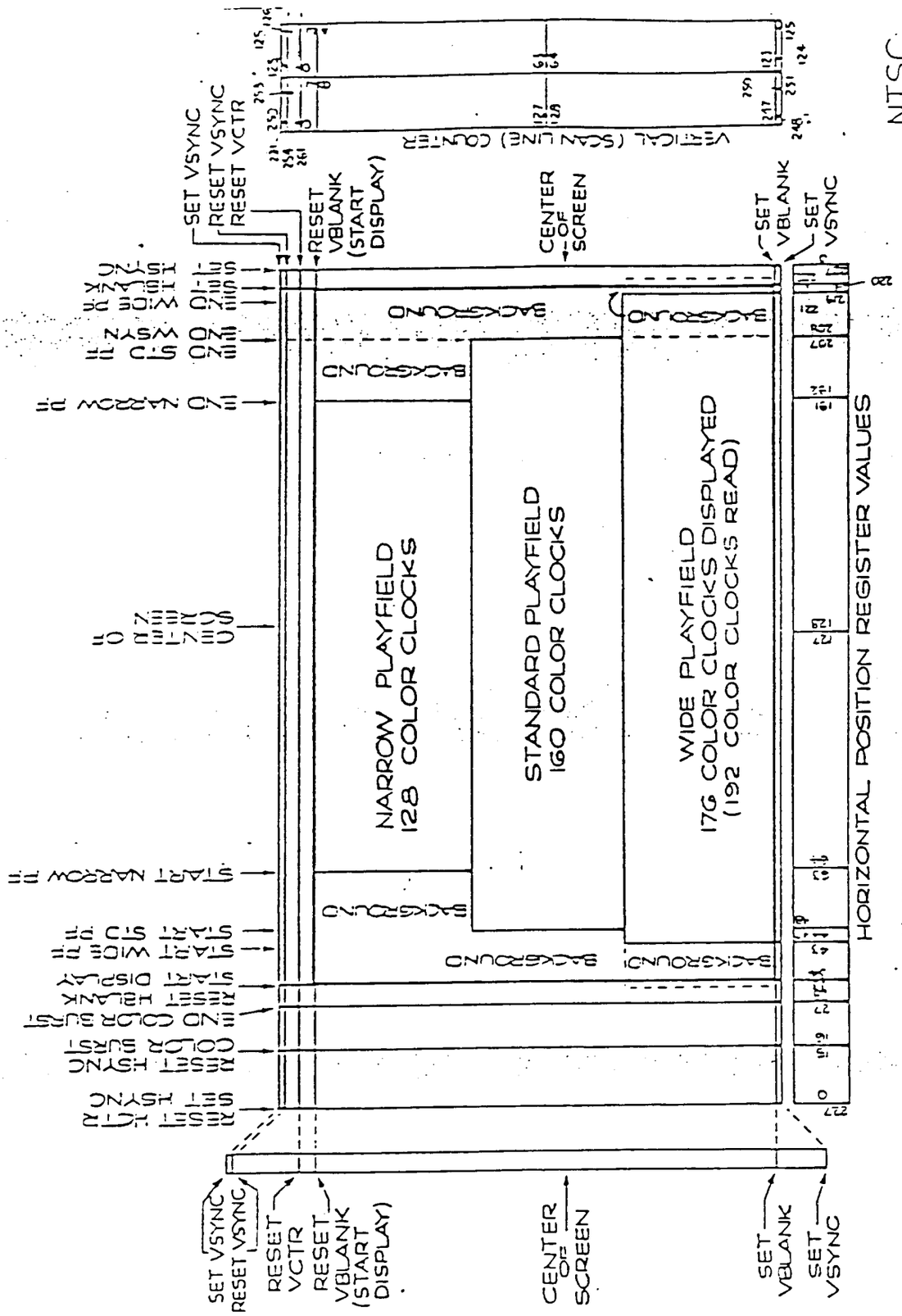
The ANTIC and GTIA chips generate the television display at the rate of 60 frames per second on the NTSC (U.S.) system. Each frame consists of 262 horizontal TV lines and each line is made up of 228 color clocks. The 6502 processor runs at 1.79 MHz. This rate was chosen so that one machine cycle is equivalent in length to two color clocks. One clock is approximately equal in width to two TV lines.

In any graphics mode, the display is divided up into small squares or rectangles called pixels (picture elements). The highest resolution graphics mode has a pixel size of ½ color clock by 1 TV line. A sample display list is given in Section IV.

The current TV line may be determined by reading the vertical counter (VCOUNT). This register gives the line count divided by 2. There are 262 lines per frame, so VCOUNT runs from 0 to 130. The 0 point occurs near the end of vertical blank (see figure on the following page). Vertical blank (VBLANK) is the time during which the electron beam returns back to the top of the screen in preparation for the next frame. The ANTIC and GTIA do not do interlacing, so each frame is identical unless the program which is being executed changes the display. Vertical sync (VSYNC) occurs during the fourth through sixth lines of vertical blank (VCOUNT = hex 7D through 7E). This tells the TV set where each frame starts. After VSYNC, there are 16 more lines of VBLANK for a total of 22 lines of VBLANK. The display list jump and wait instruction (to be described later) causes the display list graphics to start at the end of VBLANK.

The primary function of the ANTIC chip is to fetch data from memory (independent of the microprocessor) for display on the TV screen. It does this with a technique called "Direct Memory Access" or DMA. It requests the use of memory access and data bus by sending a signal called HALT to the microprocessor to become "TRI-STATE" (open-circuit) all during the next computer cycle. The ANTIC chip then takes over the address bus and reads any data it wishes from memory. Another name for this type of DMA is "Cycle Stealing". Once initiated, this DMA is completely and automatically controlled by the ANTIC chip without need for further microprocessor intervention.

The ANTIC provides DMA by use of the following registers. They are: Character Base Address register, Player-Missile Base register, Display List Low and High Pointer, Character Control register, and DMA Control register. The ANTIC also controls vertical and horizontal scrolling. The ANTIC also provides a wait for horizontal sync (WSYNC) command that allows the microprocessor to synchronize itself to the TV horizontal line rate. There are horizontal and vertical light pen registers.



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1.0) GENERAL: (continued)

The ANTIC also provides Non-Maskable Interrupt (NMI) service to the micro-processor. The micro-processor can enable NMI through a single register. The microprocessor can read the NMI interrupt status register to determine the cause of interrupt. The status register can be reset by probing a single register.

2.0) WSYNC:

In addition to a Vertical Blank Interrupt, which allows the microprocessor to synchronize to the vertical TV display, this system also provides a Wait for Horizontal Sync (WSYNC) command that allows the microprocessor to synchronize itself to the TV horizontal line rate. This sync take effect when the processor writes to an I/O location called WSYNC, whenever it desires horizontal synchronization. Writing to this address sets a latch which pulls to zero a pin on the microprocessor called READY. When READY goes to zero the microprocessor stops and waits. The latch is automatically reset (returning READY true) at the beginning of the next horizontal blank interval, releasing the microprocessor to return program execution.

WSYNC (Wait for Horizontal Blank Synchronism - i.e. wait until start of next TV line.) (D40A):

not used

This address sets a latch that pulls down on the RDY line to the micro-processor, causing it to wait until this latch is automatically reset by the beginning of horizontal blank. Display list interrupts may be delayed by 1 line if WSYNC is used.

3.0) VERTICAL LINE COUNTER:

The current TV line may be determined by reading the vertical counter (VCOUNT). This register gives the line count divided by 2. There are 262 lines per frame, so VCOUNT runs form 0 to 130. The 0 point occurs near the end of vertical blank.

3.0) VERTICAL LINE COUNTER (continued):

VCOUNT (Vertical Counter) (D40B): This address reads the Vertical TV Line Counter (8 most significant bits).

D7	D6	D5	D4	D3	D2	D1	D0
V8	V7	V6	V5	V4	V3	V2	V1

V0 not read. Two line resolution supplied.

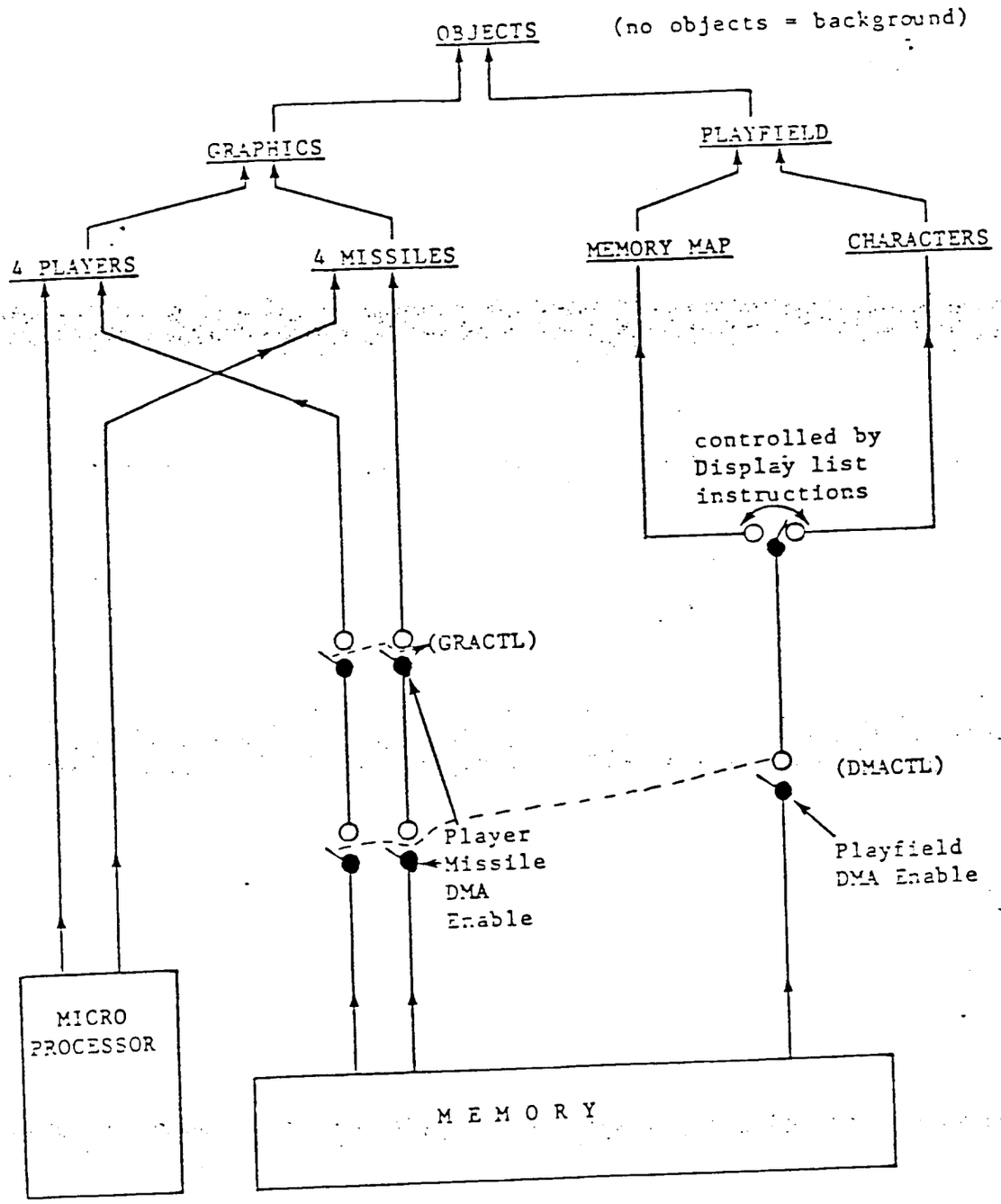
4.0) OBJECT DMA (Direct Memory Access):

The primary function of the Antic chip is to fetch data from memory (independent of the microprocessor) for display on the TV screen. It does this with a technique called "Direct Memory Access" or DMA. It requests the use of the memory address and data bus by sending a signal called HALT to the microprocessor, causing the processor to become "TRI-STATE" (open circuit) all during the next computer cycle. The ANTIC chip then takes over the address bus and reads any data it wishes from memory. Another name for this kind of DMA is "cycle stealing". Once initiated, this DMA is completely and automatically controlled by the ANTIC chip without any need for further microprocessor intervention.

There are two types of DMA: Playfield and Player-Missile (see figure on following page). The playfield DMA control circuit on the ANTIC chip resembles a small dumb microprocessor. By halting the main microprocessor it can fetch its own instructions from memory (the display list) addressed by its program counter (display list pointer). Each instruction defines the type (alpha character or memory map) and the resolution (size of bits on the screen) and the location of the data in memory which is to be displayed on the next group of lines.

In order to begin this DMA, the main microprocessor must store a display list of instructions in memory, store data to be displayed in memory, tell the ANTIC where the display list is (initialize the display list pointer) and enable the DMA control flags on the ANTIC (DMACTL register).

In addition to the playfield DMA described above, the ANTIC chip simultaneously controls another DMA channel. This type of DMA addresses PLAYER-MISSILE graphics data stored in memory and passes the graphics data on to the CTIA chip graphics registers. This type of DMA (if enabled) occurs automatically, interspersed with the playfield DMA described previously. This PLAYER-MISSILE DMA has no display list of instructions, and is therefore much simpler than the PLAYFIELD DMA.



O B J E C T D I S P L A Y S O U R C E S

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4.0) OBJECT DMA (Direct Memory Access) (continued):

In addition to the two types of display DMA, the ANTIC chip also generates DMA addresses for the refresh of the dynamic memory RAM used in this system. This is also completely automatic and need be considered by the programmer only if he is concerned with real-time programming where an exact count of the computer cycles is important.

The player-missile graphic registers may be reloaded by the microprocessor (GRAF (X)), or automatically from memory with direct memory access (DMA). (see figure on next page). The programmer must place the object graphics in memory, write the player-missile base address (PMBASE), and enable player-missile DMA (DMACTL, GRACTL). The transfer of object graphics from memory to display is then fully automatic. GRACTL is a control register on the GTIA chip.

DMACTL (Direct Memory Access Control) (D400):

This address writes data into the DMA Control Register.

Not Used	D5	D4	D3	D2	D1	D0

D5 = 1 Enable instruction fetch DMA

D4 = 1 1 Line P/M resolution

D4 = 0 2 line P/M resolution

D3 = 1 Enable Player DMA

D2 = 1 Enable Missile DMA

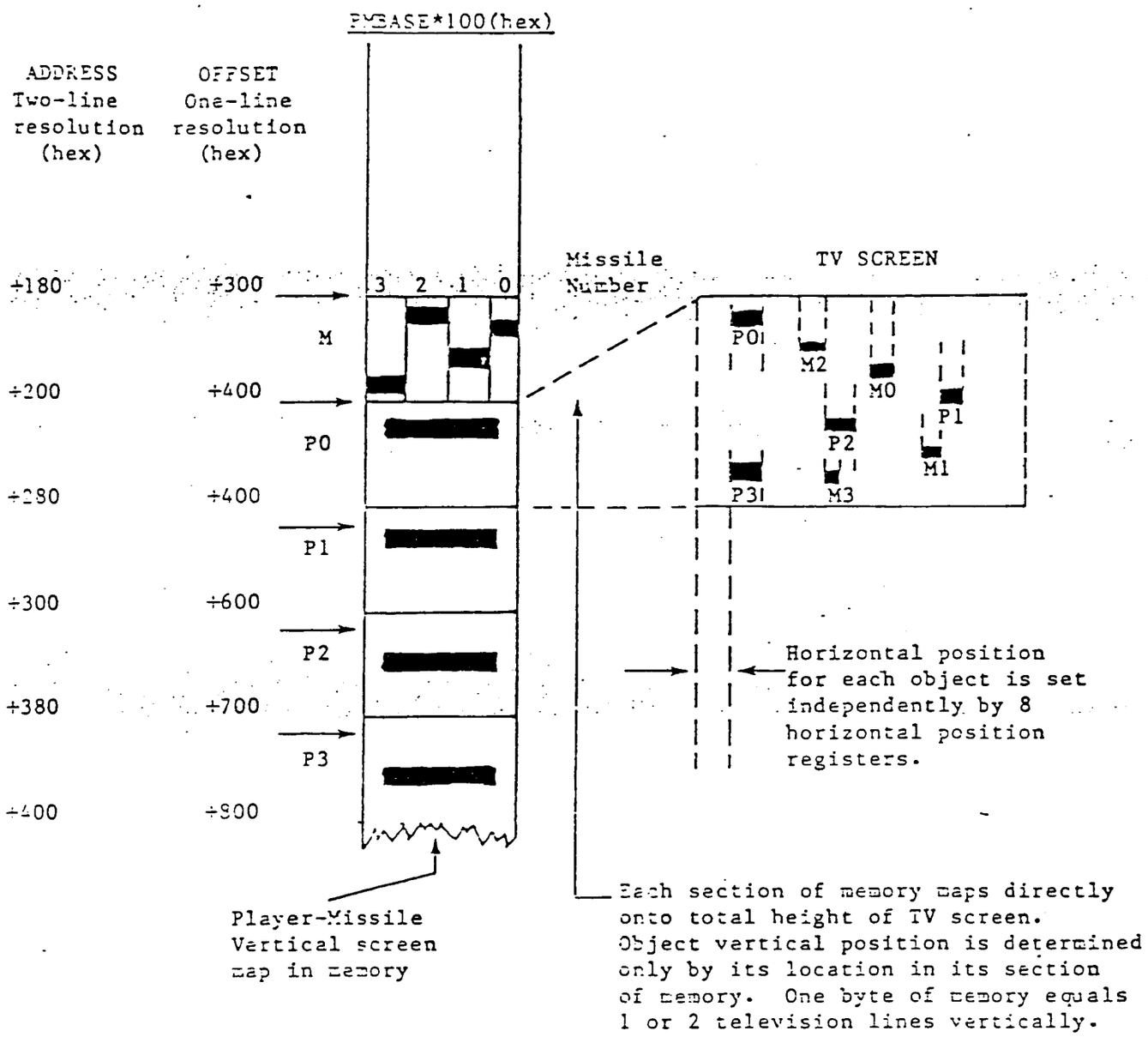
D1,D0 = 0 0 No Playfield DMA

= 0 1 Narrow Playfield DMA (128 Color Clocks)

= 1 0 Standard Playfield DMA (160 Color Clocks)

= 1 1 Wide Playfield DMA (192 Color Clocks)

Player-Missile Base Address (PMBASE) = MSB of address.
Resolution is controlled by bit 4 of DMACTL.



P L A Y E R - M I S S I L E D M A

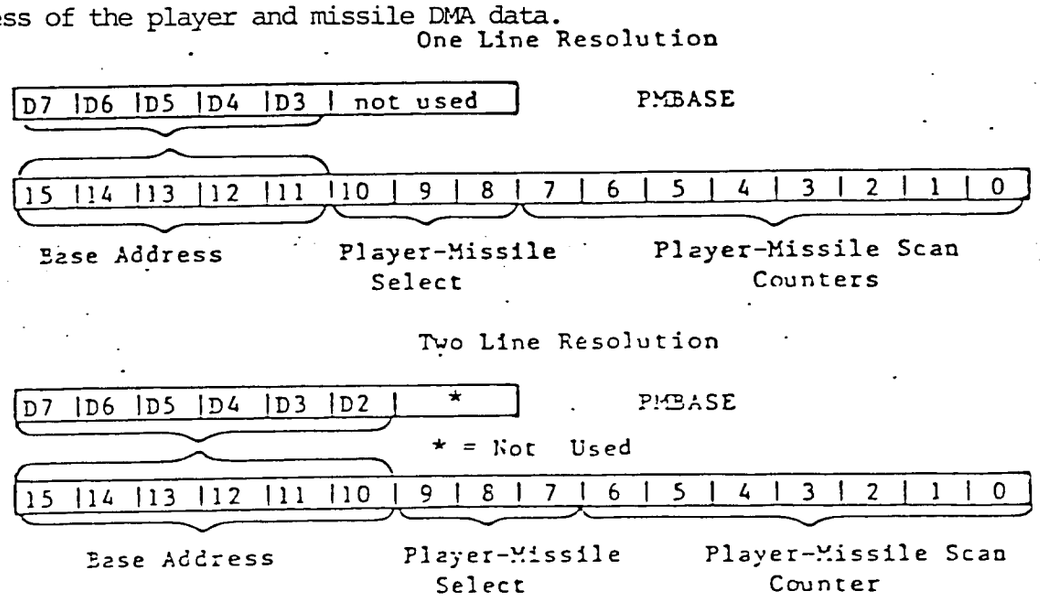
5.0) PLAYER MISSILE BASE ADDRESS

PMBASE specifies the most signifigant byte (MSB) of the address of the player-missile graphics. The location of the graphics for each object is determined by adding an offset to PMBASE *256 (decimal). The bytes between the base address and the missile data are not used by ANTIC so they are available to the programmer.

Only the five most signifigant bytes of PMBASE are used with single-line resolution and the six most signifigant bytes are used with two-line resolution. This means that the location of the graphics in memory is restricted to certain page boundaries. Two-line resolution means that each byte of data is repeated for two lines. (see DMACTL, bit 4). 640 (decimal) bytes (5 X 128) are required for two-line resolution and 1280 bytes (5 X 256) for one-line resolution.

Each byte in the player graphics area represents eight pixels which are to be displayed on the corresponding line(s) of the TV screen. A 1 indicates that the player's color-lum is to be displayed in that pixel. The graphics may be anything, not just rectangles like the ones in figure II.3. The player graphics may fill the entire height of the screen or they may be only a couple of lines high if the rest of the display data is all 0's. Each byte in the missile display also represents eight pixels, two pixels for each missile. Each pixel may be 1, 2, or 4 color clocks, and is determined by the SIZE registers.

PMBASE (Player-Missile Address Base Register): This address writes data into the Player-Missile Base Register. The data specifies the MSB of the address of the player and missile DMA data.



6.0) PLAYFIELD

Playfield is always generated by DMA. There are four playfields, each identified by its own color-lum register and collision detection. Playfield is generated by two different DMA techniques: memory map and character. Both methods provide lists of instructions in memory, independent of the player-missile generation.

Unlike players and missiles, there are no horizontal position registers for playfield. Each player can only have one byte of display per line. Playfield, on the other hand, may require up to 48 bytes per line because it can fill the entire width of the screen.

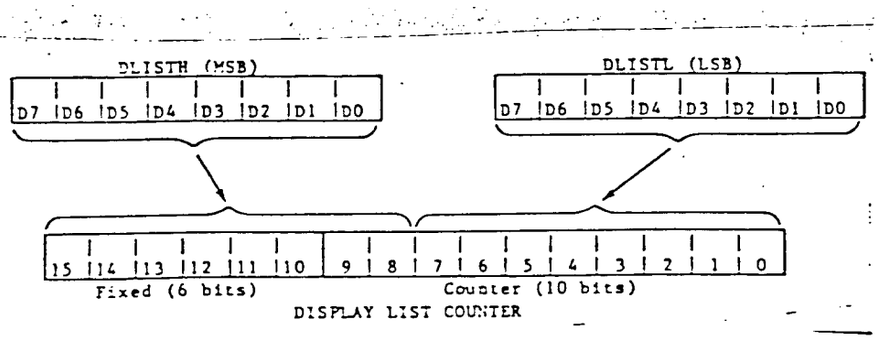
There are three different playfield widths: Narrow (128 color clocks), standard (160 color clocks), and wide (192 color clocks). The width is selected by storing into DMACTL. The advantage of a narrower width is that less RAM is required and fewer machine cycles are stolen for DMA.

6.1) Display List: The display list is a sequence of display instructions stored in memory. These instructions are either one (1) byte or three (3) bytes long. The display list can be considered a display program and the Display List Counter that fetches these instructions can be thought of as a display program counter. (10 bit counter plus 6 bit base register).

The display list counter can be initialized by writing to DLISTH and DLISTL. Once initialized, this counter value is used to address the display list, fetch the instruction, display one (1) to sixteen (16) lines of data on the TV screen, increment the Display List Counter, fetch the next display instruction, and so on automatically without microprocessor control. DLISTL and DLISTH should be altered only during vertical blank or when DMA is disabled (see DMACTL).

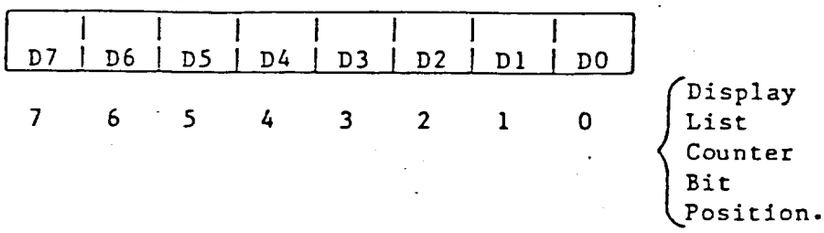
Each instruction defines the type (alpha character or memory map) and the resolution (size of bits on the screen) and the location of data in memory to be displayed for a group (1 to 16) lines. Each group of lines is called a display block.

THE DISPLAY LIST CANNOT CROSS A 1 K BYTE MEMORY BOUNDARY UNLESS A JUMP INSTRUCTION IS USED.

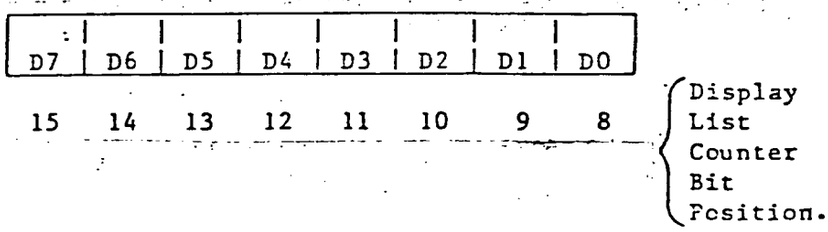


6.0) PLAYFIELD (continued):

DLISTL (Display List Low) (D402): This address writes data into the low byte of the Display List Counter.



DLISTH (Display List High) (D403): This address writes data into the high byte of the Display List Counter.

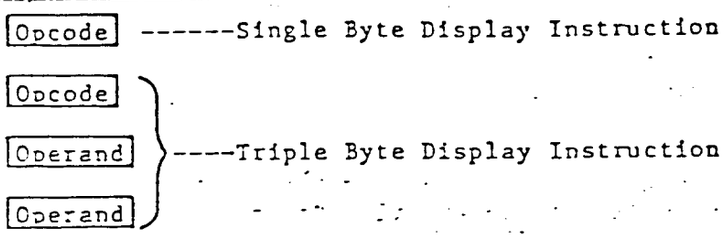


The Display List is a list of display instructions in memory. These instructions are addressed by the Display List Counter. Loading these registers defines the address of the beginning of the Display List. (See sections I and II.)

Note: The top 6 bits are latches only and have no count capability, therefore the display list cannot cross a 1 K byte memory boundary unless a jump instruction is used.

DLISTL and DLISTH should be changed only during vertical blank or with DMA disabled. Otherwise, the screen may roll. Bit 7 of NMIEN must be set in order to receive display list interrupts.

6.2) Display Instruction Format: Each instruction consists of either an opcode only, or of an opcode followed by two (2) bytes of operand.



6.2) Display Instruction Format (continued):

The opcode is always fetched first and placed in the Instruction Register. This opcode defines the type of instruction (1 or 3 bytes) and will cause two more bytes to be fetched if needed. If fetched, these next two (2) bytes will be placed in the Memory Scan Counter, or in the Display List Counter (if the instruction is a Jump).

Display Instruction Register (IR): This register is loaded with the opcode of the current display list instruction. It cannot be accessed directly by the programmer. There are three basic types of display list instructions: blank, jump, and display.

Blank (1-byte)

D7	D6	D5	D4	0	0	0	0

This instruction is used to create 1 to 8 blank lines on the display (blackground color).

D7	1	= display list instruction interrupt
D6 - D4	0-7	= 1-8 blank lines
D3 - D0	0	= blank

Jump (3-bytes)

D7	D6	X	X	0	0	0	1

This instruction is used to reload the Display List Counter. The next two bytes specify the address to be loaded (LSB first).

D7	1 = display list instruction interrupt
D6	0 = jump (creates one blank line on display)
	1 = jump and wait until end of next vertical blank
D5-D4	X = don't care
D3-D0	1 = jump

Display (1 or 3 bytes)

D7	D6	D5	D4	D3	D2	D1	D0

This instruction specifies the type of display for the next display block.

D7	1 = display list instruction interrupt
D6	0 = 1 byte instruction
	1 = 3 byte instruction (reload Memory Scan Counter using address in next two bytes, LSB first).
D5	1 = vertical scroll enable
D4	1 = horizontal scroll enable
D3-D0	2-F = display mode (memory or character map - see following pages).

Bit 7 of a display list instruction can be set to create a display list interrupt if bit 7 of NMIEN is set. The display list interrupt code can change the colors or graphics during the middle of the TV display. The type of interrupt is determined by checking NMIST. NMIRES clears NMIST.

HSCROL		XX		XX		XX		XX		XX		XX		XX		XX	Horizontal Scrolling
VSCROL			XX	XX			XX	XX			XX	XX			XX	XX	Vertical Scrolling
LD MEM SCAN					XX	XX	XX	XX					XX	XX	XX	XX	Load memory scan (3 byte)
INST INTERRUPT									XX	XX	XX	XX	XX	XX	XX	XX	Display instruction interrupt
BLK 1	00								80								Blank 1 line
" 2	10								90								Blank 2 lines
" 3-7																	Blank 3 thru 7 lines
" 8	70								F0								Blank 8 lines
JMP	01								81								Jump (3 byte instruction)
JVB	41								C1								Jump & wait for Vert. Blank (also 3 byte)
CHR (40,2,8)	02	12	22	32	42	52	62	72	82	92	A2	B2	C2	D2	E2	F2	Character Mode Instructions
" (40,2,10)	03	13	23	33	43	53	63	73	83	93	A3	B3	C3	D3	E3	F3	
" (40,4,8)	04	14	24	34	44	54	64	74	84	94	A4	B4	C4	D4	E4	F4	
" (40,4,16)	05	15	25	35	45	55	65	75	85	95	A5	B5	C5	D5	E5	F5	
" (20,5,8)	06	16	26	36	46	56	66	76	86	96	A6	B6	C6	D6	E6	F6	
" (20,5,16)	07	17	27	37	47	57	67	77	87	97	A7	B7	C7	D7	E7	F7	
MAP (40,4,8)	08	18	28	38	48	58	68	78	88	98	A8	B8	C8	D8	E8	F8	Memory Map Mode Instructions
" (80,2,4)	09	19	29	39	49	59	69	79	89	99	A9	B9	C9	D9	E9	F9	
" (80,4,4)	0A	1A	2A	3A	4A	5A	6A	7A	8A	9A	AA	BA	CA	DA	EA	FA	
" (160,2,2)	0B	1B	2B	3B	4B	5B	6B	7B	8B	9B	AB	BB	CB	DB	EB	FB	
" (160,2,1)	0C	1C	2C	3C	4C	5C	6C	7C	8C	9C	AC	BC	CC	DC	EC	FC	
" (160,4,2)	0D	1D	2D	3D	4D	5D	6D	7D	8D	9D	AD	BD	CD	DD	ED	FD	
" (160,4,1)	0E	1E	2E	3E	4E	5E	6E	7E	8E	9E	AE	BE	CE	DE	EE	FE	
" (320,2,1)	0F	1F	2F	3F	4F	5F	6F	7F	8F	9F	AF	BF	CF	DF	EF	FF	

Number of TV lines per cell
Number of Colors (Background + Playfield types)
Number of Horizontal cells (standard width screen)

4) DISPLAY INSTRUCTION OPCODES

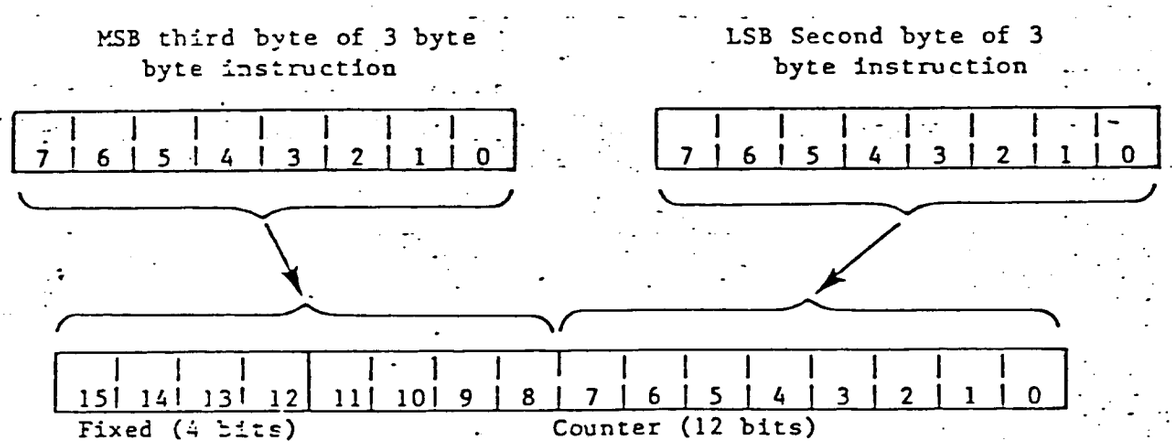
6.2) Display Instruction Format (continued):

Bits 5 and 4 of a display type of display list instructions are used to enable vertical and horizontal scrolling. The amount of scrolling depends on the values in the VSCTOL and HSCROL registers (to be described later).

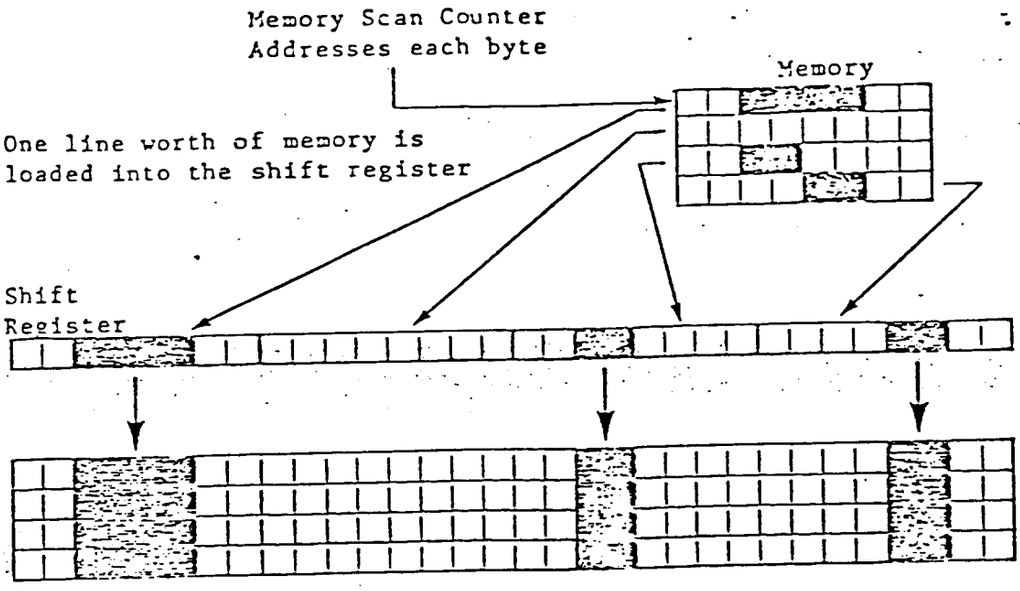
6.3) Memory Scan Counter: This counter is not directly accessible by the programmer. It is loaded with the value in the last 2 bytes of a 3 byte (non-Jump) instruction.

This counter points to the location (address) in memory of data to be directly displayed (memory map display) or to the location of character name strings to be indirectly displayed (character display).

A single byte instruction does not reload this counter. This implies a continuation in memory of data to be displayed from that displayed by the previous instruction. Since this counter really consists of 4 bits of register and 12 of actual counter, a continuous memory block cannot cross 4K byte memory boundaries, unless the counter is repositioned with a 3 byte Load Memory Scan Counter instruction.



6.4) Memory Map Display Instructions: Data in memory (addressed by the Memory Scan Counter) is displayed directly when executing a memory (bit) map display instruction. As data is being displayed it is also stored in a shift register so that it can be redisplayed for as many TV lines as required by the instruction.



Shift register data is displayed for four TV scan lines in this example.

In Instruction Register (IR) display modes 8 through F, one or two bits of memory are used to specify what is to be displayed on each pixel of the screen. Pixel sizes range from 1/2 clock by 1 TV line to 4 clocks by 8 TV lines.

In IR mode F, only one color (COLPF2) can be displayed. Two different luminances are available. If a bit is a zero, then the luminance of the corresponding pixel comes from COLPF2. If the bit is a one, then the luminance is determined by the contents of COLPF1 (abbreviated to PF1).

In IR modes 9, B, and C, two different colors can be displayed. A zero indicates background color and a one indicates PF0 color. The difference between the various modes is is the size of the pixels.

In IR modes 8, A, D, and E, two bits are used to specify the color of each pixel. This allows four different colors to be displayed. However, only four pixels can be packed into each byte, instead of eight as in the previous modes. The bit assignments are shown below:

SHIFT REGISTER	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

2 bits form one pixel

5) MEMORY MAP DISPLAY MODES

Inst. Reg. HEX	Colors per Mode	Pixels per Std. Line	Bytes per Std. Line	Scan Lines per Pixel	Color Clocks per Pixel	Bits per Pixel	Bit Values in Pixel	Color Reg. Select
8	4	40	10	8	4	2	00 01 10 11	BAK PF0 PF1 PF2
9	2	80	10	4	2	1	0 1	BAK PF0
A	4	80	20	4	2	2	00 01 10 11	BAK PF0 PF1 PF2
B	2	160	20	2	1	1	0 1	BAK PF0
C	2	160	20	1	1	1	0 1	BAK PF0
D	4	160	40	2	1	2	00 01 10 11	BAK PF0 PF1 PF2
E	4	160	40	1	1	2	00 01 10 11	BAK PF0 PF1 PF2
F	1 ½	320	40	1	½	1	0 1	PF2 PF1 (LUM)

6.5) Character Display Instructions: The first step in using the character map mode is to create a character set in memory. The character set contains eight bytes of data for the graphics for each character. The meaning of the data depends on the mode. The character set can contain 64 or 128 characters, also depending on the mode. The MSB (Most Significant Byte) of the address of the character set is stored in CHBASE. Only the most significant six or seven bits of CHBASE are used. The other one or two bits and the LSB of the address are assumed to be zero, so the character set must start at an acceptable page boundary.

The next step is to set up the display list for the desired mode. Then the actual display is set up. This consists of a string of character names or codes. Each name takes one byte. The last 6 or 7 bits of the name selects a character. For a 64 character set, the name would range from 0 through 63 (decimal). For a 128 character set, the range would be 0 through 127 (decimal). The upper one or two bits of the name byte are used to specify the color or other special information, depending on the mode.

Character names (codes) are fetched by the memory scan counter, and are placed in a shift register. On any given line of display the shift register rotates, changing only the name portion of the character address, as shown below.

After a full line of character data has been displayed the line counter will increment. The next line again addresses all characters by name for that line number.

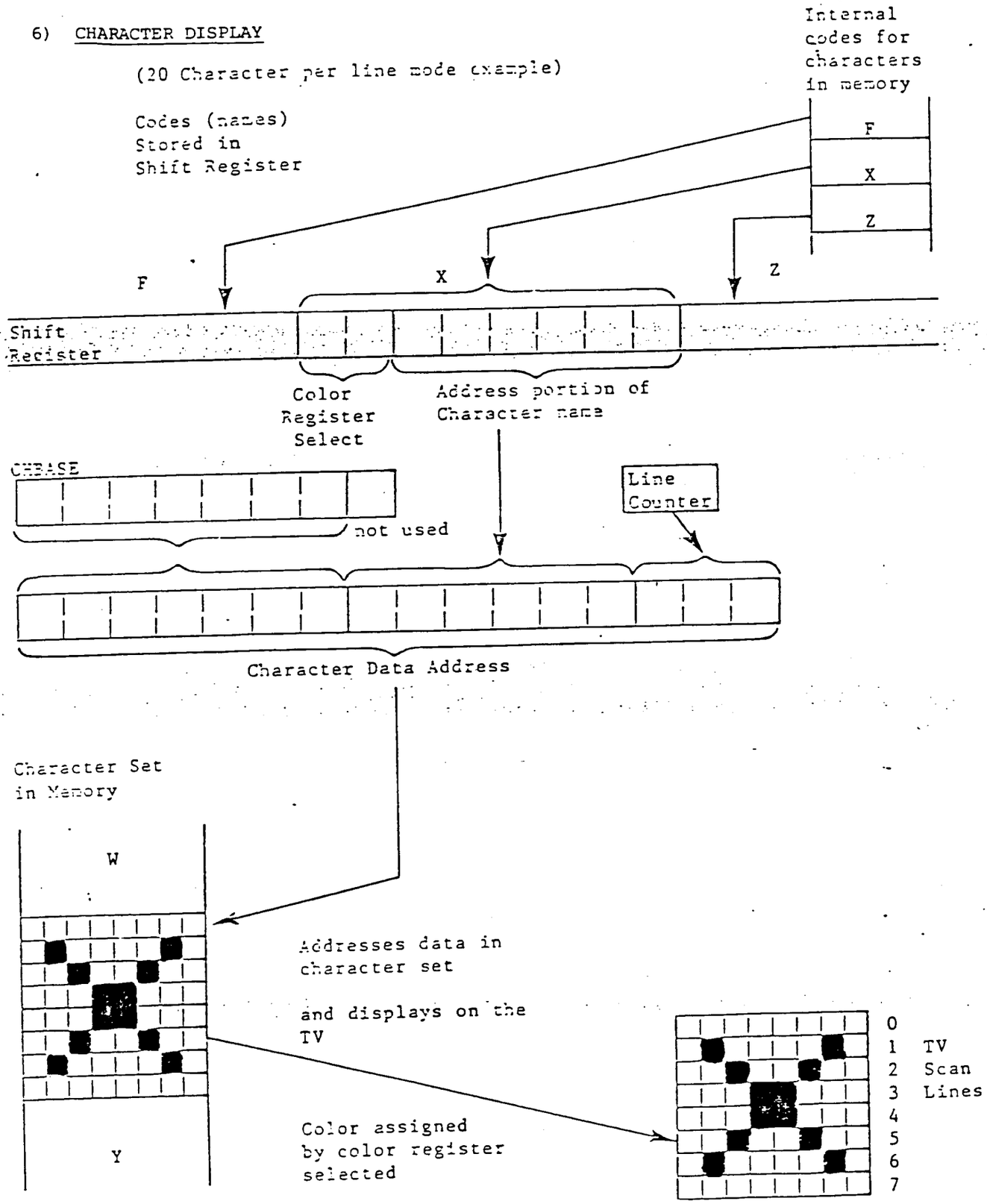
In 20 character per line modes the seven most significant bits of CHBASE are used. This requires that the character set to start upon a 512 byte memory boundary. The set must contain 64 characters, 8 bytes each giving a total of 512 bytes for the set.

The 40 character per line modes use the six most significant bits of CHBASE, forcing the character set to start on a 1K byte memory boundary. The set must have 128 characters of 8 bytes each. This gives a total of 1024 bytes for the set.

Hex Code	Graphics Mode	Chars. Per Line	Number of Colors	Bytes per Char.	Number of Char. in set	Bytes in Char Set
2	0	40	2	8	128	1024
3	-	40	2	8	128	1024
4	-	40	4	8	128	1024
5	-	40	4	8	128	1024
6	1	20	5	8	64	512
7	2	20	5	8	64	512

6) CHARACTER DISPLAY

(20 Character per line mode example)



6.5) Character Display Instructions: (continued)

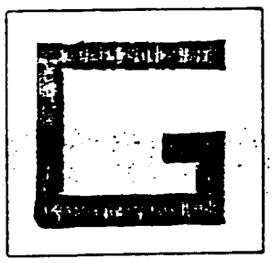
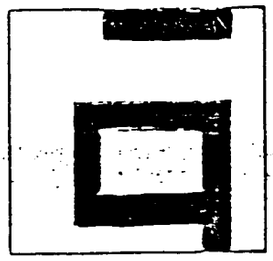
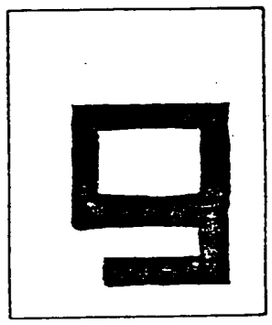
There are six character map modes, IR modes 2 through 7. In IR modes 6 and 7, the upper two bits of each character name select one of four playfield colors. For each data bit that contains a one, the selected playfield color is displayed. For each zero data bit, the background color is displayed. The four character colors plus the background color gives a total of five different colors. The mode 6 characters are eight lines high and the mode 7 characters are sixteen lines high (each data byte is displayed for two lines).

In IR modes 4 and 5, each character is only four pixels wide instead of eight (as in other modes). Two bits per pixel of data are used to select one of three playfield colors, or background. Seven name bits are used to select the character. If the most signifigant name bit is a zero then data of 10(binary) selects PF1. If the name bit 7 is a one, then data bits of 10 select PF2. This makes it possible to display two characters with different colors, using the same data but different name bytes.

In IR modes 2 and 3, each pixel is half of a color clock in width. This makes it possible to have forty eight-pixel wide characters in a standard width line. These modes are similar to memory mode F in that two luminances can be displayed, but only one color is available at a time. In IR mode 3, each character is 10 lines high. This makes it possible to define lower case characters with descenders. The last fourth of the character set (name bits 5 and 6 equal to one) is lowered. The hardware takes the first two data bytes and moves them to the bottom of the character, displaying two blank lines at the top of the character (see next page).

In IR modes 2 and 3, bit 7 of the character name is used for inverse video or blanking. This is controlled by CHACTL (Character Control). If bit 2 of CHACTL is a one then all of the characters will be displayed upside down, regardless of mode. If CHACTL bit 1 is set, then each character which has bit 7 of its name set will be displayed in inverse video (the luminances will be reversed). If CHACTL bit 0 is set, then each character which has bit 7 set will be blanked (only background will be displayed). Characters can be blinked on and off by setting name bit 7 to 1 and toggling CHACTL bit 0. Inverse video and blank apply only to IR modes 2 and 3. If both inverse video and blank are set then the character will appear as an inverse video blank character (solid square).

7) IR MODES 3 - UPPER & LOWER CASE CHARACTER DISPLAY

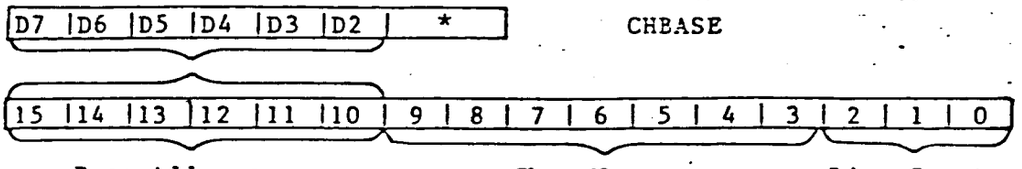
	Upper Case	Lower Case
Data		
Actual Display		

8) CHARACTER MAP DISPLAY MODES

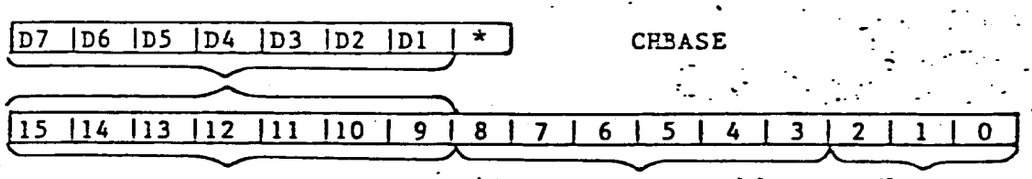
Inst. Reg. HEX	Colors per Mode	Chars. per Std. Line	Scan Lines per Char.	Color Clocks per Pixel	Data Bits per Pixel	Color Select Bits In Name	Bit Values in Data	Color Reg. Select
2	1½	40	8	½	1	-	0 1	PF2 PF1 (LUM)
3	1½	40	10	½	1	-	0 1	PF2 PF1 (LUM)
4	5	40	8	1	2	Bit 7 = 0	00 01 10 11	BAK PF0 PF1 PF2
						Bit 7 = 1	11	PF3
5	5	40	16	1	2	Bit 7 = 0	00 01 10 11	BAK PF0 PF1 PF2
						Bit 7 = 1	11	PF3
6	5	20	8	1	1	- 00 01 10 11	0 1 1 1 1	BAK PF0 PF1 PF2 PF3
7	5	20	16	1	1	- 00 01 10 11	0 1 1 1 1	BAK PF0 PF1 PF2 PF3

CHBASE (Character Address Base Register) (D409): This address writes data into the Character Address Base Register. The data specifies the most significant byte (MSB) of the address of the desired character set (see section II). Note that the last 1 or 2 bits are assumed to be 0.

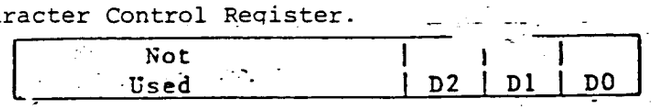
40 Character Modes



20 Character Modes



CHACTL (Character Control) (D401): This address writes data into the Character Control Register.



D2 Character Vertical Reflect Bit. This bit is sampled at the beginning of each line of characters. If true it causes the line of characters to reflect (invert) vertically (for upside down characters).

D1 Character Video Invert Flag (used for 40 Character Mode only). If bit 7 of character code is true this flag causes that character to be blue on white (if normal colors are white on blue).

D0 Character Blank (Blink) Flag (Used for 40 Character Mode only). If bit 7 of character code is true this flag causes that character to blank. Blinking characters are produced by setting bit 7 of the characters to 1, then periodically changing D0 of CHACTL.

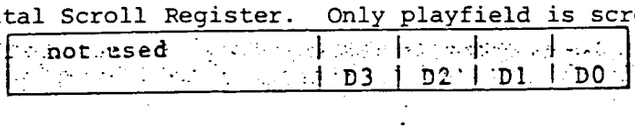
7.0) Vertical and Horizontal Fine Scrolling: Playfield objects are difficult to move smoothly. Memory map playfield can be moved by rewriting sections of memory. However, this is extremely time-consuming if large sections of the screen must be moved smoothly. Character playfield objects can be moved easily in a jerky fashion by changing the memory scan counter. However, this results in a large position jump from one character position to another, not a smooth motion. For this

7.0) Vertical and Horizontal Fine Scrolling: (continued)

reason hardware registers (VSCROL and HSCROL) and counters are provided to allow smooth horizontal or vertical motion, up to one character width horizontally and up to one character height vertically. After this much smooth motion has been done by increasing the value in these registers, memory is rewritten or the memory scan counter is modified and smooth motion is resumed for another character distance.

7.1) Horizontal Scrolling:

HSCROL (Horizontal Scroll Register) (D4 04): This address writes data into the Horizontal Scroll Register. Only playfield is scrolled, not players and missles.



The display is shifted to the right by the number of color clocks specified by HSCROL for each display list instruction that contains a 1 in its HSCROL Flag bit (bit 4 of instruction byte).

When horizontal scrolling is enabled, more bytes of data are needed. For a narrow playfield (see DMACTL bits 1 and 0) there should be the same number of bytes per line as for standard playfield with no scrolling. Similarly, for standard playfield use the same number of bytes as for the wide playfield. For wide playfield, there is no change in the number of bytes and background color is shifted in.

7.2) Vertical Scrolling:

A zone of playfield on the screen can be scrolled upward by using VSCROL and bit 5 of the display list instruction. The display blocks at the upper and lower boundaries of the zone must have a variable vertical size. In particular, the first display block within that zone must be shortened from the top, and the last display block must be shortened from the bottom (i.e. not all of the top and bottom blocks will be displayed).

The vertical dimension of each display block is controlled by a 4 bit counter within the ANTIC, called the 'Delta Counter' (DCTR). Without vertical scrolling, it starts at 0 on the first line, and counts up to a standard value, determined by the current display instruction. (Ex: for upper and lower case text display, the end value is 9. For 5 color character displays, it is 7 or 15.)

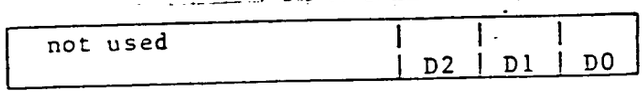
If bit 5 of the instruction remains unchanged between consecutive display blocks, then the second block is displayed in the normal fashion. If bit 5 of the instruction goes from 1 to 0 between two consecutive display blocks, the second block will start

7.2) Vertical Scrolling: (continued)

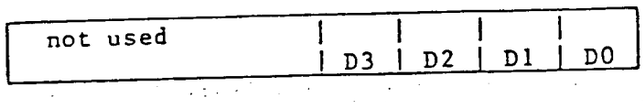
with Delta = 0, as usual, but will count up until Delta = VSCROL, instead of the standard value. This shortens that display block from the bottom.

To define a vertically scrolled zone, the most direct method is to set bit 5 to 1 in the first display instruction for that zone and in all consecutive blocks but the last one. If the VSCROL register is not rewritten on the fly, this results in a total scrolled zone that has a constant number of lines (provided that the VSCROL value does not exceed the standard individual block size). If N is the standard block size, the top block will be N-VSCROL lines (N> VSCROL), and the last block will be VSCROL + 1 lines: (N-VSCROL) + (VSCROL+1) = N + 1. Shown on the following page is an example of a scrolled zone, top block, for 8 VSCROL values for N = 8.

VSCROL (Vertical Scroll Register) (D405): This address writes data into the Vertical Scroll Register.



8 line display modes



16 line display modes

The display is scrolled upward by the number of lines specified on the VSCROL register for each display list instruction that contains a 1 in its VSCROL Flag bit (bit 5 of instruction byte). The scrolled area will terminate with the first instruction having a zero in bit 5.

13.0) ELECTRICAL PARAMETERS:

13.1) GENERAL:

A) Storage temperature $-40^{o}C$ to $+90^{o}C$
B) Ambient operating temperature $0^{o}C$ to $+70^{o}C$
C) Failure rate less than 0.1% per 1000 hours
D) Maximum voltage range on any pin with respect to VSS (Pin 1: substrate) without permanent damage to the chip -0.5V to +9.0V

13.2) D.C. OPERATING CHARACTERISTICS:

All voltages are referenced to VSS (pin 1).

	MIN.	TYP.	MAX.	UNIT
VCC (PIN 21)	+4.75		+5.25	VOLTS
ICC (PIN 21)			150.0	mA
NON-MASKABLE INTERRUPT INPUT: (WITH INTERNAL PULL-UP DEVICE)				
$\overline{\text{RNMI}}$ (PIN 6)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{PULL-UP}$ INPUT PULL-UP CURRENT:Vin=2.4V	-100.0			uA
C_{PIN} PIN CAPACITANCE			7.0	pf
DATA BUS I/O:				
D0-D3 (PIN 30-PIN 33), D4-D7 (PIN 40-PIN 37)				
INPUT:				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: OUTPUT TRI-STATED VIN=+7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			10.0	pf
OUTPUT:				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.4			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			130.0	pf

13.2) D.C. OPERATING CHARACTERISTICS:(CONT.)

All voltages are referenced to VSS (pin 1).

	MIN.	TYP.	MAX.	UNIT
R/W INPUT WITH INTERNAL ENHANCEMENT PULL-UP:				
R/W (PIN 14)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			7.0	pf
OUTPUT:				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.4			VOLTS
C_{LOAD} LOAD CAPACITANCE			30.0	pf
NORMAL OUTPUTS:				
AN0 (PIN 2), AN1 (PIN 3), AN2 (PIN 5)				
Ø0 (PIN 34)				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.8			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			25.0	pf
NORMAL OUTPUT:				
$\overline{HALT}$ (PIN 9), $\overline{NMI}$ (PIN 7), $\overline{REF}$ (PIN 8)				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.8			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			30.0	pf
READY OUTPUT: OPEN DRAIN OUTPUT				
RDY (PIN 15)				
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS PULL-DOWN IS TURNED OFF			10.0	uA
C_{LOAD} LOAD CAPACITANCE			30.0	pf

13.2) D.C. OPERATING CHARACTERISTICS:(CONT.)

All voltages are referenced to VSS (pin 1).

	MIN.	TYP.	MAX.	UNIT
ADDRESS BUS I/O: TRI-STATED OUTPUTS				
A0-A3(PIN 13-PIN 10), A8-A9(PIN 24-PIN 23),				
A10(PIN 16),A11(PIN 22), A12-A15				
(PIN 17-PIN 20)				
INPUT:				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: OUTPUT TRI-STATED VIN=+7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			10.0	pf
OUTPUT:				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.4			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			30.0	pf
ADDRESS BUS I/O: TRI-STATED OUTPUTS				
A4-A7(PIN 28-PIN 25)				
INPUT:				
$I_{LEAKAGE}$ INPUT LEAKAGE: OUTPUT TRI-STATED VIN=+7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			10.0	pf
OUTPUT:				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.4			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			30.0	pf

13.2) D.C. OPERATING CHARACTERISTICS:(CONT.)

All voltages are referenced to VSS (pin 1).

	MIN.	TYP.	MAX.	UNIT
INPUT CLOCK :				
Ø2 (PIN 29)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			10.0	pf
FAST PHASE INPUT CLOCK :				
FØ2 (PIN 35)				
V_{IH} INPUT HIGH VOLTAGE:	2.8		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			7.0	pf
SCHMITT TRIGGER INPUT):				
RES (PIN 36), LP (PIN 4)				
V_{T+} POSITIVE-GOING THRESHOLD VOLTAGE:	1.9		2.6	VOLTS
V_{T-} NEGATIVE-GOING THRESHOLD VOLTAGE:	1.0		2.1	VOLTS
V_{HYS} HYSTERESIS:	0.3			VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			7.0	pf

13.3) DYNAMIC OPERATING CHARACTERISTICS:

(VDD = 5V±5% TA = 0^{o} to 70^{o}C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNIT
CLOCK TIMING:						
Ø2 INPUT:						
LOGIC HIGH TIME			T_{HI}	230	260	nS
RISE TIME			T_{R}		25	nS
FALL TIME			T_{F}		25	nS
FAST PHASE CLOCK INPUT: FØ0						
LOGIC HIGH TIME			T_{HI}	105	135	nS
RISE TIME			T_{R}		30	nS
FALL TIME			T_{F}		25	nS
PHASE ZERO CLOCK OUTPUT: Ø0						
LOGIC HIGH TIME			T_{HI}	270	290	nS
RISE TIME			T_{R}		50	nS
FALL TIME			T_{F}		50	nS
OUTPUT DELAY TIME	1	ALE FØ0	T_{DS}		165	nS
INPUT TIMING:						
R/W SETUP TIME		BLE Ø2	T_{RWS}	130		nS
R/W HOLD TIME		ATE Ø2	T_{RWH}	30		nS
ADDRESS SETUP TIME: A0-A3,A8-A15		BLE Ø2	T_{ADS}	130		nS
ADDRESS HOLD TIME: A0-A3,A8-A15		ALE Ø2	T_{ADH}	30		nS
DATA SETUP TIME : D0-D7		BTE Ø2	T_{DSW}	50		nS
DATA HOLD TIME : D0-D7		ATE Ø2	T_{DHW}	10		nS
DATA SETUP TIME : $\overline{RNMI}$		BTE Ø2	T_{DS}	50		nS
DATA HOLD TIME : $\overline{RNMI}$		ATE Ø2	T_{DH}	10		nS

NOTE:
1) OUTPUT LOAD AT 25pF + 1 TTL LOAD.

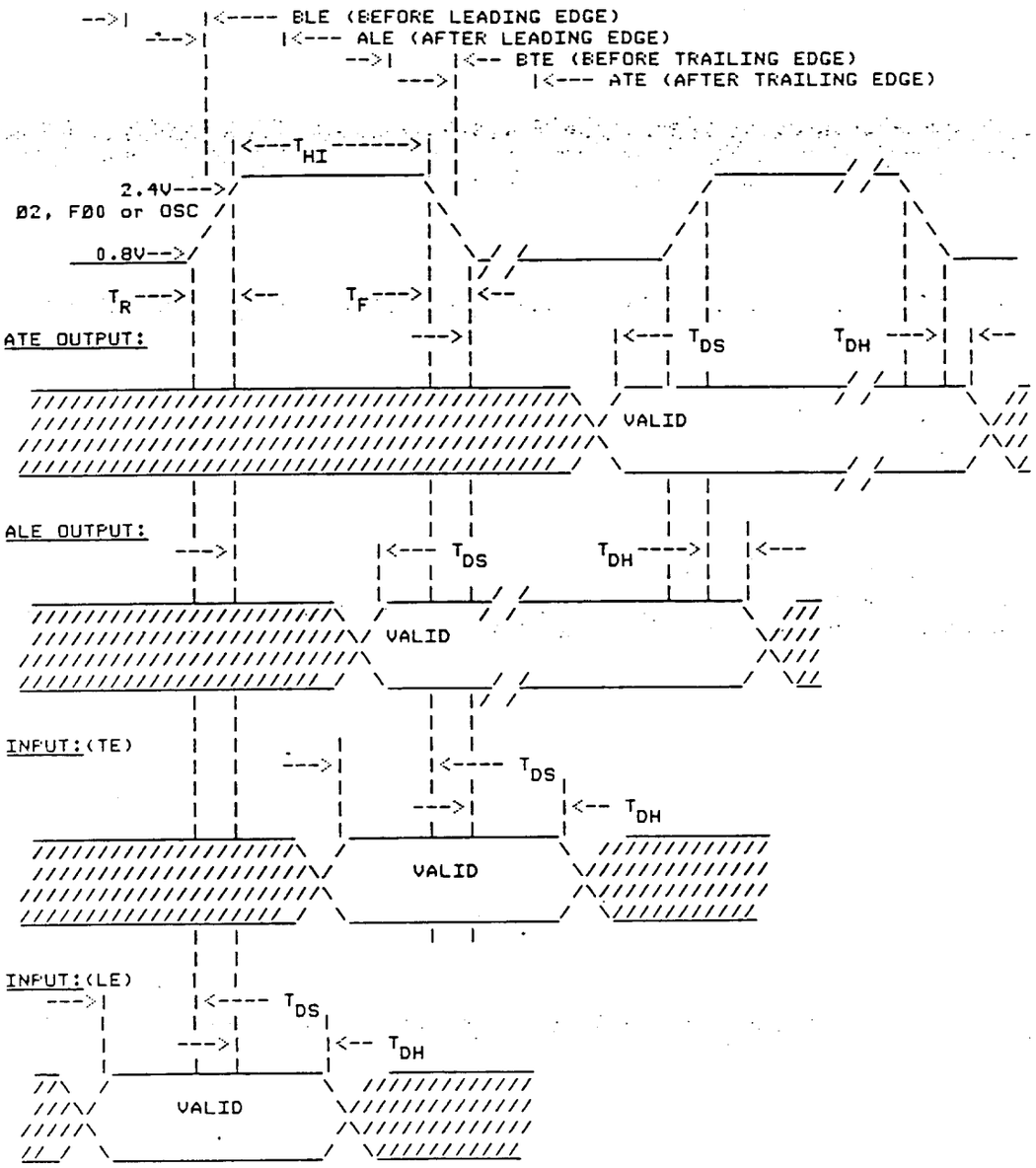
13.3) DYNAMIC OPERATING CHARACTERISTICS: (CONT.)

(V_{DD} = 5V±5% TA = 0° to 70°C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNIT
INPUT TIMING: (CONT.)						
DATA SETUP TIME : $\overline{RES}$		BTE OSC	T_{DS}	50		nS
DATA HOLD TIME : $\overline{RES}$		ATE OSC	T_{DH}	130		nS
DATA SETUP TIME : $\overline{LP}$	4	BTE Ø2	T_{DS}	50		nS
		BLE Ø2	T_{DS}	50		nS
DATA HOLD TIME : $\overline{LP}$		ATE Ø2	T_{DH}	850		nS
		ALE Ø2	T_{DH}	850		nS
OUTPUT TIMING:						
R/W SETUP TIME	2	ATE Ø2	T_{RWS}		230	nS
R/W HOLD TIME	2	ATE Ø2	T_{RWH}	23		nS
ADDRESS SETUP TIME: A0-A15	2	ATE Ø2	T_{ADS}		145	nS
ADDRESS HOLD TIME: A0-A15	2	ATE Ø2	T_{ADH}	14		nS
DATA SETUP TIME : D0-D7	3	ALE Ø2	T_{DSW}		185	nS
DATA HOLD TIME : D0-D7	3	ATE Ø2	T_{DHW}	10		nS
DATA SETUP TIME : $\overline{HALT}$, $\overline{NMI}$	2	ATE Ø2	T_{DS}		350	nS
DATA HOLD TIME : $\overline{HALT}$, $\overline{NMI}$	2	ATE Ø2	T_{DH}	35		nS
DATA SETUP TIME : RDY	2	ATE Ø2	T_{DS}		180	nS
DATA HOLD TIME : RDY	2	ATE Ø2	T_{DH}	18		nS
DATA SETUP TIME : $\overline{REF}$	2	ATE Ø2	T_{DS}		150	nS
DATA HOLD TIME : $\overline{REF}$	2	ATE Ø2	T_{DH}	15		nS
DATA SETUP TIME : AN0-AN2	1	ALE FØ0	T_{DS}		195	nS
DATA HOLD TIME : AN0-AN2	1	ALE FØ0	T_{DH}	19		nS

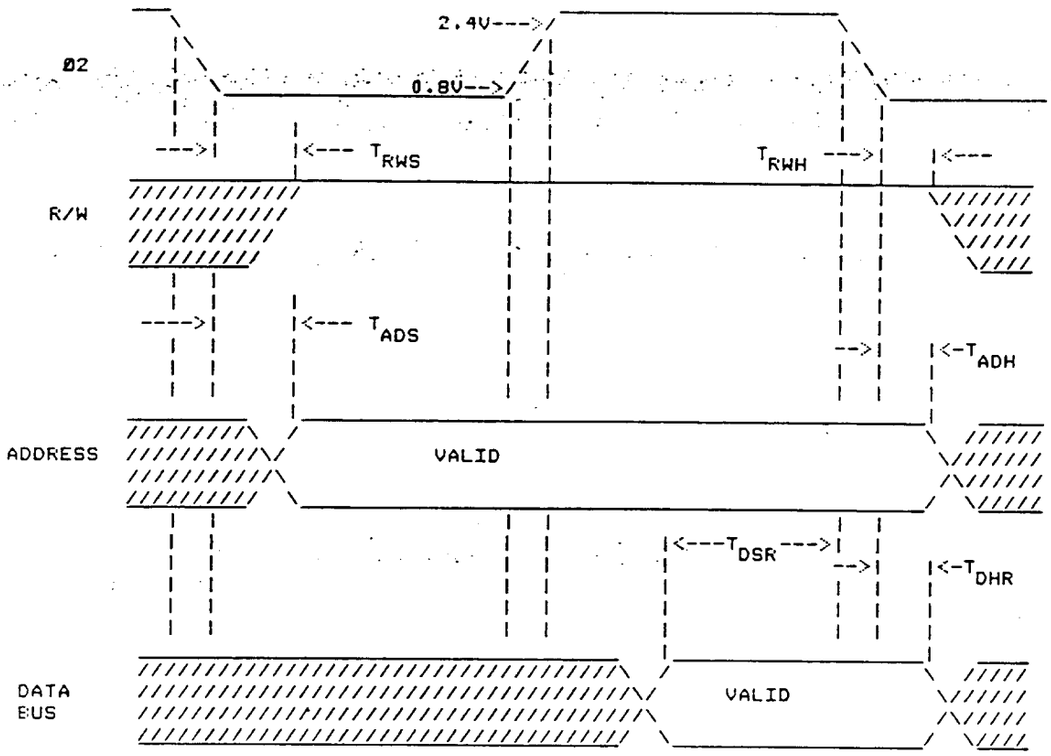
NOTE:
1) OUTPUT LOAD AT 25pF + 1 TTL LOAD.
2) OUTPUT LOAD AT 30pF + 1 TTL LOAD.
3) OUTPUT LOAD AT 130pF + 1 TTL LOAD.
4) LIGHT PEN INPUT CAN OCCUR ON BOTH EDGES OF Ø2. THE EDGE THAT IT DOES OCCUR ON WILL DETERMINE THE VALUE OF THE LEAST SIGNIFICANT BIT.

13.4) I/O TIMING:



ATARI	TITLE ANTIC (NTSC)		
	DRAWING NO. C012296	REV D	SHEET 40 OF 45

13.6) READ I/O TIMING: (ANTIC READING FROM THE RAM)



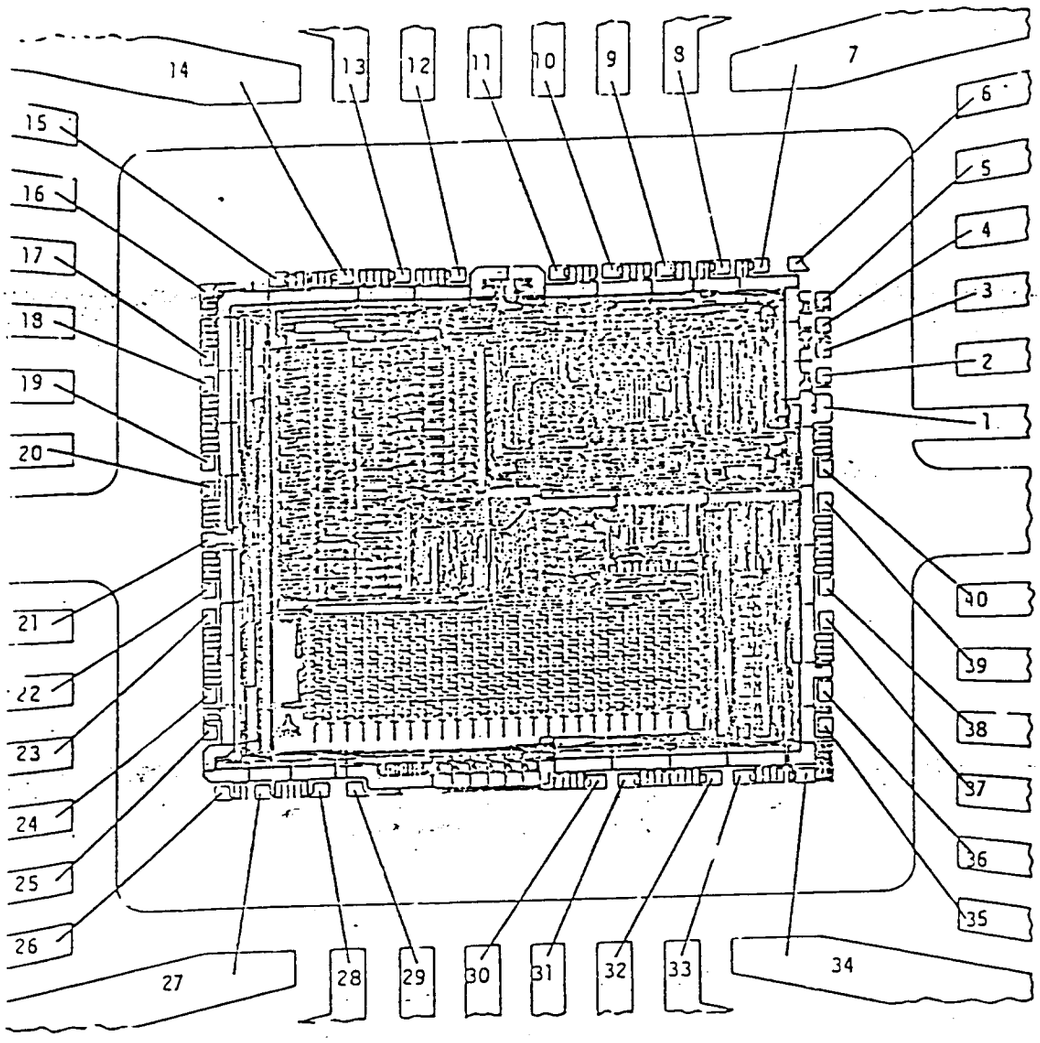
ANTIC ADDRESS TABLE

	WRITE		READ	
ADDRESS	NAME	DESCRIPTION	NAME	DESCRIPTION
D400	DMACTL	DMA CONTROL REGISTER		
D401	CHACTL	CHARACTER CONTROL REGISTER		
D402	DLISTL	DISPLAY LIST POINTER (LOW BYTE)		
D403	DLISTH	DISPLAY LIST POINTER (HIGH BYTE)		
D404	HSCROL	HORIZONTAL SCROLL REGISTER		
D405	VSCROL	VERTICAL SCROLL REGISTER		
D406				
D407	PMBASE	PLAYER-MISSILE BASE ADDRESS REGISTER		
D408				
D409	CHBASE	CHARACTER BASE ADDRESS REGISTER		
D40A	WSYNC	WAIT FOR HORIZONTAL BLANK SYNCHRONISM		
D40B			VCOUNT	VERTICAL LINE COUNTER
D40C			PENH	HORIZONTAL LIGHT PEN REGISTER
D40D			PENV	VERTICAL LIGHT PEN REGISTER
D40E	NMIEN	ENABLE NMI INTERRUPTS		
D40F	NMIRES	RESET NMI INTERRUPT STATUS REGISTER	NMIST	NMI INTERRUPT STATUS REGISTER
D410 thru D4FF	> REPEATED 15 TIMES AS ABOVE			

ANTIC PIN LIST

PIN #	PIN NAME	DESCRIPTION
1	VSS	GROUND
2	AN0	ANTIC INTERFACE TO GTIA
3	AN1	ANTIC INTERFACE TO GTIA
4	LP	LIGHT PEN INPUT
5	AN2	ANTIC INTERFACE TO GTIA
6	$\overline{\text{RNMI}}$	NMI INTERRUPT INPUT
7	$\overline{\text{NMI}}$	NMI INTERRUPT OUTPUT
8	$\overline{\text{REF}}$	RAM REFRESH OUTPUT
9	$\overline{\text{HALT}}$	HALT OUTPUT
10	A3	ADDRESS I/O
11	A2	ADDRESS I/O
12	A1	ADDRESS I/O
13	A0	ADDRESS I/O
14	R/W	READ/WRITE I/O
15	RDY	READY OUTPUT
16	A10	ADDRESS I/O
17	A12	ADDRESS I/O
18	A13	ADDRESS I/O
19	A14	ADDRESS I/O
20	A15	ADDRESS I/O
21	VCC	POWER +5V
22	A11	ADDRESS I/O
23	A9	ADDRESS I/O
24	A8	ADDRESS I/O
25	A7	ADDRESS I/O
26	A6	ADDRESS I/O
27	A5	ADDRESS I/O
28	A4	ADDRESS I/O
29	Ø2	COMPUTER PHASE 2 INPUT
30	D0	DATA BUS I/O
31	D1	DATA BUS I/O
32	D2	DATA BUS I/O
33	D3	DATA BUS I/O
34	Ø0	PHASE 0 OUTPUT
35	FØ0	FAST PHASE 0 INPUT
36	$\overline{\text{RES}}$	RESET INPUT
37	D7	DATA BUS I/O
38	D6	DATA BUS I/O
39	D5	DATA BUS I/O
40	D4	DATA BUS I/O

ANTIC BONDING DIAGRAM



ASSEMBLY INFORMATION

a. Die Size: 196 x 221
b. Package: (Plastic) 7200171
c. Assembly Code: TCF-X
D. Special Processing ☐ No ☐ Yes-See added page
E. Bond

ATARI	TITLE ANTIC (NTSC)			
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